Understanding Quantum Technologies

Ninth edition – 2026

Part 2/5 – Quantum Hardware

Olivier Ezratty

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Olivier Ezratty is an author, academic, teacher and advisor on quantum technologies. He started this endeavour in 2018.

He is the author of the reference book "Understanding Quantum Technologies" (September 2021, 2022, 2023, 2024, 2025 and 2026) following three previous editions in French in 2018, 2019 and 2020. The 2025 edition is also available in paperback version on Amazon. This 2026 edition's Amazon print version will be available before the end of 2026.

Since 2021, he has been teaching quantum technologies at EPITA, an IT engineering school in France, at Ecole Normale Supérieure Paris-Saclay since 2024 and CentraleSupelec since 2005. He's affiliated with the EPITA Research lab for his various research writings.

He is a cofounder of the Quantum Energy Initiative in 2022 with Alexia Auffèves (CNRS MajuLab Singapore), Robert Whitney (CNRS LPMMC) and Janine Splettstoesser (Chalmers University, Sweden), and member of its scientific board.

He acts as an independent expert for Bpifrance and at the Agence Nationale de Recherche (ANR) to evaluate quantum R&D projects, as a member of the European Quantum Computing Advisory Board (Q-CAB) since April 2026, and of the Inria expert group for the selection of risky research projects (Programme PIQ) since June 2024.

Since 2018, he has spoken in a large number of quantum technology events such as the Q2B Paris and Santa Clara organized by QC Ware, France Quantum, Lindau Nobel Laureate meeting, DPG, Q-Expo and other events, on top of presentations at Société Générale, BNPParibas, Crédit Agricole, Michelin, Adéo, L'Oréal, FIECC, IHEDN, Business France, CentraleSupelec, Avolta Partners, IHEDN, etc.

He coproduces two series of podcasts on quantum technologies along with Fanny Bouton (in French): a monthly "Quantum " on tech news (since September 2019) and Decode Quantum (2020-2026), with entrepreneurs and researchers, with a total of about 170 episodes as of September 2026.

He also lectures or lectured in various universities such as CentraleSupelec, ENSTA, Telecom Paristech, Les Gobelins, HEC, Neoma Rouen and SciencePo, on artificial intelligence, entrepreneurship and product management (until 2020) and on quantum technologies (since 2018), in French and English as needed. He is also the author of many open-source ebooks in French on entrepreneurship (2006-2019), the CES of Las Vegas yearly report (2006-2020) and on artificial intelligence (2016-2021).

Beforehand, Olivier Ezratty was specialized in many other topics since 2005, like digital television, internet of things and artificial intelligence. As such, he carried out various strategic advisory missions, conferences, or training assignments in different verticals and domains such as media and telecoms, finance and insurance, industry and services and the public sector.

Olivier Ezratty started in 1985 at Sogitec, a subsidiary of the Dassault group, where he was successively Software Engineer, then Head of the Research Department in the Communication Division. He initiated developments under Windows 1.0 in the field of editorial computing as well as on SGML, the ancestor of HTML and XML. Joining Microsoft France in 1990, he gained an extensive experience in many areas of the marketing mix: products, channels, markets and communication. He launched in France the first version of Visual Basic in 1991 and Windows NT in 1993. In 1998, he became Marketing and Communication Director of Microsoft France and in 2001, of the Developer Division, which he created in France to launch the .NET platform and promote it to developers, higher education and research, as well as to startups. Olivier Ezratty is a software engineer from Centrale Paris (1985), which became CentraleSupelec in 2015.

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Foreword

The birth of the second quantum revolution may be reasonably settled to 1982, with two celebrated articles: "Experimental Test of Bell's Inequalities Using Time-Varying Analyzers" by Alain Aspect and colleagues, and the famous theoretical paper "Simulating Physics with Computers" by Richard Feynman. They were quickly followed in 1985 by David Deutsch's "Quantum theory, the Church–Turing principle and the universal quantum computer", providing the birth certificate of what is known now as quantum computing. Incidentally, I got a position at CNRS also in 1982, a good spot to witness these developments. However these subjects, including the surprising quantum key distribution scheme proposed by Charlie Bennett and Gilles Brassard in 1984, were still quite confidential at that time. It took ten more years for the topic to attract broad international attention, with the articles "Algorithms for quantum computation: Discrete logarithms and factoring" (1994) and "Polynomial-Time Algorithms for Prime Factorization and Discrete Logarithms on a Quantum Computer", both by Peter Shor.

This started an explosive development, which has not stopped since then. The big impact of Shor's algorithm is that it may break cryptographic codes that were considered fully secure at that time, and are still broadly used on internet - so each layman gets concerned. This, and other reasons, triggered a huge international effort to build a quantum computer. Since it was clear that such a computer was still far away, this effort was mostly academic during the next 20 years. But another earthquake happened in 2014, when large US companies, Google and IBM as the most visible ones, decided to get into the race. They set up heavily funded research programs, focused on a specific technology, superconducting quantum bits. This move stimulated a high level of private investment, leading to the creation of a flurry of dedicated companies, initially startups, but then quite respectable enterprises in terms of funding. They were not limited to superconductors, but included all quantum objects likely to become a quantum bit, a qubit : ions, atoms, photons, and even more exotic ones. One must honestly say that, from this time, the language used in this research field changed significantly: the way to speak with investors is not the same as the way to publish articles in reputable scientific journals. The result was a mixture of authentic scientific and technological progress, coming together with hype and overselling. This may be seen either as an unavoidable evil, or as the appropriate way to communicate in an extremely competitive high-tech environment.

A good example is the way to name the "ultimate goal", the point where a quantum computer can really achieve a useful task that no classical computer can do in any reasonable time. The first name that popped up was "quantum supremacy", but it did not make it, both for technical and political reasons. The next one was "quantum advantage", more politically correct, but still difficult to warrant. The next one is "quantum utility", clearly more modest, but more likely to be reached in a reasonable time span. In the current language, "utility" is used as a step towards "advantage", with some possible oscillations between the two due to progress in classical computing.

Then a question arises : given the very fast progress of the devices, their technical complexity, and the strange mixture of science and publicity used by companies to communicate their results, how to find one's way in the jungle, without getting lost or eaten ? One would need somebody with good scientific and technological knowledge, but also a huge talent for global accounts, given the many facets of these developments, involving physics, hardware, software, middleware, logistics, and finance. We are lucky enough that this person exists, his name is Olivier Ezratty, and you hold his book in your hands or on your computer screen. This is not a modest enterprise, and ≈1,822 pages carefully written in LaTeX is a minimal container. Go for it, it's free ! But how to approach such a monument ? Fortunately there is a reading guide in the first pages, able to orient you depending on your background and interests. It includes also an illustrated "Pandora's box", listing the main high level topics (physics, mathematics, human sciences, engineering, computer science, geopolitics), together with their inner content, opening doors towards many stimulating questions for science, technology, and society.

So where do we stand now, already 44 years after the baby was born ? The general idea is that the real stuff, the one needed for supremacy / advantage / utility for practical problems of industrial interest, requires what is called now "Fault Tolerant Quantum Computing" (FTQC), in the line of Deutsch's ideas; this is quite attractive for computer scientists, but very hard to achieve. Physicists tend to prefer quantum simulators, in line with Feynman's ideas, potentially useful for more fundamental physics problems. Myself, as a physicist, will go for the second trail, because one should not dismiss fundamental physics problems: it is by solving them that science made progress, and not necessarily by jumping right now into the market. Actually, it is not clear that all fundamental questions to be answered before being able to implement quantum computing have been solved, as summarized in the old joke : "Where is quantum computing? Somewhere between cold fusion and hot fusion", a physicist's warning that nature's laws are not to be fooled around.

Anyway, as we say in French, "*on ne discute pas des goûts et des couleurs*" (there's no accounting for tastes): whatever your personal interest is - physicist, computer scientist, or investor -, and wherever you may want to look at - computing, communications, sensors or metrology - the development of quantum technologies is a fascinating arena where much more is expected to come.

I cannot close this foreword without a few words about another ongoing revolution, artificial intelligence and large language models generative artificial intelligence (simplified as "LLM"). The most straightforward step forward, taking place currently in all domains of scientific and technical activities, is to use LLM as super-efficient assisting tools; their progress during the 2 or 3 last years has been astonishing, and it cannot be listed here. Another more speculative idea is to think about a "quantum AI", an AI running on a quantum computer. The mismatch between the current performances of quantum computers, and what is used now on supercomputers running AI, makes this objective extremely far-fetched. Still, blue-sky thinking about what might be achieved by such machines - and even the question of whether they will still be "machines", is attracting attention by some quantum theoreticians. Where will these revolutions lead humanity ? Only time will tell.

Philippe Grangier

Director of Research emeritus at CNRS, Institut d'Optique Graduate School (IOGS), and incoming President of the French Optical Society (SFO).

September 2026

Contents

This is **Part 2/5 – Quantum Hardware** of the book "Understanding Quantum Technologies 2026", which is also downloadable using this link.

The downloadable PDFs are available in a single A4 and Letter version, containing the five parts in sequential order. You can also download compressed PDFs for the five parts in A4 and Letter formats. Their size fits the constraints of ebook readers like the Kindle from Amazon.

The e-reader and printed version of the book separates parts 1, 2, 3, 4 and 5.

- The **first part** contains a history of quantum physics, some quantum physics 101 and everything about quantum computing basics and engineering including quantum error correction, the energetics of quantum computing, a view on pessimism and optimism with regard to the advent of scalable and useful quantum computers, as well as some economic considerations.
- This **second part** contains the sections dedicated to quantum computing hardware with all types of qubits and their related industry vendors, enabling technologies, and unconventional computing solutions which are potential alternate routes between classical and quantum computing.
- The **third part** contains the sections dedicated to algorithms, software tools, and applications across multiple markets. It also contains an inventory of quantum computing software and service vendors.
- The **fourth part** covers quantum communications, quantum cryptography, post-quantum cryptography and quantum sensing.
- The **fifth part** describes the quantum ecosystem at the entrepreneurial level, the country level, on various societal topics, corporate adoption methodologies, quantum pseudosciences. It ends with a glossary, and book bibliography.

The book is split into five parts to make its printing easier, some online printing services including Amazon being limited to a maximum of 600 pages.

You can order the printed version of this book in five parts on all Amazon sites by searching for the book title, edition 2026, when it is released around October-November 2026.

1 Quantum computing hardware

In a bottom-up approach, we have covered successively the basics of quantum physics, the mathematical aspects of gate-based quantum computing, then quantum computing engineering and enabling technologies. Let us now move to the last stack, quantum computers, focusing on their specifics depending on the types of physical quantum objects they are using, mostly based on qubits. We are dealing here with all sorts of players: public research laboratories, large established companies as well as startups.

1.1 Segmentation

There are nine main categories of quantum objects used in quantum computers. They can be grouped into three families: atomic systems, solid-state electronic and microwave-circuit systems, and flying photonic or electronic qubits. These types of quantum objects can be sub-segmented in many different categories, as shown in Figure 1. Why quantum objects and not qubits? Because some of these quantum objects can be used to create qutrits and even qudits.

1.1.1 Atoms

This is one of the oldest types of quantum objects used to build qubits. It consists of controlling atoms in a vacuum with lasers, with one qubit being encoded per atom. Cold atoms are neutral while trapped ions are ionized atoms. One key difference is how these atoms are controlled in space. Ions can be positioned with electrodes and magnetic fields while non-ionized atoms are only controlled by lasers. They both share a similar measurement technique using laser excitation, fluorescence and visual readout with some CCD or CMOS imaging sensor.

- **Trapped ions** are atom ions that are kept in a vacuum and suspended by electrostatic suspension. They are electromagnetically trapped, and their initialization is done with laser optical pumping. Lasers are used to cool and stabilize the ions, exploiting the Doppler effect, with different energy transitions than those used to modify the state of the qubits. The most frequently used ions are calcium and strontium. Single-qubit quantum gates are activated by microwaves, lasers or magnetic dipoles. Lasers or electrodes are used for two-qubit quantum gates. While trapped ions are best-in-class for qubit fidelity and connectivity, it seems currently difficult to scale them beyond a couple dozen ions and they are very slow.
- **Neutral atoms**, *aka* cold atoms, are cooled at very low temperatures, also using the Doppler effect and other laser-based techniques. The elements used can be rubidium, an alkaline metal, as well as strontium. The quantum state of these cold atoms is their energy level, which can use their Rydberg high-excitation states on some occasions, in analog quantum simulation mode, and lower-energy levels for gate-based implementations.
- **Nuclear Magnetic Resonance** qubits were tested over 20 years ago and are nearly completely abandoned besides one startup in China (SpinQ). Most of the time, they are based on using ensembles of atoms or molecules. Ensemble liquid-state NMR quantum computing has severe scalability limitations, on polarization and individual addressability, and is no longer a leading route to large-scale quantum computing. It is a good demonstration that qubits research must remain open and cannot be settled too early around one or two technologies. Even now, it is too early to tell which qubit type will really scale to create useful quantum computers.

1.1.2 Electrons and microwave cavities

This other category of qubits is about electrons that are controlled most of the time in solid-state circuits instead of vacuum like with cold atoms and trapped ions.

- **Superconducting** qubits are a broad category with Josephson qubits (transmon, fluxonium, coaxmon, unimon, ...) and bosonic qubits using microwave photon cavities (cat-qubits, GKP, dual-rail) with Alice&Bob, AWS, Nord Quantique and QCI. Josephson-junction-based qubits use the state of an oscillating superconducting current that crosses a very thin barrier in a loop, usually a metal oxide such as aluminum, using the Josephson effect. There are several types of superconducting qubits: flux, phase, and charge. The most common one is the transmon, a variation of charge superconducting qubits. In all cases, qubit observables are two very distinct energy and phase levels of a high frequency oscillating current flowing through the Josephson junction. The oscillation is made possible by the fact that the loop integrates the equivalent of an inductance and a capacitance. The current oscillation is activated by microwave pulses using frequencies between 4 and 8 GHz and transmitted by coaxial wires and operating at about 15 mK. In transmon qubits, the qubit observable is measured with a resonator integrated in the circuit which receives a microwave and sends it back. The readout electronic system splits out the amplitude and phase of the readout microwave to detect the

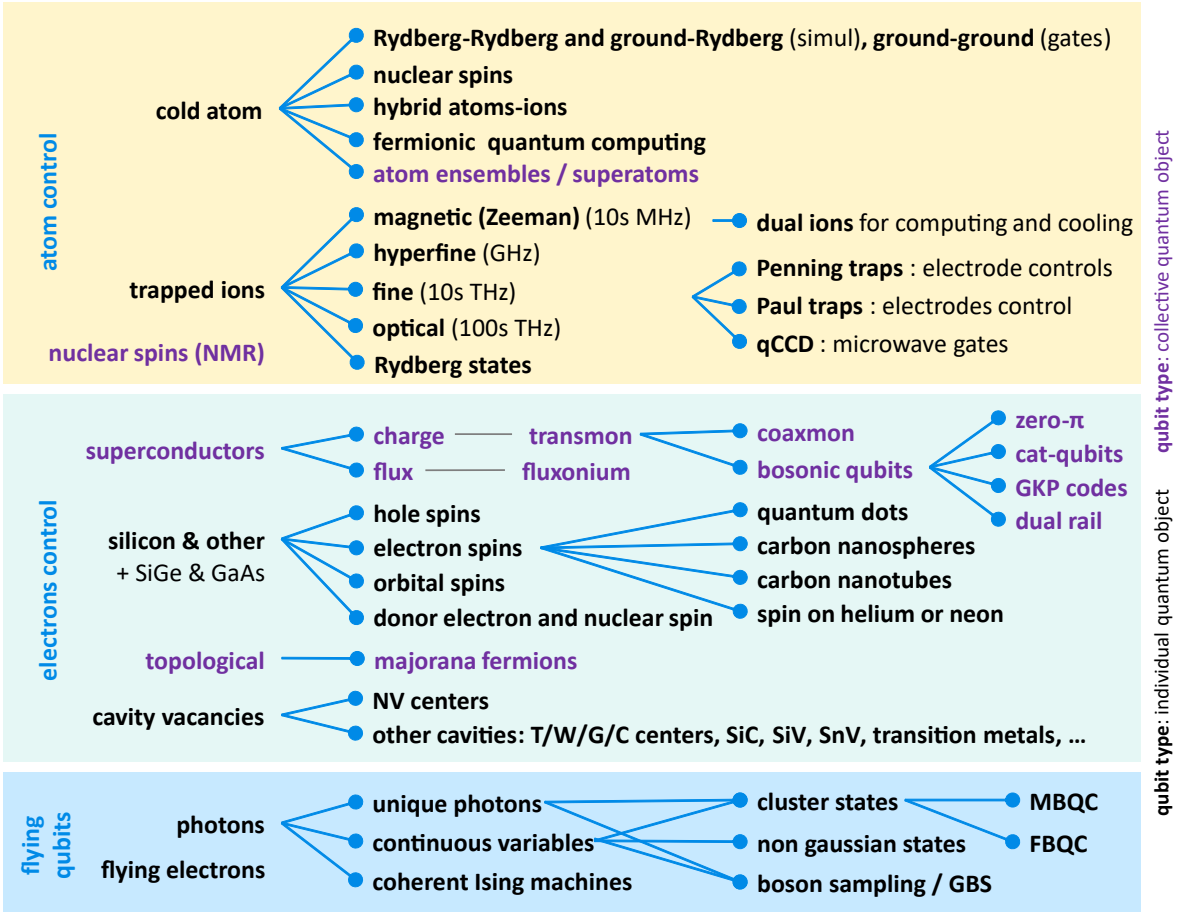


Figure 1: Rough zoology of qubits/qudits classes and sub-classes. In purple, collective quantum objects, and black, individual quantum objects. ⓒ Olivier Ezratty, 2021-2024.

qubit value. In some transmons, individual qubits' activation frequency is tuned by a direct current flux bias line.

- **Quantum dots spin qubits** are developed with scalability in sight. Most of them use two electrons trapped in a quantum well, one containing the qubit and the other one used to measure it. These qubits are usually manufactured using silicon-based CMOS circuits. Silicon is often supplemented with various dopants.

- They benefit from the reuse of CMOS manufacturing processes that are already well mastered. These qubits are easy to miniaturize down to below 100 nm. They work at temperatures between 100 mK and 1K, higher than superconducting qubits, allowing the use of more electronics around the chip, to generate the microwaves and other electric signals required to create qubit gates and handle qubit readout. This promising technology is however less mature than superconducting qubits. No lab or company has really exceeded fully 12 functional qubits as of 2026.

- **NV centers** (Nitrogen Vacancy) are artificial diamond structures in which a carbon atom has been replaced by a nitrogen atom near a carbon atom gap. Qubit states and control rely on a combination of electron, nitrogen and carbon ^{13}C nucleus spins. Qubit gates are implemented with microwaves, a magnetic field, and an electric field. Entanglement is handled with photons, magnetic coupling or with controlling the core spin of neighboring ^{13}C carbon atoms via the use of microwaves to create a CNOT gate. Qubit readout uses a laser and fluorescence detection. There are many variants with other types of vacancies such as silicon carbide (SiC). This type of qubit is also used in quantum sensing and quantum communications.

- **Topological qubits** are anyons or quasiparticles which are usually particular states of Cooper pairs in condensed matter at very low temperature. These qubits use braiding, a topological effect that makes it possible to implement error correction at the qubit level. It could enable scalable fault-tolerant quantum computers. These must also be cooled at around 10 mK. This is the path chosen by Microsoft with its Majorana fermions. Their existence is not yet proven. It is one of the most hazardous paths to quantum computing. Other topological qubits avenues are investigated in research laboratories at the fundamental research level.

	atoms		superconducting & controlled spin			photons
quantum objects	**trapped ions**	**cold atoms**	**super-conducting**	**quantum dots spins**	**vacancies (NV, SiC, …)**	**photons**
gate-based computing	main model	emerging model	main model	main model	possible	main model
analog quantum simulation	tested	main model	tested	tested		tested in CV mode
quantum annealing			D-Wave			
quantum memory	in repeaters	in repeaters			in repeaters	with cold atoms or delay lines
quantum telecoms & QKD	photon sources	repeater memory			photon sources	QKD protocols transport
quantum sensing	electric field, clocks	gravity, RF	SQUIDs, magnetism		magnetism	clocks, radars, LiDARs

Figure 2: Qubit types and their use cases in all quantum computing paradigms and in telecommunications and sensing. Light green means: less commonplace and/or harder to implement. Olivier Ezratty, 2022-September 2026.

1.1.3 Flying qubits

Flying qubits are special because they travel from the place where they originated, traverse physical devices acting on them and terminate their journey on a sensor measuring one observable. They have a limited time available to run any computing, including a finite and small number of quantum gates.

- **Photon qubits** are the most common flying qubit and there are many varieties of implementations. One type is based on a horizontal/vertical polarization observable. Others use continuous variables qubits. Boson sampling systems use multimode photons. It is quite difficult to implement two-qubit gates with these photon qubits, thus the alternative of the MBQC architecture that is an interesting workaround. Also, photon generation follows a probabilistic pattern which makes things complicated when the number of qubits grows. Most of these qubits operate at room temperature, but the photon sources and their detectors must, however, usually be cooled to temperatures between 4K and 10K, which is much less demanding than the 15 mK of superconducting qubits or the 1K of silicon qubits.

- **Flying electrons**, a separate track of qubits, with no commercial vendor yet involved in it. It is a fundamental research field[1, 2]. It is based on using single-electron transport circulating on wave guide nanostructures built on semiconductor circuits, mostly GaAs, leveraging Coulomb coupling, quantum charge Hall effect and surface acoustic waves. Single- and two-qubit quantum gates can be realized on such circuits. Electrons can fly at a distance of between 6 and 250 μm. They are created by producing THz photons which are converted into electrons. There are even electron-hole flying qubits [3].

- One qubit uses two-electron paths for states $|0\rangle$ or $|1\rangle$ [4–6]. At the end of processing, these flying electrons are detected by a quantum dot (Figure 3). This technique could also be used to create electron-shuttling qubits connecting static quantum-dots-based qubits together. A few labs in the world are working on this including NPL in the UK, Ruhr-Universität Bochum, NTT, ERATO-JST and AIST in Japan, Weizmann Institute in Israel, CEA-Leti and Institut Néel in Grenoble, France.

Table 1 presents a summary of the scalability challenges faced by the main qubit types around (I left aside topological and NV centers qubits). Many of these topics are detailed in this part and others in the "enabling technologies" part [22]. The table lists a lot of enormous challenges. For each of these, many research teams and vendors are proposing many different approaches and options. The upside is it is reassuring, the downside being that these options are still very immature, and you must look at the details of their figures of merit to understand how it could scale. I make a broad inventory of the various envisioned solutions but am not in a position to assess their viability in most cases.

1.1.4 Industry vendors

Most of the above-mentioned quantum object types inventoried before are used by a wealth of industry vendors. The number of vendors keeps growing, as shown in Figure 4, with over 90 companies as of September 2026 , and it keeps growing.

It reminds me of the Wacky Races movie and cartoons vehicles as well as the Tatooine podracers in Star Wars I, with an amazing technology diversity and true believers in their fate. The only difference is we may end up with no single winner but several winners if not some forms

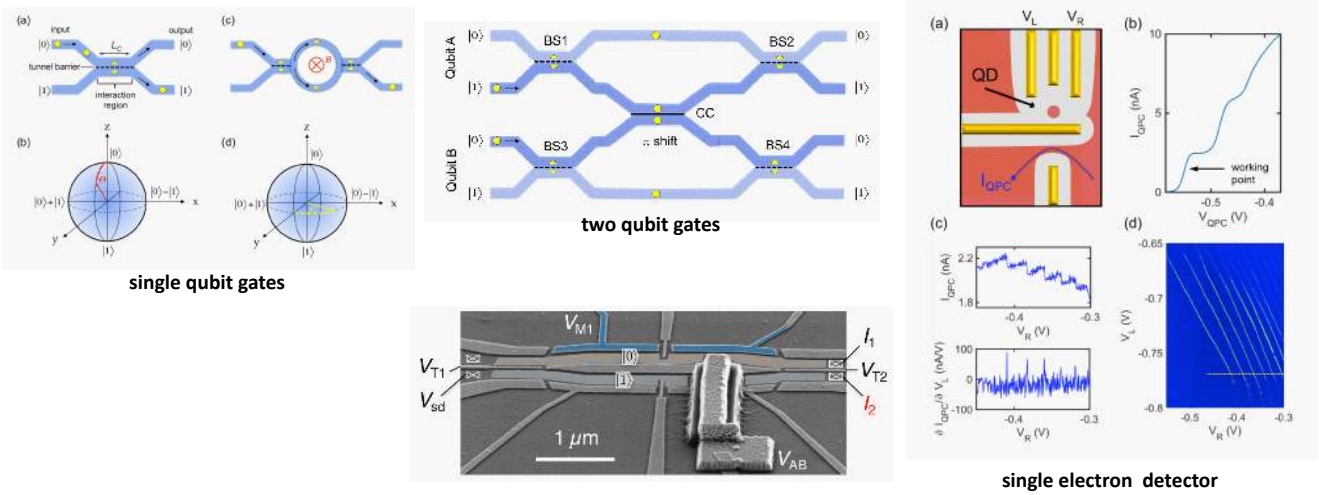


Figure 3: Flying electrons in their waveguides. Their circuit architecture has some features in common with photonic circuits. Source: [5].

of technology hybridization. Can we compare it to the Manhattan project from 1940-1945? It had only two main uranium and plutonium combustible options and some variations with the explosives, with a future project to create fusion bomb, which was implemented later in 1952. Here, with quantum computing, researchers and industry vendors are investigating many more options.

These categories of technologies have different levels of maturity. Superconducting qubits are the most proven to date. Trapped ions are best-in-class regarding fidelity and connectivity but do not seem to scale well. Neutral atoms are starting to scale better. Linear optics and NV centers also have some difficulties to scale. Electron spin-based systems could scale but are less mature. Finally, Majorana fermions are still in limbo. But other qubit types are looming around and may become promising (other topological materials, Silicon Carbide, etc.).

Assessing the maturity of these technologies is closer to weather forecast than climate change predictions. While you can forge some ideas on the relative maturity of these technologies with a short-term view, it is much harder to make sound predictions in the longer term. For example, scaling these various technologies faces very different challenges. As such, the table in Table 2 is an approximate and date-sensitive comparison between these different qubits. Many cells are not directly comparable since experimental conditions and maturity differ, particularly with cold atoms, which are so far used in quantum simulation mode and not in gate-based architectures.

Figure 2 shows how various qubit types have use cases beyond quantum computing and even, within the three paradigms of quantum computing with all qubit types being usable for quantum simulations although it seems it is only available with neutral atom qubits with commercial vendors [178]. Photons, cavity spins and cold atoms have the broadest use cases given they have many applications in quantum sensing. Silicon qubits seem to have a narrower usage scope but don't discount them too soon. They may showcase one of the best scalability potentials for quantum computing.

All in all, two overarching questions remain: how many entangled objects can be controlled in an efficient manner and with low noise, and how deterministic photon entanglement interconnectivity will scale without an exponential overhead that would kill any quantum advantage?

1.1.5 FTQC roadmaps

In Figure 5, I consolidated the public FTQC roadmaps of quantum hardware vendors. They document up to three key metrics:

- **Number of supported gates** or operations with relates to a supported logical error rate, in LQOPs (quantum logical operations).
- **Number of logical qubits**, which can be a flexible number with the same number of physical qubits. Users can choose to favor circuit breadth (number of logical qubits) or circuit depth (number of gate cycles) with the same number of physical qubits.
- **Number of physical qubits** that support all of this, and gives some indirect indication on the QPU size.

Other optional roadmap items, not consolidated in the figure would be very helpful, particularly when they provide some qualitative and quantitative operational data:

- Clock speed or number of shots per second in the case of analog quantum computers.
- Number of logical operations per second.

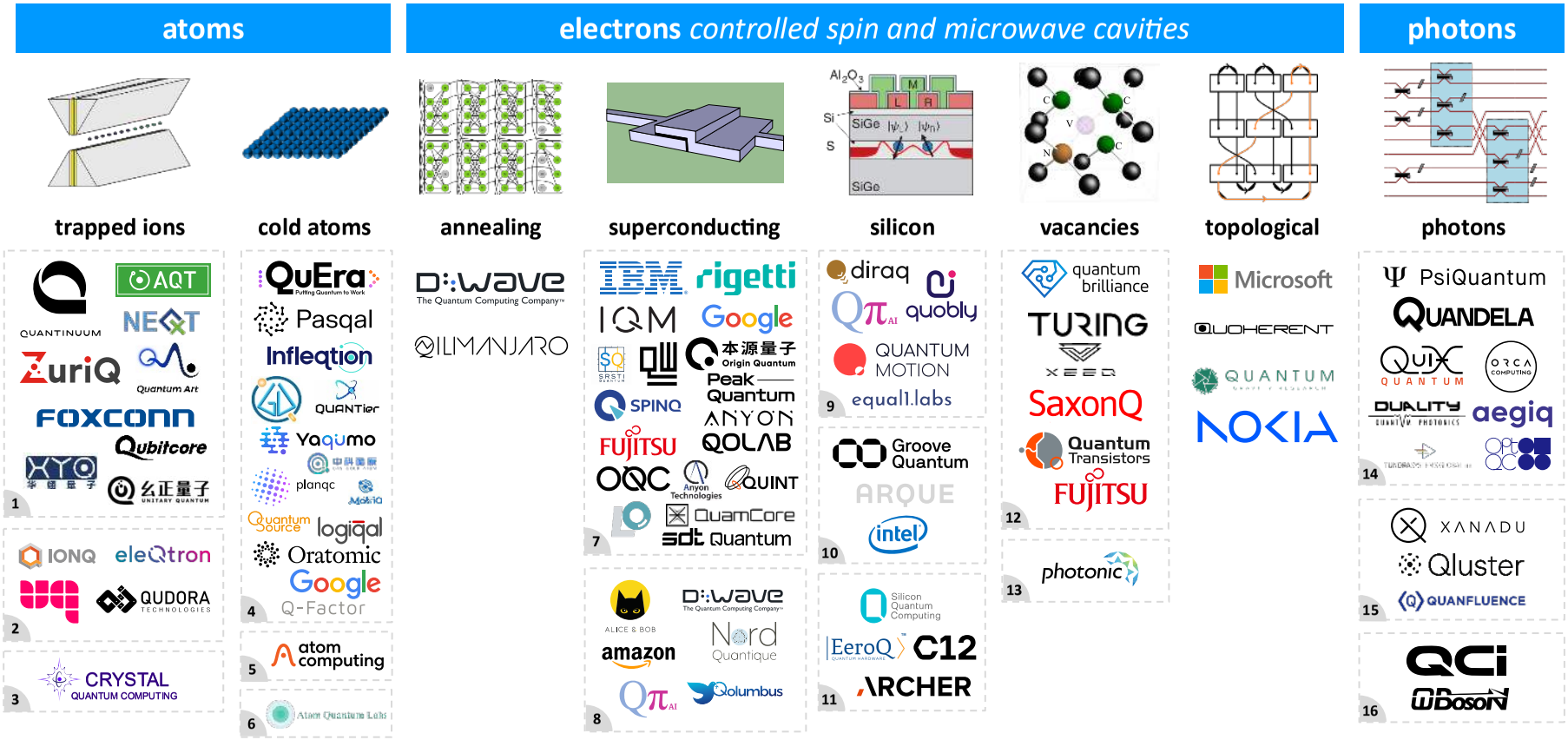


Figure 4: Map of the ≈90 industry vendors in quantum computing hardware per qubit type. Some qubit categories are organized in subclasses as follows: (1) for laser driven ions, (2) for microwave driven ions, (3) for ions in Rydberg states, (4) for regular cold atoms, (5) for cold atoms with nuclear spin manifold, (6) for a variant of cold atoms with ionization preparation, (7) for transmon superconducting qubits, (8) for other superconducting qubits like bosonic qubits, dual rail qubits and fluxonium qubits, (9) for silicon spin qubits, (10) for silicon-germanium qubits, (11) for other spin variant qubits like nanosphere and nanotubes, spin on helium and donor spin, (12) for NV centers qubits, (13) for silicon vacancies qubits, (14) for discrete variable photon qubits, (15) for continuous variable photon qubits and (16) for coherent Ising model photonics systems. 🅭 Olivier Ezratty, September 2026.

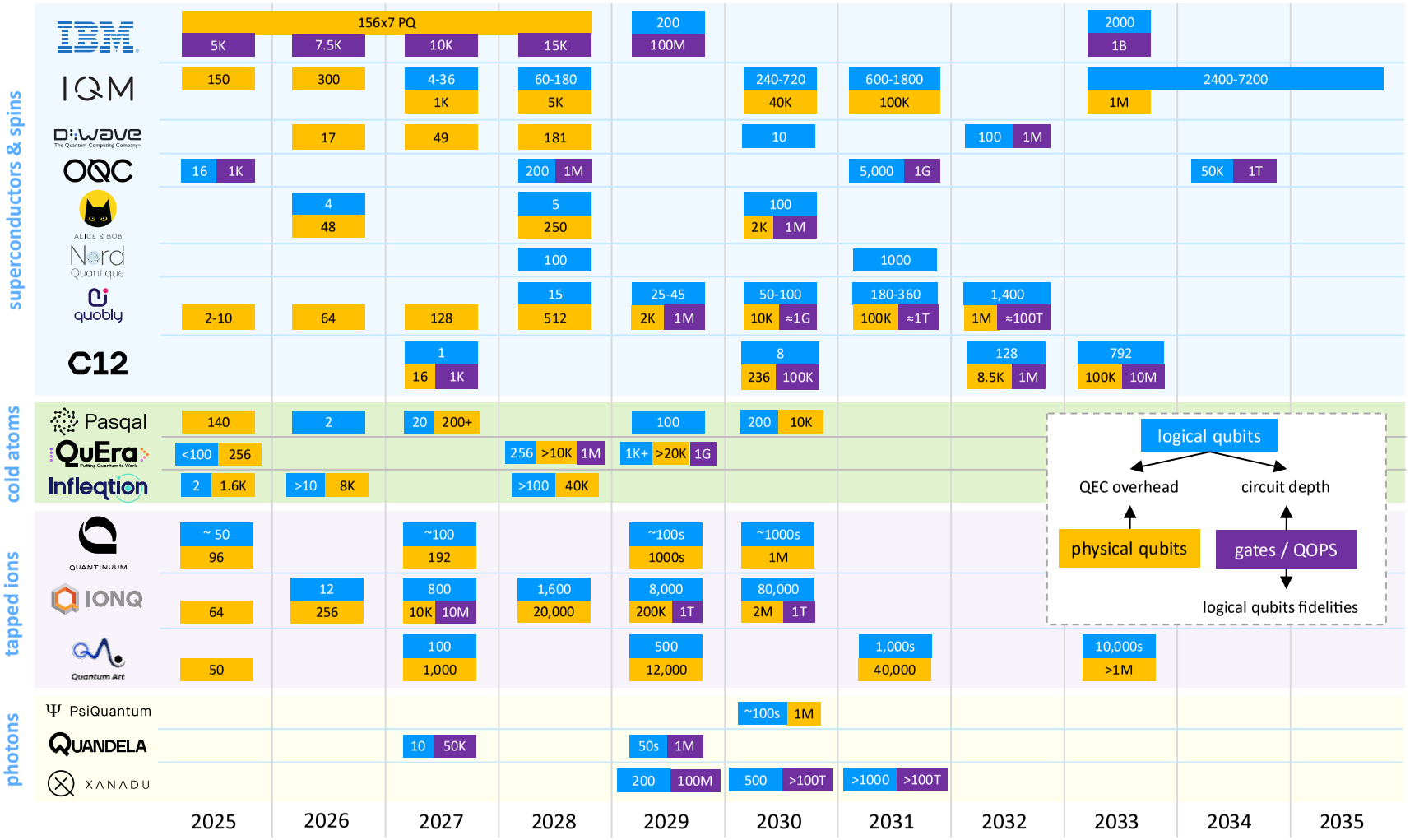


Figure 5: Consolidation of quantum computer industry vendors roadmaps per qubit type with physical qubits, logical qubits and number of logical operations. Roadmap values are vendor targets. These roadmaps were published at variable dates and are frequently updated to account for usual delays. Roadmap sources: IBM in 2025 [7], IQM in 2025 [8], OQC in 2025 [9], Alice & Bob in 2025 [10], Nord Quantique in 2025 [11], Quobly in 2025 [12], Pasqal in 2025 [13], QuEra in 2024 [14], Infleqtion in 2025 [15], Quantinuum in 2024 [16], IonQ in 2025 [17], Quantum Art in 2026 [18], PsiQuantum in 2025 [19], Quandela in 2025 [20], Xanadu in 2026 [21]. 🅭 Olivier Ezratty, September 2026 and vendor roadmaps officially published.

trapped ions	neutral atoms	superconducting	silicon spins	photons
challenges				
▪ slow two-qubit gate speed [23, 24]. ▪ scaling the number of ions per interaction zone while maintaining high-fidelity gates and motional-mode control [25, 26]. ▪ motional heating and motional-mode management [27]. ▪ control-signal variability [28, 29]. ▪ laser amplitude, frequency and phase stability [30].	▪ maintaining uniform high-fidelity control with 1000s of atoms [31, 32]. ▪ fast mid-circuit measurement, reset and QND readout with low crosstalk [33]. ▪ atom loading, rearrangement and replenishment overhead [34]. ▪ laser amplitude and phase noise. ▪ atom loss and leakage during computation [35].	▪ noise and crosstalk ↗ with # of qubits [36, 37]. ▪ electronics energetic cost [38, 39]. ▪ scaling cryogenic I/O, cabling and circulators [38]. ▪ cryostat cooling-power and thermal-load scaling [40, 41]. ▪ getting $> 99.9\%$ two-qubit gate fidelities with large chips [42, 43].	▪ precise electrostatic control of large quantum-dot arrays [44]. ▪ two-qubit gate fidelities at scale [45, 46]. ▪ charge noise and qubit variability [47, 48]. ▪ device variability and automated tuning of large quantum-dot arrays. ▪ limited native connectivity and high-fidelity transport between distant qubits [49].	▪ photon-source efficiency and indistinguishability [50]. ▪ photon losses in circuits [51, 52]. ▪ detector efficiency, photon-number resolution and large-scale cryogenic integration [53, 54]. ▪ scalable generation of entangled cluster states (RSG) [55, 56]. ▪ probabilistic entanglement increasing resource-state and multiplexing overhead [57].
solutions				
▪ QCCD and microwave qubit drive [58–60]. ▪ ion shuttling [61]. ▪ multiple ion species [62]. ▪ Rydberg-state ions [63, 64]. ▪ photonic QPU interconnects [65, 66]. ▪ 2D QCCD and multilayer traps [67, 68].	▪ movable atoms for two-qubit gates and readout [69]. ▪ multiple atomic species [70, 71]. ▪ higher-power, lower-noise and highly parallel laser control. ▪ atom replenishment techniques [72–74]. ▪ atom-photon conversion for interconnects [75]. ▪ faster FPGA and ASIC controls [76, 77].	▪ materials improvement [78, 79]. ▪ 3D chipset stacking [80, 81]. ▪ cryo-CMOS or SFQ [82, 83]. ▪ microwave-signal multiplexing [84]. ▪ higher cooling-power and more efficient cryogenic architectures, JJ circulators [85]. ▪ scale-out with photons [86, 87]. ▪ mid-range couplers enabling qLDPC codes [88, 89].	▪ material and interface improvement [90, 91]. ▪ integrated cryoelectronics [92, 93]. ▪ more powerful cryostats [94]. ▪ industrial CMOS-compatible fabrication and process optimization [95, 96]. ▪ electron shuttling and spin buses for long-range coupling [49, 97].	▪ high-efficiency, deterministic and indistinguishable photon sources [98]. ▪ deterministic sources of cluster states [99]. ▪ MBQC / FBQC models [55, 100]. ▪ hybrid integrated nanophotonics [52, 101]. ▪ photon routing and multiplexing [102, 103]. ▪ fast cryogenic feedforward control [104].
caveats				
▪ photonic interconnect viability [105, 106]. ▪ photonic interconnect statistics and impact on speedups [66].	▪ gate control precision at scale [107]. ▪ scaling repeated high-fidelity QEC cycles while controlling atom loss, leakage and correlated errors.	▪ photonic interconnect overhead and statistics [86]. ▪ energetic cost of microwave multiplexing and control drive [39]. ▪ SFQ backaction on qubits [82].	▪ understanding noise sources [108, 109]. ▪ scalability potential is capital intensive. ▪ two-qubit gate fidelities improving more slowly than single-qubit fidelities [110].	▪ obtain photon-loss budget matching FTQC requirements. ▪ sufficiently large cluster state generation [56]. ▪ nanophotonic circuit losses [52, 111]. ▪ overheads generated by photon losses and probabilistic fusions [51].

Table 1: Key challenges, solutions and caveats for the top five qubit technologies. 🅭 Olivier Ezratty, 2022-September 2026.

- Planned error correction codes and methods.
- Processor size and reliance on QPU interconnect.
- Nominal power consumption, fully burdened.
- Processor and components operating temperature.
- QPU weight and size.
- Operational constraints like temperature variability.
- QPU and components MTBF (mean time between failure) which may be important for some critical components.
- End-user capex and opex cost structure.
- When was the roadmap published and/or updated.
- Later, compare actual delivery vs roadmap. This is something that we can already do with some past NISQ vendor roadmaps. In most of the cases, vendors were late on their roadmaps by between 1 and 3 years, or they quietly changed their roadmaps to hide it.

By the way, you can read the May 2025 report on FTQC from the French Academy of Technology [179]. I was one of the cowriters of the report which explains why you will find there some (older version) charts from this book.

What is the most promising qubit type?

This question is on the lips everywhere in the ecosystem, particularly with governments who may be willing to prioritize their scattered investments, or private investors and stock-exchange traders who are selecting a startup.

The response ranges from "none" to "many", with intermediate answers such as "some of them" and "I don't know". The most honest answer would be the latter.

When you consider all the scaling challenges presented in Table 1 as well as in the tables for each individual qubit type and paradigms (quantum annealing in Figure 9, superconducting in Figure 19, quantum dots spins in Figure 115, vacancies in Figure 163, topological in Figure 174, ions in Figure 187, in cold-atoms Figure 238 and photons in Figure 279), you understand that all of them face a complex mix of scientific and technology development challenges. In these charts, the right column cells with challenges and solutions are filled with complex and interacting elements.

The challenge is still about scaling the number of physical qubits *while* while maintaining physical error rates (PER) at a level compatible with the selected error correction codes, ensuring the best non-local qubit connection, experimenting them, and implementing full-fledged FTQC architectures implementing all Clifford and non-Clifford logical gates. And without using post-selection during the logical circuit execution. All qubit types face materials and manufacturing quality challenges either at the qubit chip level (for superconducting, silicon, and trapped-ions qubits, and for photon sources, detectors and integrated photonics) or at the enabling technologies level (lasers and light-forming devices for cold-atoms, cryoelectronics, and cabling for solid-state qubits, etc.).

Scaling is also about testing our experimental capabilities and the laws of quantum physics. We don't know yet how far we can go by controlling a large many-body entangled state. Testing is the only way to know.

The "some of them" response can be related to the potential hybridization of qubit types in full-fledged systems, with different qubits types used for connectivity (photons), quantum memory (vacancies, cold-atoms) and fast computing (superconducting, silicon). This is a scenario that is dependent on the capability to interconnect these different qubit types, which is an enormous scientific and technology challenge, particularly when it involves transduction between the microwave and optical photon regimes.

At last, unrelated with the best-qubit quest lies an underlying question about finding algorithms which will deliver a practical quantum advantage whatever its nature (computing time, result quality, energy consumption).

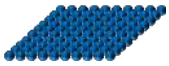
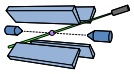
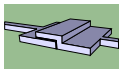
	atoms		electrons: *controlled spin and microwave cavities*			photons
						
	cold atoms	**trapped ions**	**superconducting**	**silicon spin**	**NV centers**	**photons**
qubit size	3 to 5 μm pitch, tweezer waist <1 μm [32, 112]	2 to 5 μm between ions, 30 to 100 μm between QCCD zones	$(100\ \mu\text{m})^2$, miniaturization degrades coherence [113, 114]	$(100\ \text{nm})^2$ [49, 115]	$< (100\ \text{nm})^2$ cavity, ≈4 μm diamond cell [116]	no fixed size, set by waveguides, MZI, PBS and delay lines [53]
best two-qubit gate fidelities	99.85% CZ, 374-atom QuEra array [117] 99.40% raw on 256 qubits (Atom Computing) [118]	99.92% on 98 qubits (Quantinuum Helios) [119, 120] 99.97% on 10 ions (Oxford Ionics) [121]	99.86% iSWAP and 99.67% CZ on 105 qubits (Google Willow) [122] 99.7% on 156 qubits (IBM Heron r2)	no randomized-benchmarked value above 2 qubits yet: 99.32% on 4 and 99.9% CZ on 11 donor qubits (SQC) [123, 124]	99.2% on the 5-qubit Quantum Brilliance system [125], >90% on 4 qubits (XeedQ)	98.2% on 12 qubits (Quandela) [126], 99.22% fusion on Omega test chips (PsiQuantum) [53]
best readout fidelities	99.93% QND (Atom Computing) [127], 99.6% non-destructive (QuEra) [128]	99.95% (Helios) [119], SPAM 99.9904% [129], heralded SPAM error $< 10^{-5}$ [130]	99.18% on 105 qubits (Zuchongzhi 3.0) [131], IBM Heron values published on the cloud only	99.44% in 175 ns (SQC) [132], 99.2% single-electron box (Quantum Motion) [133]	≈98%, limited by fluorescence contrast and readout scaling [134]	89% detection efficiency, 96% with PNRD (PsiQuantum) [53], 93% SNSPD [135]
best readout time	2.4 μs at 99.4% [136], a few μs at >99.9% on Yb tweezers [137], 1 to 10 ms in commercial arrays	11 μs at 99.93% with SNSPDs [138], 46 μs with a trap-integrated SNSPD [139], 100 μs to 1 ms with PMTs and cameras	56 ns integration at 99.77% on 4 multiplexed qubits, 115 to 215 ns with resonator ring-down [140]	175 ns at 99.44% (SQC) [132], a few μs with RF reflectometry	tens of μs for single-shot resonant readout at 4 to 8 K [141], averaged over many shots at RT	<1 ns detection with 3 ps SNSPD jitter [142], 10 to 50 ns detector reset
best two-qubit gate time	≈200 ns CZ, sub-ns Rydberg gates in lab [143], >1 ms per layer with shuttling [69]	10 to 100 μs, 950 μs (IonQ Forte) [144], 40 to 55 ms per layer with transport (Helios) [119]	20 ns to 300 ns [145], 30 to 48 ns CZ (IQM) [146]	40 to 75 ns [147, 148]	10 to 700 ns on electron spins, 13 μs for a nuclear-spin CNOT [149]	<1 ns, set by the optical path, 10 ns SPAM in cavity-QED blueprints [150]
best T_1	40 s on 100 atoms [151], 3,000 s in a cryogenic array [152], 2 h trap lifetime at 4 K [153]	seconds to minutes, >10 h with sympathetic cooling [154]	100 to 400 μs transmons, >1 ms fluxonium [155, 156], 22 s cat-qubit bit-flip [157]	>1 s with >3 ms T_2 on SiGe dots [158], 9 s on an isolated Si qubit [159]	400 μs at room temperature [160, 161], 1 mn on a 10-qubit register at 3.7 K [162]	∞ and time of flight, limited by optical losses [101]
qubits operating temperature	<1 mK atoms in a RT chamber, 4 K for vacuum and Rydberg lifetime [153, 163]	<1 mK ions, traps at RT to 4-15 K [119]	15 to 20 mK dilution cryostat [38]	100 mK to 1.5 K [94, 147]	RT to 4 K, two-qubit gates needing 1 to 4 K [164, 165]	RT circuits, 2 to 4 K for sources and detectors [166, 167]
operational qubits	256 (Atom Computing) [118], 6,100 to 11,000 atoms trapped without gates [32, 168]	98 (Quantinuum Helios) [119]	156 (IBM Heron)	18 qubits (HRL) [45]	10-qubit register (QuTech) [162]	12 modes (Quandela Belenos, Xanadu Aurora) [169], 32 modes (QuiX)
potential scalability	10,000s per QPU with metasurface traps [31, 32]	1,000s with multi-zone QCCD and photonic interconnect [25, 170]	10K to 20K per chip, 1M with chip interconnect [86, 171, 172]	potentially millions on 300 mm CMOS lines [49, 115]	unknown, 10K claimed with stacked diamond chips [116]	100s to 1M with many interconnected PICs [53, 55]

Table 2: Key figures of merit per qubit type. Best gate time covers only the electronics or optics drive part, not the whole classical drive computing time. Best T_1 is the best qubit relaxation time. RT = room temperature. These are the best figures of merit for commercial systems, but it does not mean a single system in a column has them all. Two-qubit gate and readout fidelities are restricted to commercial-vendor systems characterized on more than two physical qubits. This excludes the usual two-qubit laboratory records: 10^{-7} two-qubit error rates with trapped ions [173], 99.99% on a two-ion Oxford Ionics chip [174], 99.94% on two fluxonium qubits [155], 99.93% on two NV center qubits [175, 176] and >99% on two SiGe qubits. Silicon spin qubits have no published randomized-benchmarked two-qubit fidelity above two qubits, so the cell reports only the best multi-qubit register values. The chart does not include cold atoms and silicon systems with over 1,000 atoms or dots from various vendors and labs since they are not commercial products nor have been characterized for gate-based computing [32, 168, 177]. Superconducting qubits numbers do not include IBM Osprey (433) and Condor (1,121) which were not really functional and were dismantled, nor the 180-qubit Origin Quantum Wukong whose vendor-published 99.9% fidelities are not documented in any scientific paper, or the 504-qubit Xiaohong processor which did not support 2-qubit gates. Google Willow is a research chip and is not commercially available, contrarily to the IBM, Quantinuum, IonQ, Atom Computing, Infleqtion and Quandela systems mentioned here. 🅭 Olivier Ezratty, 2020-September 2026.

1.1.6 Bibliography and notes

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1.2 Quantum annealing

Quantum annealing is a special-purpose quantum computing paradigm based on the controlled evolution of a many-qubit Hamiltonian. It works differently from gate-based quantum computing and is primarily used as a heuristic optimizer or analog quantum simulator. There is no general performance ordering that places quantum annealers between classical supercomputers and fault-tolerant gate-based quantum computers because their accessible problem classes, accuracy, and scaling properties differ (Figure 9). D-Wave is the main commercial player in this category. Several research laboratories also investigate quantum annealing and related Ising machines.

In the 2000s, interest in Shor's factoring algorithm created more traction for gate-based quantum computing, at the expense of quantum annealing. A 2018 experiment reported factoring 376,289 with a D-Wave annealer [180]. This was superseded in 2024 by the factorization $8{,}219{,}999 = 32{,}749 \times 251$ using a compact, Pegasus-specific controlled-full-adder encoding on D-Wave Advantage 4.1 [181]. These records depend strongly on problem-specific classical compilation and concern integers that are trivial for classical computers.

1.2.1 History

The quantum annealing paradigm (QA) seeks low-energy states, ideally the ground state, of a problem Hamiltonian by using quantum fluctuations and quantum tunneling. It is mostly used for discrete combinatorial optimization problems with rugged energy landscapes. Continuous variables and quantum-chemistry problems must first be approximated or encoded into a discrete Ising or QUBO formulation, often with substantial overhead. A finite-temperature, noisy annealer does not guarantee that the global minimum will be found.

The idea to implement quantum annealing using the quantum tunnelling effect came first in 1988 and 1989 from the same group at the University of Milan in Italy [182, 183]. It was then perfected in Japan by **Tadashi Kadowaki** and **Hidetoshi Nishimori** in 1998. They replaced the thermal fluctuations of simulated annealing by "*quantum fluctuations*" that drive transitions between states, tested the idea on the transverse-field Ising model where the field decreases over time much like the temperature in the classical method, and looked for the ground state of the diagonal part of the Hamiltonian as quickly and as accurately as possible [184].

In the ideal closed-system description, quantum annealing starts in the ground state of a driver Hamiltonian, commonly $H_D = -\sum_i \sigma_i^x$, whose ground state is $|+\rangle^{\otimes N}$. The Hamiltonian is then changed from the driver to a problem Hamiltonian that is diagonal in the computational basis. The transverse field is the coefficient of the noncommuting x-directed driver term. In a flux-qubit annealer it is implemented by magnetic-flux controls, but the abstract model does not require a spatially uniform laboratory magnetic field. The Ising model was introduced in statistical physics to describe interacting binary spins. Optimization applications use the same mathematical energy function, with programmable local biases and pairwise couplings.

A year after Tadashi Kadowaki and Hidetoshi Nishimori's paper, **D-Wave** was created in Canada and it sold its first commercial annealer, the D-Wave One, to Lockheed Martin 12 years later, in 2011 [185]. But Japan did not surrender to the idea to create annealing industry solutions. It took the form of a digital annealer created by **Fujitsu** and plans by **NEC** to create a quantum annealer. Also, many Japanese software startups are dedicated to quantum annealing.

At **UCSB**, John Martinis's group studied highly connected superconducting flux-qubit architectures for quantum annealing. The group later focused on gate-based superconducting qubits, and Martinis and part of his team joined Google in September 2014 [186].

In 2000, **Edward Farhi** et al. at MIT introduced an adiabatic algorithm for a satisfiability problem, an algorithmic cornerstone of adiabatic quantum computation and an important precursor of quantum annealing [187].

In 2013, Google and NASA set up the joint Quantum Artificial Intelligence Laboratory, QUAIL, and evaluated D-Wave systems. A highly publicized 2015 benchmark reported a large speedup over simulated annealing for specially constructed instances, but did not establish an end-to-end quantum advantage against the best classical methods Figure 18. The resulting debate damaged D-Wave's credibility in part of the quantum-computing community. Results became more scientifically compelling after 2020 for native Ising-model dynamics, while broad optimization advantage remained unproven.

1.2.2 Science

We must start here with explaining Figure 6 which connects the (quantum) adiabatic theorem and the various forms of digital simulated and quantum annealing:

- The **adiabatic theorem** states, under regularity and spectral-gap conditions, that a system initialized in a nondegenerate eigenstate remains close to the corresponding instantaneous eigenstate when the Hamiltonian changes sufficiently slowly. The required runtime depends on the minimum spectral gap and on matrix elements of derivatives of the Hamiltonian. Max Born and Vladimir Fock formulated an early version in 1928.

- **Diabatic evolution** is deliberately or unavoidably fast enough to induce transitions between instantaneous energy eigenstates. It is not a separate general "diabatic theorem". Controlled diabatic protocols can sometimes reach a useful final state faster than

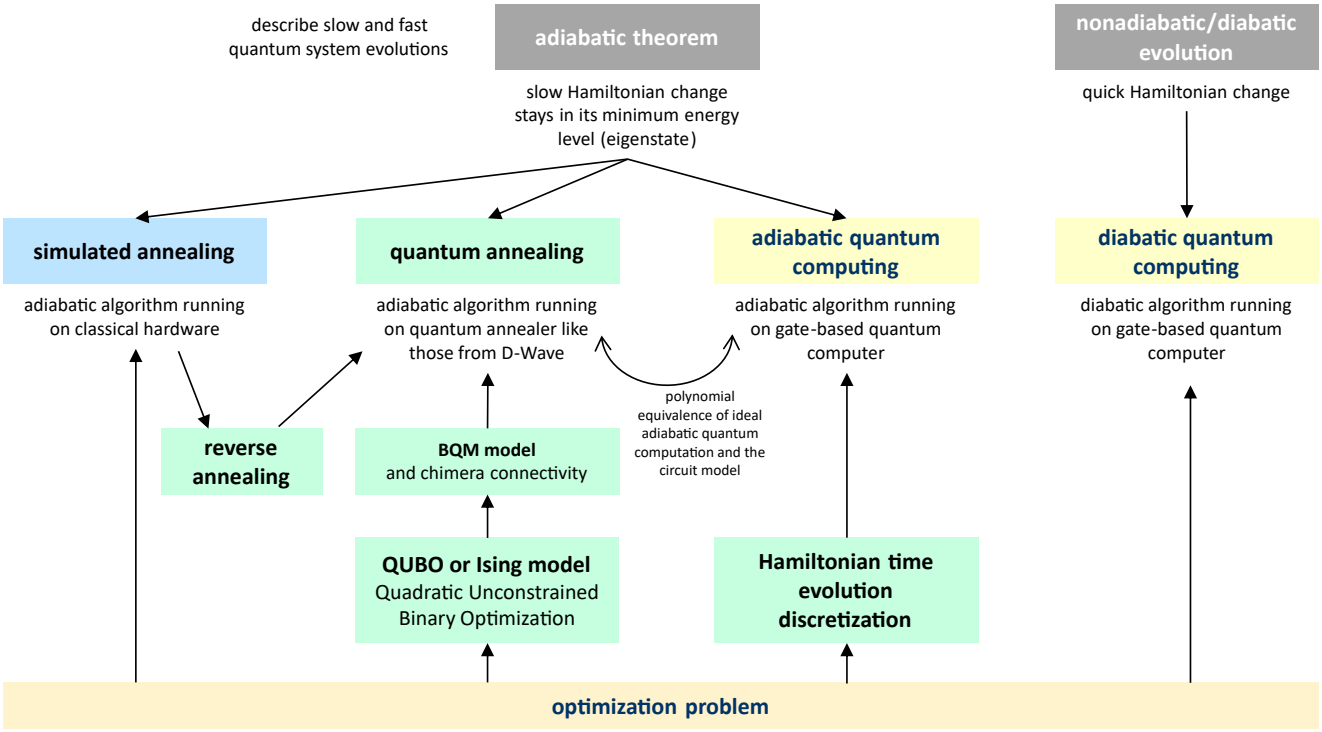

Figure 6: From the adiabatic theorem to quantum annealing. The green rectangles corresponds to what can be done with a quantum annealer. The yellow rectangles correspond to gate-based quantum computing. Blue corresponds to classical computing. Olivier Ezratty, 2022-September 2026, and some references found in [188].

strictly adiabatic evolution, including with locally controlled transverse fields [189].

Implementations are based on:

- **Simulated and digital annealers** run classical heuristics, including Fujitsu's Digital Annealer. They are different from digitized adiabatic algorithms implemented as gate sequences on a QPU [190]. In one 2025 MaxCut benchmark, Fujitsu's Digital Annealer outperformed D-Wave's hybrid solver on the tested QUBO instances, but this workload-specific result is not a general ordering of the two platforms [191].
- **Quantum annealers** such as D-Wave accept a **BQM** (binary quadratic model) expressed either as a **QUBO** (quadratic unconstrained binary optimization) over binary variables or as an equivalent **Ising** model over spin variables. A 2022 benchmark found advantages over selected simulated and digital annealers on some tested use cases, not a universal speed advantage [192].
- **Gate-based quantum computers** using a time discretization of the system Hamiltonian evolution [193].
- **Reverse annealing** starts from a user-supplied classical candidate state, increases quantum fluctuations to explore its neighborhood, and then returns toward the classical problem Hamiltonian. D-Wave has supported it since 2017. It can improve local refinement when a good starting point is available, but it is not generally more efficient than forward annealing [194].
- **Diabatic quantum computing** is also running on gate-based quantum computers modeling a quick Hamiltonian change. It is used as part of the counter-diabatic technique promoted by ParityQC [195–197].

Quantum annealing programs local biases h_i and pairwise couplings J_{ij} in the longitudinal, or z, part of the Hamiltonian. The couplers set interaction energies between connected qubits, while each h_i sets a local energy bias.

The requested h_i and J_{ij} are real-valued coefficients within solver-dependent normalized ranges. Their physical realization has finite resolution, calibration error, noise, and crosstalk. Early D-Wave control systems targeted about four effective bits of Hamiltonian-parameter precision, while their two-stage flux DACs used hundreds of flux steps and approximately eight physical bits to achieve that effective precision [198].

The minor embedding process is about mapping the problem to solve to the quantum annealer qubit structure and connectivity. It sits in the NP-hard realm and is a real bottleneck as problem size grows [199]. There are many optimizations available for this embedding process, particularly for solving optimization problems [200–204]. It can even be done with reinforcement machine learning techniques [205].

Uneven qubit connectivity within the annealing chip must also be considered [206]. Ideally, the system is

initialized in $|+\rangle^{\otimes N}$, the ground state of the transverse-field driver Hamiltonian under the usual sign convention. It is an equal superposition of all 2^N computational-basis states. See examples of QUBO embeddings in a D-Wave Advantage system in [207] and Figure 7.

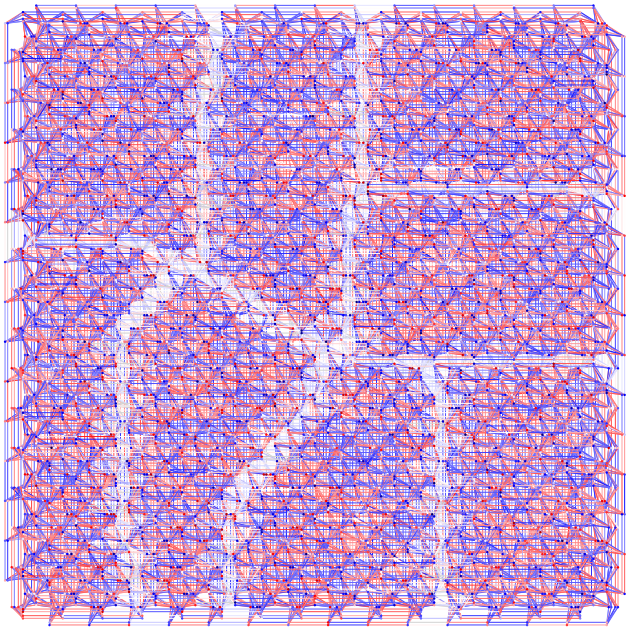

Figure 7: Example of a QUBO problem embedding in a D-Wave Advantage 2. Source: [207].

During the anneal, the driver coefficient $A(\mathrm{s})$ decreases while the problem coefficient $B(\mathrm{s})$ increases, generally according to nonlinear schedules shown in Figure 8. Quantum tunneling and thermal relaxation can help the system move between configurations, while nonadiabatic transitions, thermal excitations, control errors, and freeze-out can leave it in an excited state. Repeated measurements therefore sample a distribution of candidate spin configurations rather than automatically returning the optimum. The analogy with thermal annealing is useful, but the source of fluctuations and the nonequilibrium dynamics differ.

From a mathematical standpoint, the system Hamiltonians $\mathcal{H}_p$, $\mathcal{H}_S$, and $\mathcal{H}_n$ described in Figure 8 are operators represented by $2^N \times 2^N$ matrices for N qubits. The notation σ_j^z in the Ising and annealing Hamiltonians can be confusing.

It denotes the tensor product of the identity on every qubit except j, on which the Pauli Z operator acts. A Pauli operator is a 2×2 matrix and is also a single-qubit unitary gate. Thus, σ_j^z is shorthand for a $2^N \times 2^N$ operator, with I_k denoting the identity on qubit k:

$$\sigma_j^z = I_1 \otimes \cdots \otimes I_{j-1} \otimes Z_j \otimes I_{j+1} \otimes \cdots \otimes I_N$$

Likewise, $\sigma_i^z \sigma_j^z$ denotes a $2^N \times 2^N$ operator with Pauli Z acting on qubits i and j:

$$\sigma_i^z \sigma_j^z = I_1 \otimes \cdots \otimes I_{i-1} \otimes Z_i \otimes I_{i+1} \otimes \cdots \otimes I_{j-1} \otimes Z_j \otimes I_{j+1} \otimes \cdots \otimes I_N$$

The eigenvalues of a system Hamiltonian are its possible energy levels. An ideal adiabatic evolution remains close to the instantaneous ground state under the theorem's conditions. A physical annealer instead returns measured spin values $s_i \in \{-1, +1\}$, with some probability of sampling the ground-state configuration of the final Hamiltonian. It does not explicitly calculate the Hamiltonian spectrum.

The optimization task is to find the configuration of N classical spin variables, denoted $\widehat{\boldsymbol{s}}$, that minimizes the final Ising energy. The search space $\Omega_N = \{-1, +1\}^N$ contains 2^N configurations.

$$\widehat{\boldsymbol{s}} = \underset{\boldsymbol{s} \in \Omega_N}{\arg\min} \left(\sum_{i=1}^{N} h_i s_i + \sum_{1 \le i < j \le N} J_{ij} s_i s_j \right)$$

At the end of the anneal, each flux qubit is measured in the computational basis, producing $s_i = +1$ or -1 according to its persistent-current direction. Quantum nondemolition readout is not required because the final state is not reused. Many anneal-and-read cycles estimate the output distribution and increase the chance of observing a low-energy configuration. The outcomes are probabilistic because of quantum measurement, finite-temperature open-system dynamics, nonadiabatic transitions, analog control errors, and readout errors.

Implementations differ in the available driver and coupling terms. D-Wave implements a transverse-field Ising model with an (x)-directed driver and programmable (z) biases and (zz) couplings. More general (xx), (yy), and (zz) interactions can realize non-stoquastic or Heisenberg-type models, but require additional control hardware. **Qilimanjaro** (Spain) describes its planned platform as multimodal and digital-analog.

1.2.3 Qubit operations

Using a quantum annealer works as described in Figure 10. The objective and constraints are formulated classically, often as a QUBO, converted to an equivalent Ising model, and minor-embedded onto the hardware graph. The programmed quantities are the qubit biases h_i, couplings J_{ij}, and any chain strengths used by the embedding.

The annealing process then takes place with controlled evolutions of A(s) and B(s) as described in the previous chart, with tuning the magnetic transverse field affecting the qubits chip. When s=1, the system proceeds with reading the qubits values +1 or -1.

D-Wave annealers use niobium superconducting flux qubits derived from rf-SQUID circuits. In the documented compound-compound Josephson-junction de-

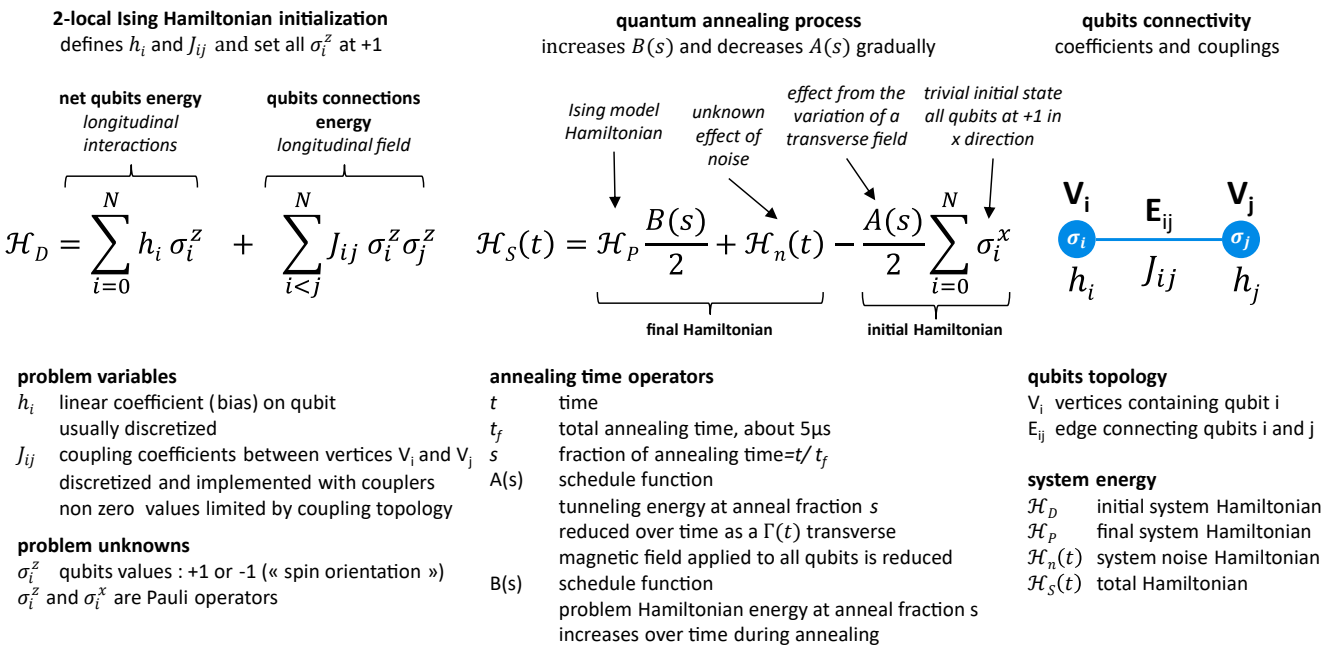

Figure 8: Uncovering a quantum annealing Hamiltonian. ⓒ Olivier Ezratty, 2022-September 2026.

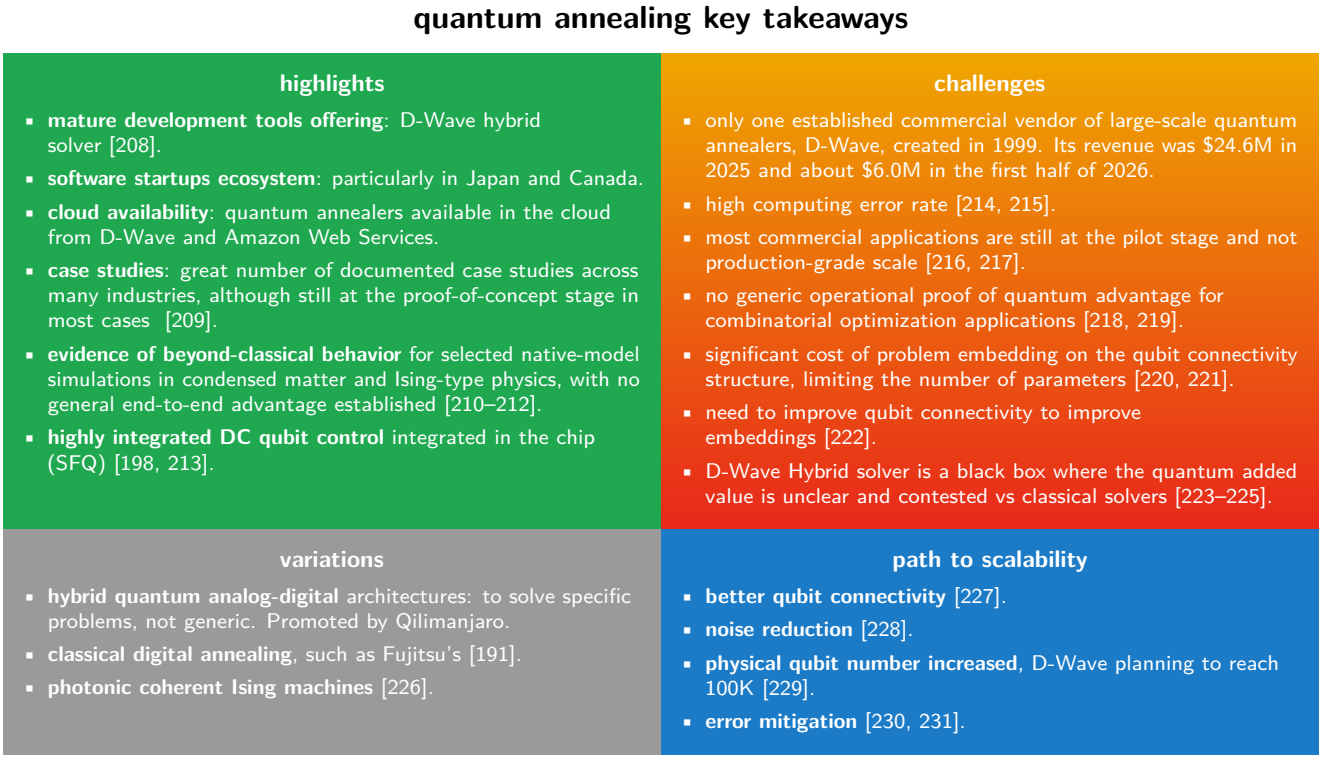

Figure 9: Quantum annealers highlights, challenges, variations and path to scalability. ⓒ Olivier Ezratty, 2021-2026.

sign, a main superconducting loop stores clockwise or counterclockwise persistent-current states, while compound Josephson-junction loops tune the tunneling energy and compensate fabrication asymmetries (Figure 11). An ideal rf-SQUID contains one Josephson junction, but D-Wave's practical qubit circuit contains several junctions.

Taking again the example of D-Wave annealers, we can dig into how the qubits are controlled to prepare and handle an annealing process [198, 213]. The process needs to control several parameters:

J_{ij} coupling between vertices V_i and V_j is controlled by DACs (digital to analog converters). These couplers are set with a static DC flux current applied to their compound-junction.

h_i energy between two states of qubits i is also controlled via a DAC. But other DACs

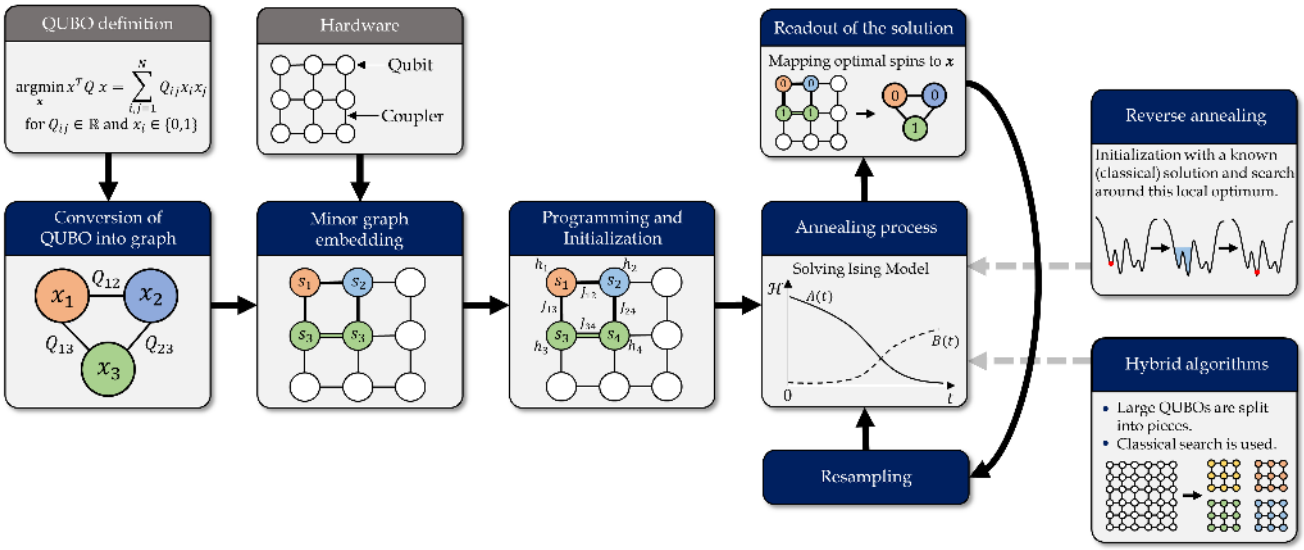

Figure 10: Quantum annealing computing workflow. Source: [209].

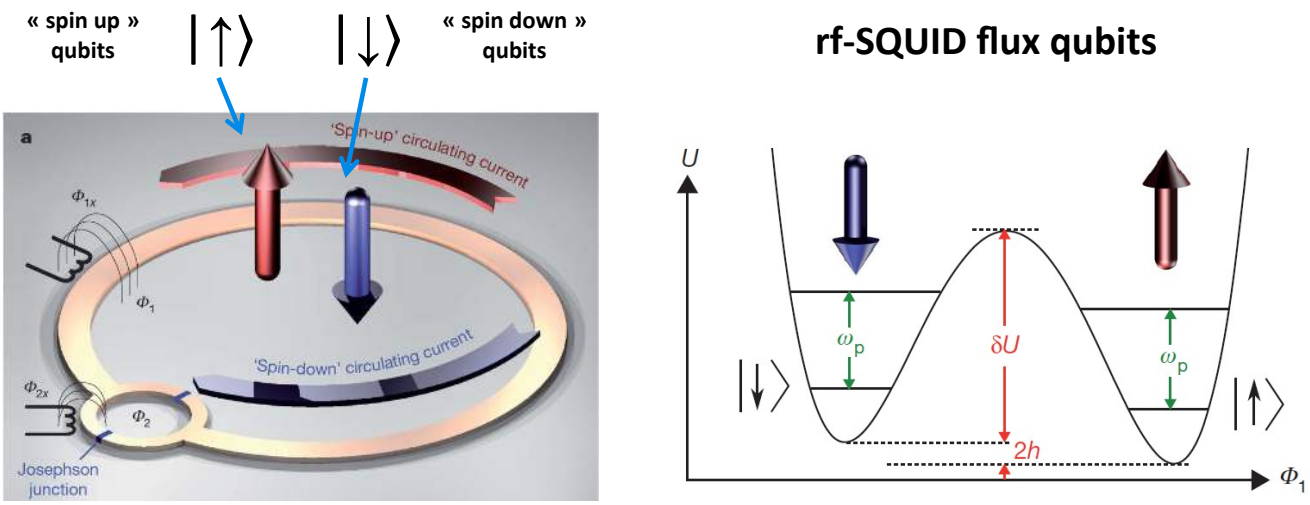

Figure 11: rf-SQUIDs used in a D-Wave quantum annealer. $\Phi_1 x$: flux bias on the outer superconducting loop which controls the energy difference « 2h » between two states, i.e. superconducting current direction. $\Phi_2 x$: flux bias on the inner superconducting loop with two Josephson junctions, controlling energy level δU enabling the switch between two spin directions. ω_p: energy variation for $|\uparrow\rangle$ and $|\downarrow\rangle$ states, δU: energy potential barrier between states. Φ_1: current phase difference before and after the Josephson junctions. for an isolated local-bias term $h_i s_i$, the two local-bias energies differ by $2|h_i|$, while interactions can change the effective energy difference. Source: D-Wave.

are there to correct the drift created by the annealing process.

A(s) transverse magnetic field applied to all qubits and controlled in the chip
by analog lines via the CCJJ DACs.

B(s) increases over time during annealing, also controlled by CCJJ analog lines in the chip.

The binary variables take values $s_i \in \{-1, +1\}$ in an Ising model or $x_i \in \{0, 1\}$ in a QUBO. By contrast, h_i and J_{ij} are programmable real coefficients. On Advantage systems, the documented linear-bias range is $[-4, 4]$. Advantage2 widened it to a nominal $[-6, 6]$, while the allowed coupling range remains a separate solver property. Values outside supported ranges are normally rescaled. The coefficients are submitted digitally but realized through analog flux biases with finite resolution and intrinsic control error. Early D-Wave control systems provided roughly 300 to 400 physical flux steps and targeted about four effective bits, or approximately 5% relative precision, in Hamiltonian parameters [198]. This is far below FP32 numerical precision and motivates calibration refinement and robustness studies [232].

For the D-Wave 2000Q generation, programming a problem took about 25 ms, a commonly used anneal lasted 20 μs and could be extended to 2 ms, and each readout took a few hundred microseconds. One thousand reads therefore required well below one second of QPU access time after programming, although end-to-end wall-clock time also included network, queueing, embedding, and post-processing overheads.

The static Hamiltonian parameters are loaded through multiplexed SFQ addressing into on-chip flux DACs. This replaces one room-temperature analog line per programmable element with a small set of digital address and power lines plus shared analog annealing lines. The tradeoff is serial programming time and substantial on-chip classical circuitry. The cited architecture does not establish an $O(N^{1/3})$ external-line scaling law [198].

This greatly simplifies the cabling of the cryogenic enclosure of the computer compared to the superconducting IBM and Google computers, as shown in Figure 12 of a 2000Q. Most of what can be seen in the intermediate stages in the cryostat corresponds to the dilution cryogenics system.

Annealers do not need to send microwave pulses to the qubits and thus avoid the related coaxial cables used in gate-based superconducting qubits.

Some of the magic comes from the integrated DC ramp pulses generation circuits that are built-in in the quantum chip.

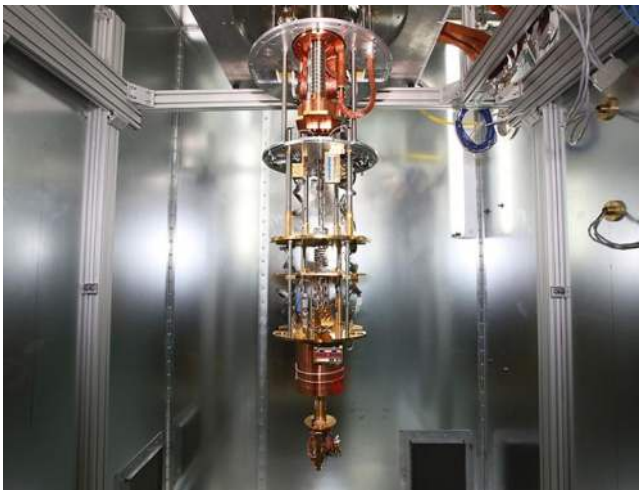

Figure 12: Inside a D-Wave system, with the cryostat open. Source: D-Wave.

These circuits use Josephson-junction SFQ demultiplexers to route individual flux quanta into persistent-current storage inductors. The stored flux is coupled to a target qubit or coupler and acts as a static analog DAC output. Josephson junctions are nonlinear superconducting circuit elements, not superconducting transistors. Control imperfections and device variability contribute to analog Hamiltonian errors [214, 233].

1.2.4 Research

Let's mention some research work beyond what D-Wave is doing.

IARPA launched its **Quantum-Enhanced Optimization** (QEO) program in 2017 to investigate whether high-coherence superconducting annealers could provide increasing performance enhancements on hard combinatorial-optimization problems. Its stated target was optimization, including machine learning, circuit-fault diagnosis, and scheduling, not the execution of Shor's factoring algorithm. DARPA's later **Quantum Annealing Feasibility Study** (QAFS) separately investigated the prospects for quantum enhancement using coherent superconducting annealing testbeds.

Stanford University and **NTT** demonstrated a 100-spin photonic coherent Ising machine in 2016 with a fully programmable 100×100 coupling matrix [234]. For an undirected Ising graph this corresponds to at most $100 \times 99/2 = 4{,}950$ independent pairwise couplings, although the paper describes 10,000 matrix entries. The adjective coherent refers to the phase-coherent optical parametric oscillator network, not to all-to-all connectivity. Peter McMahon, Tatsuhiro Onodera, and Edwin Ng later proposed an all-to-all superconducting Ising-machine architecture based on Josephson parametric oscillators and Floquet engineering [235]. MIT Lincoln Laboratory demonstrated coherent coupled capacitively shunted flux qubits in 2017 [236] and later investigated related two-dimensional superconducting-qubit arrays for analog simulation [237].

At last, the H2020 European project **AVaQus** (Annealing-based VAriational QUantum processorS) launched in October 2020 brings together five research laboratories (Institut de Física d'Altes Energies of Barcelona, Karlsruhe Institut für Technologie (KIT) of Karlsruhe, CNRS Institut Néel in France, the University of Glasgow and the Consejo Superior de Investigaciones Científicas in Madrid), associated with three startups **Delft Circuits** (The Netherlands), **Qilimanjaro** (Spain) and **HQS** (Germany). The project was scheduled to end in 2023 and got a funding of €3M, independently of the Quantum Flagship program.

1.2.5 Vendors

We'll of course start with D-Wave and then follow-on with Qilimanjaro and NEC.

D-Wave

Canada, 1999, $1.4B

D-Wave Quantum Inc. has been headquartered in Palo Alto since its 2022 listing on the New York Stock Exchange, while its historical engineering and fabrication operations remain in Burnaby, in the Vancouver area. For many years, D-Wave was the only commercial supplier of quantum annealing processors (Figure 14).

Company. D-Wave was founded in 1999 by Geordie Rose, Haig Farris, Bob Wiens, and Alexandre Zagoskin. Rose received his PhD in physics from the University of British Columbia in 2000, not in the mid-1990s. He met Farris during his studies while Farris was teaching a business and entrepreneurship course [238]. None of the four original founders remains in management. Eric Ladizinsky joined from Northrop Grumman in 2004 to lead the superconducting-processor effort and remains

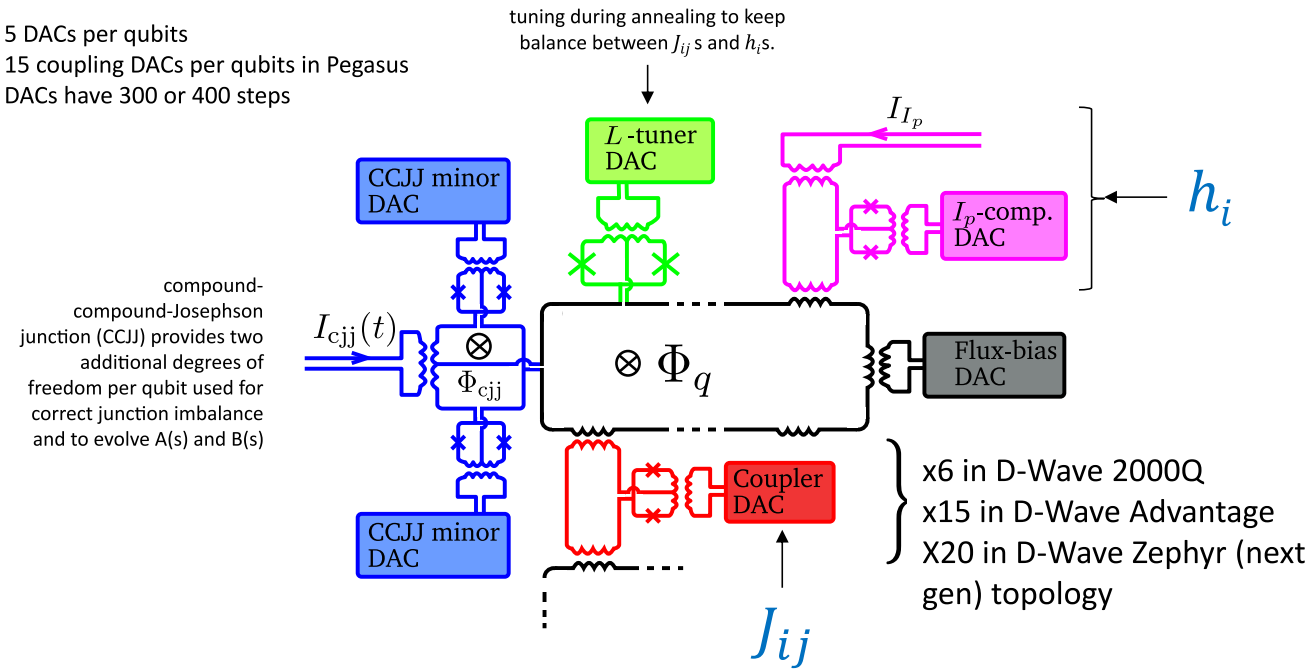

Figure 13: How D-Wave qubits are controlled at the physical level. Source: [198].

Chief Scientist, but he was not one of the four company founders. Alan Baratz joined D-Wave's executive team in 2017 and became CEO in 2020.

It took D-Wave about eight years to prototype its first four-qubit chip. The first D-Wave One was sold to Lockheed Martin in 2011, about 12 years after the company's creation, rather than in 2012. During these years, D-Wave raised about $31M, followed by a $1.2M investment in 2012 from In-Q-Tel, the US intelligence community's venture fund. The company later went public through a SPAC transaction completed in August 2022 [239] and subsequently arranged an equity line of credit with Lincoln Park Capital.

The investor forecast issued for D-Wave's 2022 SPAC transaction projected $551M of revenue in 2026. Actual revenue was $5.1M in 2020, $6.3M in 2021, $7.2M in 2022, about $8.8M in both 2023 and 2024, and $24.6M in 2025. The 2025 increase was strongly influenced by $12.6M recognized from a system sale to the Jülich Supercomputing Centre. The 2025 net loss of $355.1M included about $270.5M from noncash warrant-liability remeasurement, while adjusted net loss was $84.5M. Revenue was about $6.0M in the first half of 2026, comprising $2.9M in the first quarter and $3.1M in the second. Bookings were $33.4M in the first quarter and $2.1M in the second, for $35.5M in the first half. These figures make the old $551M forecast unattainable.

D-Wave acquired the Yale startup Quantum Circuits in January 2026 for $550M ($300M in stock and $250M in cash, closed on January 20, 2026) to develop its gate-model systems. They had been working internally on fluxonium qubits since about 2021. This acquisition is a technological shift to another superconducting qubit technology based on dual-rail qubits. We discuss it in 1.3.

Technology. D-Wave sells an end-to-end quantum-annealing platform. After prototypes developed from 2007 to 2009, its commercial life began with the 128-qubit D-Wave One, announced and sold to Lockheed Martin in 2011 [185]. The D-Wave 2000Q followed in 2017 with up to 2,048 qubits and about 128,000 Josephson junctions. Advantage launched in September 2020 with more than 5,000 qubits, roughly one million Josephson junctions, and Pegasus connectivity. Advantage2 was announced in 2021 and became generally available on May 20, 2025, with more than 4,400 qubits, over 40,000 couplers, and Zephyr connectivity [227, 228, 240]. D-Wave also introduced faster anneal schedules on compatible systems [241].

- **Qubit connectivity**. Higher native degree generally reduces minor-embedding overhead. Chimera, used in D-Wave 2000Q, has nominal degree 6. Pegasus, used in Advantage, has nominal degree 15. Zephyr, used in Advantage2, has nominal degree 20 Figure 15. These degrees can't be compared with gate-model QPU connectivity because annealers implement static programmable Ising couplings, while gate-model processors execute calibrated two-qubit gates and can use routing, tunable couplers, or modular links. The Chimera unit cell is a $K_{4,4}$ bipartite graph. Pegasus and Zephyr add internal and external couplers in more complex repeating structures [227].

  D-Wave's physical connectivity is fixed by the chip layout. User problems are minor-embedded into this hardware graph, often representing one logical variable by a ferromagnetic chain of physical qubits. This

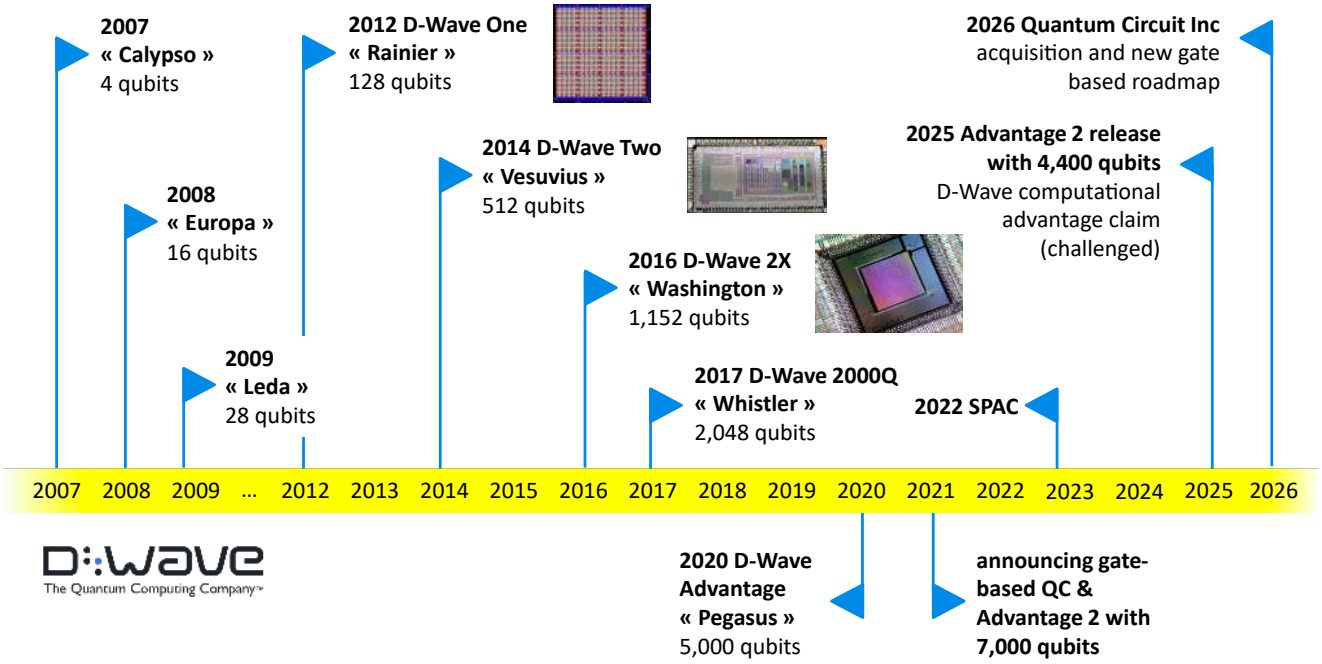

Figure 14: Timeline of D-Wave's history and products. The main recent news is the 2026 acquisition of Quantum Circuits Inc. and the switch from an internal fluxonium program to dual-rail qubits for D-Wave's gate-based approach. ⓒ Olivier Ezratty, 2022-2026.

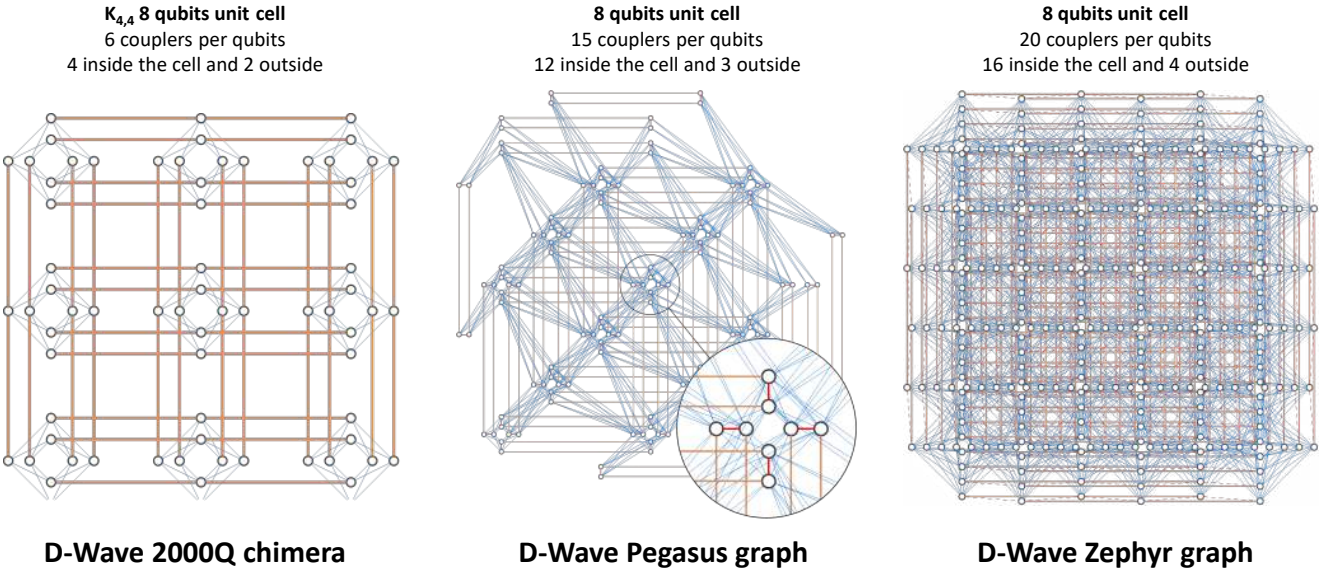

Figure 15: Evolution of D-Wave's qubit connectivity. Its comparatively high native degree reduces, but does not eliminate, the overhead of embedding dense logical graphs. Source: [217].

consumes qubits, reduces the effective energy scale, introduces chain-break errors, and adds classical compilation cost [220–222]. Zephyr reduces this overhead relative to Chimera and Pegasus, but does not remove it.

- **Qubit control**. D-Wave's superconducting annealers require fewer individually routed microwave lines than gate-based superconducting QPUs because static problem parameters are stored in on-chip flux DACs and the annealing schedule is distributed through shared analog controls. This simplifies cryogenic wiring but adds many Josephson junctions, calibration requirements, and serial programming operations on the processor. In July 2025, D-Wave announced a technology partnership with NASA JPL and Caltech to develop packaging for future annealing and gate-based chips using a superconducting bump-bond process.

- **Error mitigation**. Error sources include thermal excitations, decoherence, nonadiabatic transitions, intrinsic control error in h_i and J_{ij}, crosstalk, chain breaks, and readout errors [242, 243]. There is no single annealer "error rate" comparable to a gate infidelity. Percent-level coefficient errors are some-

times quoted, but their impact depends on the programmed energy scale, graph, chains, temperature, and solution gap [215, 244]. Mitigation methods include gauge transformations, chain-break decoding, anneal offsets, repetition, calibration refinement, energy penalties, and classical post-processing [230, 245, 246]. These methods improve sampling but do not constitute fault-tolerant quantum error correction.

A team of Italian quantum thermodynamics researchers explained in 2020 that the thermal noise from the annealing process could be used as a resource to enable faster and more reliable computations, involving the curious process of reverse annealing [247]. It can help finding a better solution than an existing solution already computed with a regular annealing process. In a 2024 experiment, they found a way to minimize the error rate of qubit initialization on a D-Wave Advantage with up to 5,612 qubits using their cooperative quantum information erasure (CQIE) protocol that leverages global quantum thermodynamics effects. However, given the way these flux qubits are controlled with direct current only, it is not clear how this initialization process could be implemented in a gate-based superconducting QPU [248]. Other error mitigation techniques were created in 2025 [231].

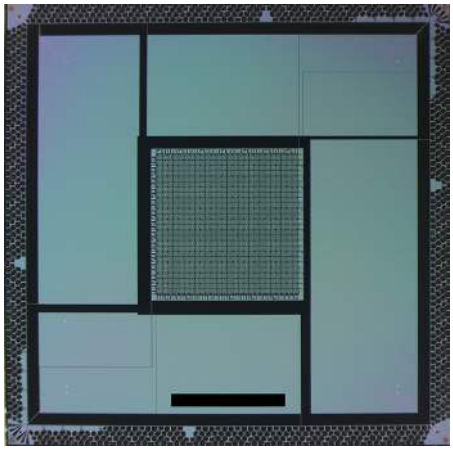

Figure 16: D-Wave Advantage2 1,200 qubits prototype chip. Source: [249].

- **Cryogenics**. D-Wave chips operate at 10 to 15 mK like all gate-based superconducting qubits. The cryostat is thus the same, using a dry dilution system. D-Wave publicly quotes a total system draw of about 12.5 kW, constant across five generations, which is the figure used in their energy-advantage messaging (Figure 17). The dilution cryogenics accounts for the large majority of it, the remainder going to the room-temperature control and classical computing systems outside the cryostat. The cryogenic part includes an enclosure with five layers of magnetic isolation.

Manufacturing. D-Wave's chips are manufactured in the USA in SkyWater Technology's fab in Bloomington, Minnesota, formerly operated by Cypress Semiconductor [250]. IonQ's 2026 acquisition of SkyWater changes the ownership of this supplier, but its consequences for D-Wave cannot be inferred without information about the foundry agreement.

We will now describe the scientific debates around D-Wave's annealers quantumness, actual quantum speedup, and quantum advantage.

Quantumness. D-Wave processors use quantum tunneling, superposition, and open-system many-body dynamics [251]. Experiments have detected entanglement in selected two- and eight-qubit subsystems during annealing [252], and later work observed coherent dynamics in chains of more than 2,000 qubits [253]. These results establish quantum behavior in specific regimes, but neither small-subsystem entanglement nor agreement with a coherent dynamical model proves a computational advantage for optimization.

Debates about the computational relevance of this quantumness concern whether coherence and multiqubit tunneling persist over the instance sizes and timescales that determine performance, and whether classical models can reproduce the output statistics [254]. Connectivity affects embedding overhead but is not itself a test of quantumness. A 2025 Jülich study compared Schrödinger, Lindblad, and classical Markov models and found a crossover toward dissipative classical dynamics as annealing time increased [255]. This is subtler than an absence of quantum behavior beyond a universal 5 ns threshold.

Universal adiabatic quantum computation and the circuit model are polynomially equivalent when sufficiently general local Hamiltonians and controls are available [256, 257]. This theorem does not imply that an arbitrary gate-model algorithm can be efficiently compiled to the stoquastic transverse-field Ising Hamiltonian and fixed sparse connectivity of a commercial D-Wave annealer. Specific circuit-to-adiabatic translations can require large qubit and coupling overheads. The factor of 32 reported in [258] belongs to one construction cannot be generalized.

Quantum advantage. D-Wave annealers can encode many NP-hard or NP-complete optimization and decision problems, including routing variants and the traveling salesperson problem. This does not mean that they solve arbitrary instances in polynomial time. The success probability may decrease exponentially, the minimum spectral gap may become exponentially small, and embedding and repetition costs must be included. No scalable polynomial-time algorithm for generic NP-complete problems has been demonstrated on a D-Wave system [259, 260]. The polynomial equivalence of ideal computational models does not supply such an algorithm [261]. Annealers can also be used as samplers in statistical applications [262].

John Preskill noted in 2017 that there was no convincing theoretical basis for a broad computational advantage

from the form of quantum annealing implemented by D-Wave [263]. This remains distinct from the universality of ideal adiabatic quantum computation. Depending on the oracle model and problem structure, theoretical speedups can range from none to quadratic or larger, but no general quadratic upper bound applies to every quantum-annealing problem [264].

In the good news realm:

- In general, D-Wave performs best when an Ising problem maps natively to the hardware, with a small "semantic gap" and little embedding overhead [212, 265]. A 2025 analysis of exact ground-state searches for three-dimensional Ising spin glasses compared a classical estimate $2^{N^{2/3}}$ with an empirical annealer fit $2^{N/\beta}$, where $\beta \approx 10^3$ over the accessible range [211]. This can favor the annealer at tested sizes, but N/β eventually grows faster than $N^{2/3}$. The fit therefore does not establish an asymptotic quantum speedup.
- In 2025, a paper described molecular ground-state estimation with D-Wave annealers for a small water-molecule active space [266]. This is an electronic-structure calculation mapped to an Ising optimization problem, not a condensed-matter simulation at 0 K. Its small scale and encoding overhead prevent it from establishing an industrially relevant quantum advantage.
- Quantum annealing outperformed one gate-based QAOA implementation on IBM's 127-qubit processor in a 2023 benchmark [267]. This compares two present-day implementations, not the asymptotic algorithms. A 2023 French study reported competitive MaxCut results on a quantum annealer [268], and a Bulgarian study examined Set Cover [269]. Neither result by itself proves a scalable quantum advantage over the best classical solvers.
- Researchers from the University of Alberta (Canada) found in 2026 that D-Wave annealers could generate some quantum advantage for solving QUBO-formulated optimization problems when its energy landscapes exhibit high gradient variance [270]. It was confirmed in another survey [271].
- Researchers from CSIRO (Australia) applied an error-mitigation technique to weighted MaxCut instances and reported favorable time-to-solution and solution-quality results against native D-Wave BQM, simulated annealing, and tabu search on the tested cases [272]. Negative edge weights are not intrinsically harder merely because their magnitude is more negative. Difficulty depends on the complete signed graph, frustration, weight distribution, degeneracy, and solver. The benchmark does not demonstrate quantum advantage because the classical comparison was limited, used a single CPU thread, and omitted embedding time.

In the bad news domain:

- A classical Tabu search solution was faring better in 2022 than quantum annealing [224].
- A benchmark done in Japan in 2023 on a D-Wave 2000Q against several state-of-the-art classical optimization algorithms designed for continuous-variable problems found that the D-Wave 2000Q matches classical algorithms only in a limited domain of computation time. It was tested on the D-Wave Advantage and its results were worse than with the 2000Q [273].
- A test of the Zephyr Advantage2 prototype chip was done and didn't detect a quantum advantage with optimization problems [274].
- Other studies in the Netherlands, Norway, Belgium, and the USA found no generic advantage for the tested combinatorial-optimization workloads and, in some settings, no evidence even for a quadratic speedup [218, 219, 275]. These results do not prove that every possible annealing algorithm lacks an advantage. New optimization proposals continue to be developed, including for MaxCut [276].
- In June 2024, Q-CTRL released a benchmark to prove that a 127-qubit IBM QPU equipped with their quantum error suppression and mitigation tools could outperform a D-Wave annealer to solve some non-trivial optimization problems [277]. D-Wave responded sharply, pointing out some methodological errors in the comparison [278, 279]. And Q-CTRL responded again. Whatever, in both cases, the compared implementations were not operating at all in a quantum advantage regime.
- In March 2025, D-Wave scientists published a Science paper claiming beyond-classical quantum simulation of quench dynamics in two-, three-, and infinite-dimensional spin glasses [210]. The claim was relative to the classical methods and accuracy targets examined in the original study, not a proof that the model could not be solved classically. Researchers from the Flatiron Institute subsequently obtained comparable results with lattice-specific tensor networks, work published in Science in May 2026 [280], while an EPFL group proposed another tensor-network approach [281]. D-Wave argued that these classical approaches faced scaling or accuracy limitations [282–284]. A July 2026 comment also reported neural-quantum-state simulations [285]. The episode illustrates why a beyond-classical claim must specify observables, error tolerance, classical compute budget, and scaling regime.
- Daniel Lidar's team reported in 2025 that quantum annealing correction (QAC) produced evidence of an advantage on selected combinatorial-optimization instances [286]. Subsequent studies challenged the exact-solution criterion [287] and the runtime comparison [288]. The disagreement again depends on the success metric, classical baseline, and accounting of preprocessing and repetitions.

- A French team reported in 2026 that classical simulated annealing (SA) was more efficient, more accurate, and simpler to implement than the tested quantum-annealing approaches for graph-cut instances. Its first paper compared a D-Wave QPU, conventional SA, and D-Wave's hybrid solver, including embedding and post-processing costs [223]. SA produced cut values about 10 to 15% better on the reported instances. The hybrid solver sometimes achieved a lower encoded QUBO energy without a better feasible graph solution, illustrating how penalties and embedding can separate mathematical energy from application quality. Classical decomposition let the hybrid solver process instances too large for a direct QPU embedding, but did not make it outperform SA in solution quality. Preprocessing and post-processing accounted for roughly one third of the reported computation time.

  A second paper studied the Minimum Edge Multiway Cut problem, which removes the fewest edges needed to separate k terminals [225]. Its assignment encoding requires multiple binary variables per vertex, increasing logical-variable and physical-qubit demand. The hybrid solver found valid solutions on instances where direct QPU execution failed, but SA again produced better cuts. An earlier 2025 study by the same group reported evidence of an advantage in finding exact solutions under a different benchmark design [289]. These results are not directly contradictory because they use different instances, success criteria, and solver configurations.

D-Wave also claims an energy advantage for selected annealing workloads Figure 17. Such a comparison must multiply the complete system power by time-to-solution and include programming, readout, repetitions, embedding, post-processing, networking, and any classical part of a hybrid solver. A nearly fixed QPU-system power alone is not evidence of a quantum energy advantage.

Software tools. Ocean is D-Wave's open-source Python software stack for formulating, embedding, submitting, and post-processing optimization and sampling problems. It is available through D-Wave's GitHub repositories and integrates with the Leap cloud service, while D-Wave hardware is also accessible through Amazon Braket. Ocean includes a problem inspector that visualizes minor embeddings and chain behavior on the hardware graph [290].

D-Wave introduced a Constrained Quadratic Model (CQM) hybrid solver in October 2021. CQM supports binary, integer, and real variables with explicit constraints. This differs from a Binary Quadratic Model (BQM), whose variables are binary or spin-valued, and a Discrete Quadratic Model (DQM), whose variables select from finite cases. Published capacity limits refer to particular versions of cloud hybrid solvers, not to the number of variables directly embedded on a QPU [208, 291]. The hybrid solvers combine classical decomposition with annealer calls, but their proprietary orchestration makes it difficult to attribute performance gains to either component [292].

Figure 17: D-Wave CEO presenting the company's claimed energy advantage for quantum annealers in 2025. Source.

D-Wave has also promoted quantum-assisted generative-AI workflows based on Restricted Boltzmann Machines (RBMs) and GPU integration in Leap [293, 294]. A 2025 study found only modest statistical differences between D-Wave sampling and classical Markov chain Monte Carlo for the tested RBMs [295].

In 2025, D-Wave launched its Launchpad Program, aimed at attracting developers on their platform. It provides free trial access to D-Wave hardware and software, to create solutions [296].

D-Wave is partnering with many independent software vendors, particularly in Japan, and with Zapata AI (until it disappeared in 2024), Multiverse and Kipu Quantum.

Roadmaps. In their Clarity roadmap announced in October 2021, D-Wave planned to support 7,000 qubits to be released by 2024. A first intermediate 500-qubit prototype was delivered in June 2022 and another one, of 1,200 qubits, in April 2024 (Figure 16). A final version of Advantage2 with 4,400+ qubits and 40,000+ couplers was produced in May 2024, calibrated in November 2024, and integrated in a commercial system whose general availability was announced on May 20, 2025. We can suppose that its increased connectivity has a cost in the "real estate" (surface) of the chip, explaining why they had to decrease the number of qubits vs their initial plans and vs the Advantage Pegasus. In a 2025 white paper [228], D-Wave explained how their Advantage 2 improved compared to the 2020 Advantage annealer. It has 40% higher energy scales which creates a greater energy separation between high-quality solutions and lower quality ones, creating more optimal results. It also accelerates quantum dynamics in the annealer. It doubles coherence time which improves the effectiveness of quantum annealing to solve more complicated problems. At last, noise is reduced by 75%, so by a factor of 4, which improves the quality of the solutions. Also, its better qubit connectivity improves problems embedding capabilities.

In March 2025, D-Wave updated its roadmap with a long-term target of a 100,000-qubit annealer based on

a multichip architecture [229]. In 2026, it associated this target with a future Advantage3 generation. As of August 2026, D-Wave had not publicly specified the interconnect, yield, calibration, thermal, or embedding architecture needed to reach this scale. In 2026, D-Wave also updated its gate-based roadmap through the acquisition of Quantum Circuits Inc. We discuss it in the superconducting subsection of this part (1.3).

Applications. One of the oldest and most famous D-Wave publicized "case study" came from Google and NASA in 2015. They were using a D-Wave 2X, the 2015 generation with 1,097 usable qubits, on a weak-strong cluster instance built to favor finite-range tunneling. Google announced that, on that particular case study, D-Wave's annealer was 100 million times faster than an Intel Xeon server processor core [297]. This is what drove my own interest in quantum computing!

Like many such claims, it was questionable since based on a single optimized algorithm, here, a Quantum Monte Carlo simulating quantum tunneling on a classical computer. Critics abounded about this performance [298]. It was a first of a kind "hype" moment for quantum computing (Figure 18).

D-Wave communicates regularly on many other "proof of concept" references. At some point, its web site referenced over 250 "case studies", the largest number of any quantum computing vendor [209]. But they are now harder to find and are generally poorly documented.

Quantum annealers are commercially accessible and supported by a mature software ecosystem, but most published case studies remain small proofs of concept. A few hybrid applications have been described as production deployments. None has yet provided an independently validated, end-to-end quantum advantage over the best classical alternative [216, 217].

The following examples begin with the automotive and transportation sectors.

- **Volkswagen** simulated the operation of a 418-cab fleet in Beijing in 2017 using a hybrid classical and quantum-annealing algorithm trained on data from 10,357 cabs [303]. In November 2019, Volkswagen, HERE, and Volkswagen Data:Lab used a related approach to optimize shuttle-bus routes for the Web Summit in Lisbon, covering 185 trips with nine buses over four days [304]. Neither demonstration established a quantum advantage.
- **Denso**, a Japanese car equipment manufacturer presented at CES 2017 in Las Vegas a system for optimizing a fleet of Toyota delivery vehicles. Toyota and Denso also crafted a solution to find the optimal location of electrical components and conductor paths in electric circuit systems [305].
- **Volkswagen** experimented quantum annealing to optimize its car paint-shop processing in order to minimize color switching, but with no clear quantum advantage [306], and also a solution to develop new batteries [307]. These batteries are not there yet.
- **Lockheed-Martin** produced in 2014 some validation procedures for its embedded software in 6 weeks instead of 8 months with a D-Wave and its QVTRace tool [308].
- **SavantX** developed a port operations optimization prototype for the Port of Los Angeles. It is supposed to be a deployed solution but it is hard to verify.
- **Ford Otosan** and D-Wave announced in 2025 the deployment of a hybrid-quantum application in production to improve vehicle production sequencing [309]. It is said to reduce the scheduling time of 1,000 vehicles per run from 30 minutes to less than five. Who knows whether this comes from the classical part of D-Wave's hybrid solver or from the annealing part!
- Researchers in Poland, Hungary, Brazil and the USA found in 2021 a way to use D-Wave annealers to **optimize trains dispatching** on single-railways lines [310].
- Researchers in Slovakia developed in 2025 a TFO (traffic flow optimization) application for 25,000 vehicles that reached results nearing the optimization from classical Gurobi-based solutions [311].
- Researchers in South Korea found good results for solving maritime routing problems [312].

In retail operations:

- **Ocado**, a British retailer, prototyped some optimization solution for its robots-based warehouse operations.
- **Pattison Food Group** is working on grocery operations optimization.

In financial services:

- **Mastercard** works on customer loyalty and rewards allocation, cross-border settlement, and fraud management. The partnership with D-Wave started in 2022.
- Scientists in Germany in the US proposed in 2025 a QUBO-based solution to cluster financial assets with an exhibited qualitative advantage [313].
- In 2025, D-Wave proposed to use its quantum annealers to run a custom-made Blockchain proof of work, providing an energy advantage vs classical methods [314]. It was prototyped on 4 annealers. The practicality of such solution is of course questionable.
- A 2026 audit of D-Wave's hybrid portfolio-optimization service on cardinality-constrained mean-variance-turnover instances demonstrated the absence of quantum-advantage for this problem class vs Gurobi and Tabu Search [315].

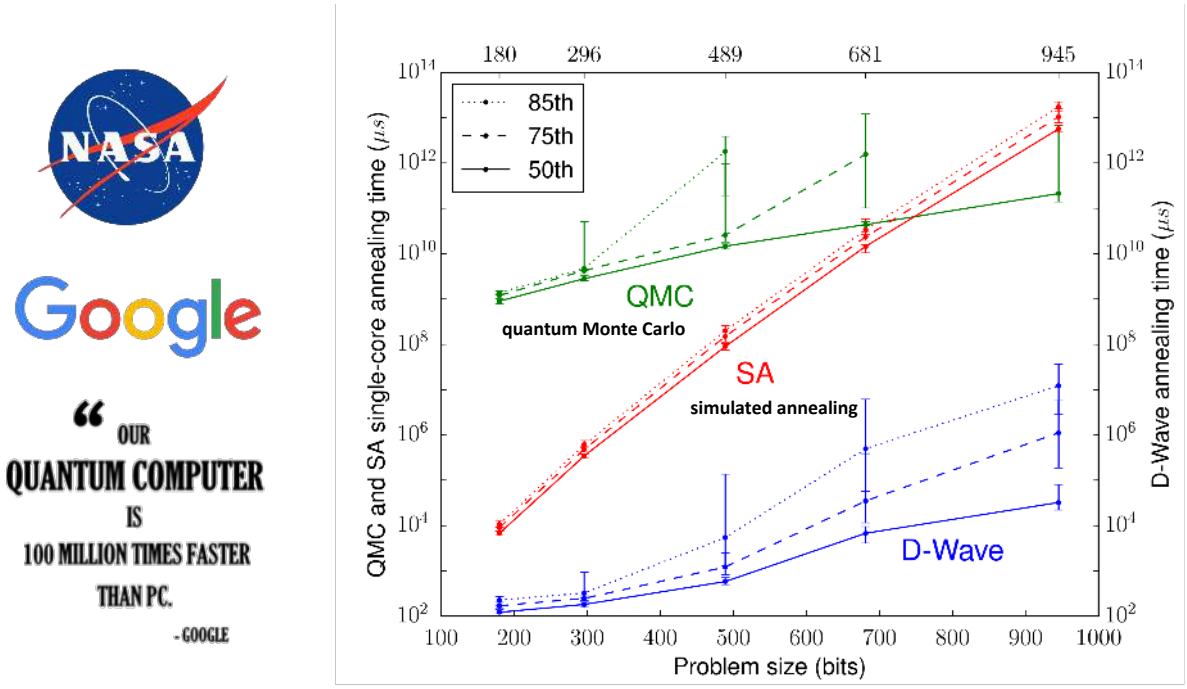

Figure 18: How Google and NASA communicated in 2015 about the performance of a D-Wave annealer vs simple personal computers. The benchmark used specially constructed Ising instances closely matched to the 1152-qubit D-Wave 2X hardware graph, in a finite-range tunneling task aimed at finding the ground state of an Ising graph. It did not establish a general end-to-end advantage. The comparison was made with classical simulated annealing running on a single core. Since then, this performance has been revisited, and such a 2D instance can be solved faster on a single GPU using classical tensor networks [299–302]. Source: [297]. Caption revisited in 2026.

In telecommunications:

- NTT Docomo plans to put in production a quantum annealing-based application that optimizes mobile network performance and reduces network congestion [316].

In life sciences:

- **Biogen**, **1QBit**, and **Accenture** reportedly prototyped a molecular-comparison workflow for drug repurposing. D-Wave's work with **Menten AI** concerns computational protein design and is a separate case study.
- In April 2020, D-Wave opened free access to its cloud systems to researchers investigating the **COVID-19 pandemic** [317]. Projects included patient routing, epidemic modeling, nurse scheduling, mutation analysis, and molecular screening. None established a quantum advantage for these applications.
- In 2022, a study showcased some potential benefits in molecular docking [318].
- Another one published in 2023 in South Korea was about X-ray image segmentation [319].
- A South Korean team used functional near-infrared spectroscopy (fNIRS) measurements of prefrontal activity to study cognitive performance and academic achievement. Its quantum-annealing pipeline improved selected metrics relative to the classical methods tested, but the study did not establish a scalable quantum advantage [320].
- **Pfizer** created a proof of concept to optimize production planning at their Healthcare Hub in Freiburg, Germany, in collaboration with QuantumBasel. The results are “promising” but not documented [321].
- **Kipu Quantum** created in 2025 two tests using 200+ qubits for a molecular toxicity classification and 111+ qubits for predicting myocardial infarction complications, which improved classification accuracy against classical machine learning techniques [322, 323].

In marketing:

- **Recruit Group** has used D-Wave's CQM hybrid solver to schedule television advertisements with the objective of improving campaign yield [324].
- **Interpublic Group** develops optimization tools for marketing campaigns.

In various other industry domains:

- **Aramco** and its research center in Delft, the Netherlands, have investigated D-Wave annealers for optimization problems related to seismic imaging.

- **GE Research** experimented a hybrid maintenance resource allocation optimization application. The company has a team of over 80 people working on quantum technologies.
- **KAIST** and **LG U+** in Korea optimized some data-transfer routing for a fleet of low-earth orbit telecommunications satellites using a QUBO algorithm, with the help of **Qunova Computing**, a South Korean quantum software startup [325].
- **BASF** compared the performance of the classical Gurobi optimization algorithm with quantum annealing (D-Wave) and digital annealing (Fujitsu) versions to solve a transport robot scheduling problem [326]. At this point, Gurobi fares better, particularly with large data sets.
- Potential **emergency-management** applications include tsunami-response planning at **Tohoku University** [327, 328] and last-mile military resupply explored by the Australian Army and NEC Australia [329]. Osaka University also tested nurse scheduling on a D-Wave 2000Q [330]. These demonstrations showed feasibility on selected instances, but did not establish a large-scale end-to-end quantum advantage.
- In 2024, a Franco-Belgian team from IÉSEG and Junia mapped small and medium **Resource-Constrained Project Scheduling Problems** (RCPSPs) from mixed-integer linear programs to QUBOs and evaluated them on D-Wave Advantage using time-to-target and Eviden Q-score metrics [331]. An RCPSP schedules tasks subject to precedence and resource constraints while minimizing project duration. The reported experiments did not establish a quantum advantage and remained at modest scale. The authors estimated that larger instances could require about 35,000 physical qubits. This exceeds current single-QPU capacity, although it is below D-Wave's unverified long-term 100,000-qubit roadmap target.
- An interesting comparison was made by researchers in Germany in 2024 for solving optimization problems with gate-based QPUs, quantum annealers and an atom-based analog QPU from QuEra. The benchmark seems to show that quantum annealing had greater capabilities than both the analog and gate-based QPU [332].
- A greenhouse control QUBO benchmark in 2026 done in Karlsruhe found that D-Wave Leap Hybrid BQM workflow is less reliable and does not beat classical baselines. The annealer can't yet help for this agricultural or HVAC-style control problem [333].
- **Staque Computing**, an AI, blockchain and quantum computing service company announced in 2025 the creation of a commercial hybrid-quantum application that simulates and optimizes the routing of autonomous agriculture vehicles at scale [334].

In government security:

- **Los Alamos National Laboratory** and **Stanford University** prototyped a graph-analysis method for identifying anomalous structural patterns in conflict-related social-network data from Syria [335]. The method infers patterns in a data model rather than directly detecting the formation of terrorist networks.

In fundamental research, where the most credible quantum advantages could be found so far:

- **NASA** experimented D-Wave annealers in its joint QUAIL lab with Google in various fields, including the detection of exoplanets by analysis of telescopic observations using the transit method, as well as for various optimization and planning problems [336, 337].
- Polymer simulations were achieved in 2023 by a team of researchers in Italy with a seemingly quantum advantage [338].
- A transverse field Ising model magnetization dynamic was implemented on a D-Wave annealer, reproducing the IBM 2023 kicked Ising model experiment (using 127 superconducting qubits) [339].
- Several spin glass simulations have been conducted on D-Wave annealers with a potential quantum advantage [340, 341]. A new version was even positioned as a "quantum supremacy" in March 2024 [342]. In 2024 again, a team including Nobel laureate Giorgio Parisi conducted a classical simulation of a phase transition of Ising spin glass model quantum annealing in two large Nvidia GPU supercomputer configurations. They found out that with some symmetry restrictions, it could be potentially possible to run it efficiently on a quantum annealer [343]. Other such experiments extend this to frustrated Ising models supporting more interactions [344].
- In 2021, a D-Wave-led study reported a computational advantage exceeding three million for a specific quantum-magnetism simulation relative to the classical path-integral Monte Carlo baseline used in the paper [345]. The ratio is algorithm-, observable-, accuracy-, and hardware-dependent.
- Quantum field theory analog simulations were done in 2025 to observe in real time the nucleation of quantized true-vacuum bubbles in a 1D ferromagnetic transverse-field Ising chain [346]. The problem was embedded natively as the hardware Ising Hamiltonian on the Pegasus topology and run as an analog quench. In [347], the same group extended the work to two dimensions, realizing a 2D quantum Ising model whose spin-polarized metastable state encodes a false vacuum. The advantage claim is about simulation reach, the 2D geometry with 4000+ coupled spins over these dynamical timescales being difficult classically.

- A Los Alamos and D-Wave team studied in 2026 the piled-up dominoes model interpolating between the 2D ferromagnetic Ising model and Villain's fully frustrated odd model [348]. The annealer samples thermal distributions near criticality without the critical slowing down that plagues classical Monte Carlo.
- A 2022 experiment used more than 2,000 qubits in one-dimensional Ising chains and found dynamics consistent with coherent quantum annealing across a phase transition [253]. This is strong evidence of large-scale coherent dynamics in that fast-anneal regime, but it is not a direct certification of real 2,000-qubit entanglement or of optimization advantage.

We can also mention some other generic quantum annealing solutions:

- **Sorting lists** and building search trees or heaps, which can be modeled as QUBO problems [349].
- **Classical HPC load balancing** optimization [350].
- **Machine learning** basic tasks like feature selection and clustering [351].
- **Neural-network training** using binary encodings of trainable parameters, polynomial approximations of activation functions, and reduction of higher-order binary polynomials to quadratic form [352, 353].
- **Physical simulations** of topological matter and phase change [354] and neutrino oscillations [355].
- **Decomposed quantum annealing** partitions a problem graph into smaller subproblems, as in DBK approaches to Maximum Clique [356]. Demonstrations have included graphs with 120 vertices and 6,395 edges [357, 358]. The subproblems can be executed separately on D-Wave Advantage, but this is not automatically equivalent to coherent parallel execution across several QPUs. More general distributed annealing architectures remain a research topic [359].

And some variants of processes to implement on D-Wave annealers:

- **Shortcuts to adiabaticity** (STA) are control protocols designed to reproduce the target of slow adiabatic evolution in a shorter time. A familiar sufficient-condition estimate scales as the inverse square of the minimum spectral gap, but the exact bound also depends on Hamiltonian derivatives, boundary conditions, and the chosen theorem. Counterdiabatic driving adds terms that suppress unwanted transitions, while diabatic quantum annealing deliberately populates excited states and later transfers amplitude back toward the ground state. These related strategies are not synonymous, and both can require controls unavailable on current annealers [360].
- **Inhomogeneous quantum annealing** (IQA), in which transverse fields are turned off one by one rather than simultaneously, can avoid the first-order phase transitions that impede conventional quantum annealing. But the implementation is challenging [361].
- **2-SAT combinatorial optimization** problems solving with four known solutions with standard annealing and reverse annealing [362].
- **Classical-quantum transfer learning**, where parameters are trained classically, and the trained parameters are used in the solver with quantum annealing. The trainable quantum COP solver using classical-quantum transfer learning improves convergence speed and execution time over the original solver [363].
- **Quantum annealing eigensolver** (QAE), a QUBO-based approach to molecular eigenvalue estimation that was tested on H_4 [364]. The reported $N^8 \log_2^2 N$ and N^8 costs depend on the encoding, basis, precision, optimizer, and measurement model.
- **Branch-Price-and-Cut for vehicle routing**, for which the projected speedup depends on future annealers with greater capacity and unspecified performance characteristics [365].
- **Nonlinear-Program Hybrid Solver** to solve the Traveling Salesman Problem, the Knapsack Problem, and the Maximum Cut Problem [366].

Customers. D-Wave has installed systems at a small number of customer sites and provides broader remote access through its Leap service and Amazon Braket. Publicly identified installations have included the Google/NASA/USRA QUAIL program, Lockheed Martin and the University of Southern California, Los Alamos, the Jülich Supercomputing Centre, and Florida Atlantic University. Ownership, hosting, and cloud access are not equivalent to system sales. Jülich began cloud access in 2021 and announced acquisition of an Advantage2 system in 2025 [367]. Pharmaceutical users such as Shionogi have accessed annealers through Leap for hybrid molecular-design studies [368].

Los Alamos National Laboratory ordered a D-Wave system in September 2019 and has used it in subsequent studies [275, 369]. In January 2022, the first D-Wave Advantage system in Europe was deployed at the Jülich Supercomputing Centre near Cologne. It was integrated with classical HPC through the Jülich Unified Infrastructure for Quantum Computing (JUNIQ). The Jülich team and other German researchers have since published several algorithm benchmarks [370, 371].

In June 2024, D-Wave announced the upcoming deployment of a D-Wave Advantage 2 QPU at New Davidson Technologies, a contractor for the US DoD, in Alabama [372]. The QPU assembly was completed in April 2025, with several weeks remaining for calibration. D-Wave

and Davidson are working with the US defense contractor Anduril for the creation of some quantum-classical hybrid applications for US air and missile defense planning. In 2026, D-Wave announced a partnership with AT&T with plans to use their annealers for network optimization [373].

In summary, quantum annealing may be a technique contested by many specialists, but it has the merit of existing and being testable in many use cases [374].

Qilimanjaro

Spain, 2019

Qilimanjaro is a startup based in Barcelona created around three physicists coming from different Spanish institutions (Barcelona Supercomputing Center, IFAE, University of Barcelona), joined by two cofounders on the business and finance side, with a staff of 50 as of June 2024.

Company. The founding team assembles Jose Ignacio Latorre (Chief Science Officer, also now the Director of CQT in Singapore, went through MIT, CERN and Niels Bohr Institute), Pol Forn-Díaz (Chief Hardware Architect, TU Delft, MIT, Caltech and IQC Waterloo), Artur Garcia Sáez (Chief Software Architect, ICFO, Stony Brook), Víctor Canivell (Chief Business Officer) and Jordi Blasco (Chief Financial & Legal Officer). They initially wanted to launch an ICO (initial coin offering) to fund the company when it was trendy but abandoned it.

Technology. Qilimanjaro develops a quantum annealer based on superconducting flux qubits. Its claimed differentiation is improved coherence, coupling design, and connectivity. Initial devices use room-temperature classical control electronics, with cryogenic control on a separate chip described as a later objective. The company labels its combination of analog and gate-based operation "multimodal" and continues to publish research on flux-qubit coupling [375]. Its offering is organized around quantum application-specific integrated circuits (QASICs), although public hardware specifications remain limited.

Qilimanjaro also benefited from European funding through the project **AVAQUS**. This project coordinator is Pol Forn-Díaz, head of the IFAE Quantum Computing Technologies group on top of his role in Qilimanjaro. It involved the superconducting team from Nicolas Roch at Institut Néel in Grenoble who designs the microwave amplifiers used in flux qubits readouts and is also a cofounder of the TWPA startup Silent Waves.

Manufacturing. They relied initially on two fabs for their qubit designs, the one from IFAE and the one from the Institute of Microelectronics of Barcelona (IMB-CNM). They got their first qubit chips from QuantWare (The Netherlands) and even defined an annealing architecture to solve Ising models using the typical nearest neighbor connectivity of superconducting qubits [376]. Their last prototype as of 2026 had 15 physical qubits.

Software. Qilimanjaro is a principal contributor to **Qibo**, an open-source full-stack framework for quantum simulation and hardware execution, not merely a cloud operating service. **Qibolab** extends it with a hardware-control layer for laboratory instruments and qubit calibration [377, 378]. In October 2025, Qilimanjaro released QiliSDK for digital, analog, and hybrid workflows on its SpeQtrum platform. Public specifications of the QPUs exposed by that service remain limited. In January 2025, the company introduced EduQit, an educational superconducting quantum computing system using a compact Bluefors cryostat and Qblox controls.

In 2026, Qilimanjaro published a white paper comparing the time and energy of analog and gate-based superconducting simulations of Hamiltonian dynamics [379]. Using two systems drawing about 19 kW each, but different execution times and shot counts, it reported energy ratios favorable to analog execution by factors ranging from roughly 1 to 90. This is not yet an accuracy-matched quantum energy advantage because analog and digital simulations accumulate different errors. A 2026 analysis by Jens Eisert and colleagues shows that accounting for stability under noise can substantially narrow the comparison [380].

Customers. In 2025, Qilimanjaro received an €8.5M procurement contract for MareNostrum-Ona, described as the first quantum annealer designed and built in Europe. It was integrated with Spain's MareNostrum 5 supercomputer and inaugurated in May 2026. The first commercial annealer deployed in Europe was nevertheless the D-Wave Advantage installed at Jülich in January 2022. MareNostrum-Ona started with about 10 qubits and is planned to exceed 30 qubits. It was jointly funded by the EuroHPC JU and the EuroQCS-Spain Consortium, which includes the Barcelona Supercomputing Center, IFAE, and INL.

The company started working with CMA CGM on quantum-inspired optimization algorithms. It later partnered with Abu Dhabi's Technology Innovation Institute to help establish the Quantum Research Centre, build expertise, and provide access to its technology. José Ignacio Latorre subsequently became TII's Chief Researcher. Public information is insufficient to determine the present scope of that partnership, while TII has also announced work with other quantum vendors.

NEC

Japan, 2018-2026

NEC researched coherent Ising and quantum-annealing architectures based on superconducting parametric oscillators, while also developing classical simulated-annealing software for its SX-Aurora TSUBASA vector platform. Earlier roadmaps discussed highly connected

systems, but no comparable commercial quantum annealer had been publicly delivered by 2025.

In June 2023, NEC announced a partnership with Tohoku University on an 8-qubit quantum annealing QPU that was developed using superconducting technology in association with the ParityQC LHZ counter-diabatic architecture. The available evidence does not establish scalability or quantum advantage for this device.

In September 2026, NEC announced it was discontinuing its quantum computing hardware effort, explaining that the return on investment was too long in the future.

1.2.6 Bibliography and notes

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This **Quantum annealing** subsection contains 201 bibliographical references and notes containing at least 4,045 pages.

1.3 Superconducting qubits

Following the part on quantum and classical annealing, let's move on to gate-based superconducting qubits quantum computers. From a physical point of view, D-Wave's quantum annealers and gate-based superconducting qubits QPUs have in common their Josephson junctions and low temperature operations but their qubit physics, overall architectures, control signals and programming models are very different.

Superconducting qubits are the dominant solid-state gate-based modality, used by IBM, Google, Rigetti, AWS, IQM, OQC, Fujitsu/RIKEN and other vendors. Qubit count alone is no longer a useful record metric: current systems span from about one hundred to several hundred physical qubits, including Google's 105-qubit Willow, IBM's 156-qubit Heron family and the 256-qubit Fujitsu/RIKEN system announced in 2025. Their computational value depends much more strongly on gate and readout errors, connectivity, leakage, stability, calibration and executable circuit depth than on raw qubit count.

Most commercially accessible superconducting systems remain noisy physical-qubit processors. Some platforms now execute useful experiments with many tens or more than one hundred qubits, while recent QEC experiments have crossed important milestones such as below-threshold surface-code memories.

The short term workaround of low fidelity is a mix of quantum error mitigation techniques in association with adapted quantum algorithms. Longer term workarounds are quantum error correction and qubits number scalability. It creates problems that are not yet solved with regards to fidelity stabilization with a growing number of qubits, solving the qubits cabling maze with cryogenic electronics or signals multiplexing and scaling cryostats cooling power.

The Josephson junction used in these qubits is a thin nanometric insulating barrier between two superconducting metals, creating a tunnel junction. It creates a quantum electrical component with a single degree of freedom, the superconducting phase difference between its electrodes, conjugate to the number of Cooper pairs passed through the junction. The supercurrent flowing through the junction (direct current Josephson effect) is driven by the phase difference between both sides of the junction. From the electrical point of view, a Josephson junction behaves as a non-dissipative and nonlinear inductance whose value depends on the phase, and thus on the current. Superconducting qubits have the particularity of being the only mainstream ones that are macroscopic. Their states are collective excitations of a superconducting circuit rather than states of an individual quantum object such as an atom, an electron or a photon, as in most other qubit technologies.

At superconducting temperature well below the superconductivity critical temperature, Josephson junctions embedded in an electrical circuit behave as an artificial atom, with gate and/or flux controlled quantum levels and about 10^{11} electrons (100 billion) of electron Cooper pairs.

They form an artificial atom with precisely controllable energy levels according to their parameters comprising a Josephson barrier, some capacitances and inductances connected in series and/or in parallel and some readout circuits using a nearby resonator [395]. This artificial atom property was first demonstrated in 1985.

Superconducting qubits use non dissipative elements: capacitors, inductors and the Josephson junction which act as a nonlinear non-dissipative inductor. Capacitors store energy in the electric field while inductors store energy in the magnetic field. But at any non-zero frequency, superconductors still dissipate some power, through three channels: the transport by the Cooper pairs, by normal charge carriers (quasiparticles), that is proportional to the quasiparticle density, which diminishes exponentially at low temperatures, and through the dissipative qubit readout process.

1.3.1 History

The history of superconducting qubits started in the mid-1980s but you need to fly back to 1957 with the elaboration of the **BCS theory** that explained (partially) how pairs of opposite spin electrons - *aka* Cooper pairs - behave at low temperatures, generating the superconducting effect. Then, 1962 marks the Josephson effect discovery by **Brian Josephson**, completed by its experimental proof in 1963 by **John M. Rowell** from the Bell Labs.

In 1980, **Anthony Leggett** modeled the collective degrees of freedom of superconducting circuits. A bit like a Bose-Einstein condensate of cold neutral atoms, electron Cooper pairs in a superconducting material behave like a single quantum object with its own quantum wave [396]. Antony Leggett understood that the quantum behavior of a Josephson junction, if any, can be inferred from its classical behavior. In a Josephson junction, the Cooper pair density difference n and the Josephson phase θ are conjugate variables with $[n,\ \theta] = i$.

In 1985, **John Clarke**, **Michel Devoret** (his post-doc) and **John Martinis** (his PhD student), demonstrated the phenomenon of Macroscopic Quantum Tunneling of a current-biased Josephson junction out of its zero-voltage state [395]. For the first time, a collective quantum object exhibited quantization. The three scientists were awarded the Nobel prize in physics in 2025 for this foundational discovery.

Soon after, they demonstrated quantum levels for the phase. This was the first artificial electrical atom. Back then, the JJ (the little nickname for Josephson junctions) was implemented with Nb-NbO_x-PbIn (niobium, lead, indium) and cooled with a He_4-based cryostat.

superconducting qubits key takeaways

highlights

- **key technology** in the academic world and with the largest and well funded commercial vendors community including large players like IBM, Google, IQM and Rigetti.
- **large programmable superconducting QPUs** now exceed 100 physical qubits with Google (105 qubits), IBM (120 and 156 qubits) and Fujitsu (256 qubits).
- **noise reduction** constant progress in regular transmons with tunable couplers and with bosonic qubits which could enable a record low ratio of physical/logical qubits [381, 382].
- **below-threshold surface-code memory beyond break-even**: Google's Willow reached a distance-7 surface-code memory using 101 physical qubits, with a logical error per cycle of about 0.143% and a suppression factor $\Lambda = 2.14 \pm 0.02$ [43].
- **enabling technologies** are abundant with cryostats, cabling, analog electronics, amplifiers, and sensors.
- **quantum error mitigation** techniques to enable NISQ applications [383].

challenges

- qubits variability: requires calibration and complex microwave frequency maps and need to contain crosstalk [36, 37].
- **qubit connectivity**: limited to neighbor qubits in 2D structures.
- **qubit coherence time**: usually < 300 μs with some lab records >1 ms [155, 156].
- **cryogeny**: qubits operating at <15 mK.
- **cabling clutter**: complexity and many passive and active electronic components to control qubits with microwaves and other signals.
- **qubits size**: uneasy miniaturization limits qubit # per chips and requires QPU interconnect solutions [86].
- **qubit fidelities**: QEC does not have a universal 99.9% fidelity requirement. Thresholds depend on the code, circuit, noise bias, leakage and correlations. For surface-code-like circuits, physical two-qubit error probabilities of order 10^{-3} are a useful engineering target, but fault tolerance is determined by the complete error model [42, 43].

variations

- **bosonic qubits**: cat-qubits, GKP, dual rail, whose encodings can provide hardware-efficient error protection or biased noise, potentially reducing QEC overhead. They are less mature but promising [382, 384, 385].
- **fluxonium qubits**: with better fidelities but a more complicated designs and few involved vendors [155, 156].
- **qutrits**: with larger Hilbert space, which are exotic in the commercial world [386, 387].
- **Andreev spin qubits**: localized excitation of the BCS condensate encoding a computational two-level subspace in Andreev bound states, using a nanowire [388, 389].
- **hybrid quantum analog-digital architectures**: to solve specific problems, not generic.

path to scalability

- **materials**: improve elements purity, identify other promising ones [78, 79].
- **EDA**: full stack electronic design automation tools [390].
- **manufacturing**: industrialization, 300 mm wafers epitaxial deposition [391, 392].
- **qubit mid-range coupling**: to enable lower overhead qLDPC QEC [88, 89].
- **interconnect**: using transduction and photonic gate teleportation [86, 87].
- **signals multiplexing** with microwave-photonic conversion, or SFQ control electronics: to reduce cabling overhead and cryogenic requirements [82–84].
- **QEC syndrome detection** speed gains using ASICs [393, 394].
- **cryostats**: larger and more efficient with helium liquefiers.

Figure 19: Superconducting qubits highlights, challenges, variations and path to scalability. 🅭 Olivier Ezratty, 2021-2026.

In 1998, **Vincent Bouchiat**, then a PhD in **Michel Devoret**, **Daniel Esteve** and **Cristian Urbina**'s Quantronics group at CEA-Saclay in France, implemented the first Cooper Pairs Box (CPB) and characterized its ground state. Practically speaking, a Cooper pair box is a JJ connected to a voltage source by a capacitor on one side, and a Josephson junction on the other side.

The first demonstration of quantum coherent superposition with the first excited state was achieved in 1999 by **Yasunobu Nakamura** with **Yuri Pashkin** and **Jaw-Shen Tsai** at NEC Labs in Tsukuba, Japan [397]. It was the first "charge qubit" per se, with a tiny coherence time of 2 ns. They extended it in 2001, implementing the first measurement of Rabi oscillations associated with the transition between two Josephson levels in the Cooper pair box, using the configuration developed by Vincent Bouchiat and Michel Devoret in 1998. A first functional qubit version of the Cooper pair box, the quantronium, was demonstrated by the CEA-Saclay Quantronics team in 2002. It took about 12 years to CEA's team to reach 4 qubits (Figure 20) [398]. Back then, IBM and Google teams were also at a similar stage.

The modern version of the CPB circuit, the transmon, was developed at Yale University in 2006 (Figure 22). The Yale University research teams led by **Rob Schoelkopf**, **Michel Devoret** and **Steve Girvin** welcomed many talented theoreticians and experimentalists who were key contributors to the progress of transmon qubits.

Alexandre Blais and **Andreas Wallraff** developed around 2003-2004 the key principles of circuit QED (cQED) as shown in Figure 21 [399–402]. It allowed quantum non-demolition readout of qubit state in the dispersive regime. A QND readout happens after measurement collapses the wave function onto $|0\rangle$ or $|1\rangle$ and a subsequent readout will yield the same $|0\rangle$ or $|1\rangle$.

Then, **David Schuster** and **Jay Gambetta** created between 2007 and 2011 2D and 3D cavity resonators designs [403–405].

Jens Koch created Cooper pair boxes with a large shunting capacitance which created a modest reduction in anharmonicity and enabled strong coupling with microwave photons [406].

Jerry Chow was also a key contributor between 2005 and 2010 and has since then been at IBM, now leading their quantum hardware system developments in Jay Gambetta's team.

In 2009. Devoret, Schoelkopf, **Leonardo Di Carlo** (now at TU Delft), **Jerry Chow** et al. created the first programmable two-qubit processor and implemented a small Grover search on it. The first functional two-qubit processor fully fitted with a universal set of gates and individual single-shot qubit readout was then in 2012 demonstrated with Grover's search algorithm by A. Dewes et al. at CEA Saclay.

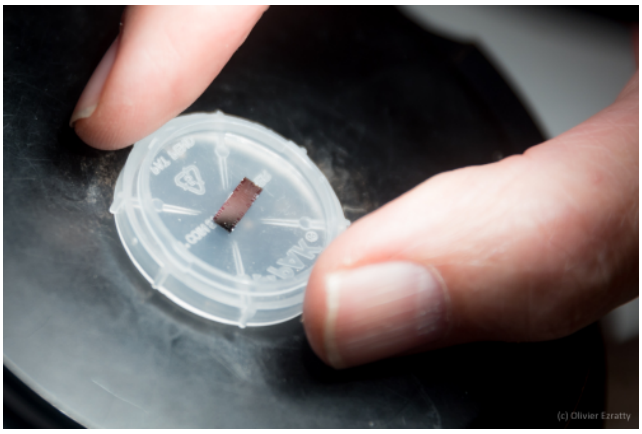

Figure 20: Daniel Esteve (CEA Quantronics) showing to the author the first operational two-transmon processor in his laboratory, June 2018.

In another domain, **Matt Reagor** and **Hanhee Paik** improved in 2013 the stability of microwaves and qubit coherence (T_1/T_2) with transmons embedded in 3D cavities [408]. These high Q-factor cavities enable long T_1 and are still investigated [409].

Other contributions worth mentioning are **Hans Mooij** (TU Delft) who created a flux-qubit with three Josephson junctions in 1999 with experiments done in 2000. **Andrew A. Hook** (Princeton) contributed to the development of the transmon qubit. In 2010, **Andrew Cleland**, **John Martinis** and their PhD **Arron O'Connell** were able to entangle three flux superconducting qubits and to control it with a mechanical resonator [410]. It led to the creation of the Xmon tunable qubit in 2013 [411], which was later used by John Martinis at Google after 2014, and later, by Rigetti and IBM. **Andrew Cleland** now runs his own lab at the University of Chicago.

Blake Robert Johnson proposed in 2011 to use a Purcell filter to protect a qubit from spontaneous emission coming from the Purcell effect that is a relaxation through the readout resonator. It is a mix of low-pass and high-pass microwave filter [412–414]. The spontaneous emission rate (SER) is one key contributor that affects a superconducting qubit coherence time T_1.

In 2017, **Peter Leek,** then at Oxford University, created the coaxmon superconducting qubit, where the qubit and resonator are on opposing sides of a single chip, with control and readout wiring being provided by coaxial wiring running perpendicular to the chip plane [415]. It led the same year to the creation of OQC.

In 2022, **Mikko Möttönen** from IQM created the Unimon superconducting qubit with a simpler setting, better nonlinearity and fidelities [416]. However, both these qubits have not yet showcased improved figures of merit vs the state of the art.

Then, cat-qubits were created in 2013 by **Mazyar Mirrahimi** at Yale with Michel Devoret, with later contributions by **Zaki Leghtas** and many advances since then.

Let's now circle back to the different types of superconducting qubits that differ in the way they encode quantum information in two distinct states (Figure 23):

Phase Qubits use larger Josephson junctions than in charge qubits. Their state corresponds to two levels of current energy in a Josephson junction. This approach was tested by NIST in the USA among other places but no commercial vendor seems to use this type of superconducting qubit. John Martinis tested such qubits back in 2012 at UCSB in a 5-qubit system used to factor the number 15 [417]. A German (Jülich, University of Munster) and Russian (Kotelnikov Institute) team proposed in early 2020 to use $YBa_2Cu_3O_7$-x nanotubes (also called YBCO, for yttrium, barium, copper and oxide, which is superconducting at 92K) to create phase qubits controllable by a single microwave photon [418]. Overall, the phase qubit seems to be dead-end.

Flux and fluxonium qubits: a conventional flux qubit can be described in a persistent-current basis, with clockwise and counter-clockwise currents corresponding approximately to two flux states. A fluxonium is different: it is an inductively shunted Josephson circuit whose computational states are eigenstates of the nonlinear phase/flux degree of freedom. Fluxonium combines large anharmonicity with long coherence in optimized devices, at the cost of a superinductor, flux biasing and more complex control. Atlantic Quantum adopted fluxonium before its acquisition by Google. Rigetti, by contrast, uses transmon-family superconducting qubits rather than fluxonium [419].

It is studied in research labs at the MIT Lincoln Lab in Will Oliver's team [419–421], the Lawrence Berkeley National Laboratory (Irfan Siddiqi [422, 423]), the University of Berkeley, the University of Maryland (Vladimir Manucharyan – now working at EPFL - with a T_2 exceeding 1.35 ms and single-qubit gate fidelity over 99.99% [156, 424], flip-chip packaging with an SFQ electronics chip [425] and other improvements [426–428]), Princeton University [429], Stanford University [430, 431], the University of Illinois Urbana-Champaign [432,

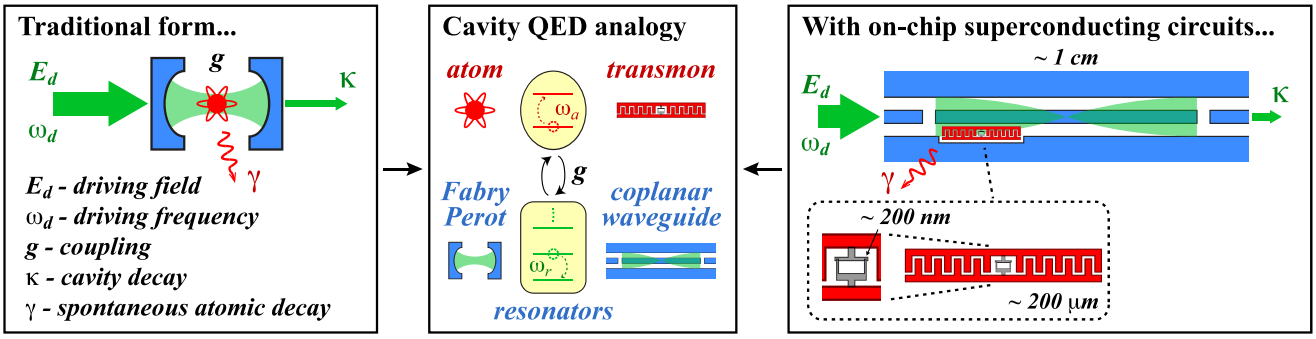

Figure 21: Circuit QED principles. Source: [407].

433], NBI in Denmark [434], QuTech and TU Delft [37, 435, 436], in Russia, with two qubits CZ gates fidelities of 99.23% [437], the creation of a native CCZ gate [438], and simulations reaching 99.99% fidelities [439, 440]), in China at Hefei [441–443], in Shenzhen Tenghui Wang's team [444–446], Guangzhou Zheng-Yuan Xue's team [447–449] and Hangzhou Chaoying Zhao's team [450, 451], in Shanghai and other places [452], in Taiwan [453], and in Israel at Bar Ilan University, with improved fabrication techniques [454, 455].

In recent works, Vladimir E. Manucharyan's team at Maryland University and EPFL created fluxonium qubits with the best T_1/T_2 with T_1 exceeding 1 ms and two-qubit gate fidelities reaching 99.94%, although with only two qubits in a lab setup [155]. They use control frequencies usually below 3 GHz which lowers down dielectric loss effects and leads to long relaxation time T_1.

Single-qubit gates can have good speed in the range of 10 ns and errors levels around 10^{-4} [456]. In this architecture, both readout and control crosstalk are expected to be small [457, 458]. State-of-the-art devices are attractive because T_1 and T_2 can be long [155, 156]. The engineering costs are instead the Josephson-junction-array superinductor, low transition frequencies in some designs, flux-bias requirements, control/readout complexity, possible readout-induced leakage [459], and the wiring and crosstalk associated with DC flux lines [460, 461]. Work is also ongoing with improving qubit reset as well as non-demolition and fast readout [462–464].

The **heavy fluxonium** variant uses a different geometry with a 3D transmon shunted by a large linear inductance of a Josephson array [465]. Qubit gates can be driven by simple DC and RF flux, removing the need for complex microwave waveforming with AWG (arbitrary waveform generators). It reached two-qubit gate fidelities of 99.9%, although with only two qubits. There's even a variation of the fluxonium nicknamed the Fracxonium, which implements qudits [466].

In the quantum annealing domain, D-Wave uses superconducting flux-based circuits coupled magnetically to implement quantum annealing. D-Wave previously developed a separate fluxonium gate-model roadmap, but its January 2026 acquisition of Quantum Circuits shifted the public gate-model emphasis toward dual-rail cavity erasure qubits. The acquisition does not by itself prove that every fluxonium research activity was terminated.

Charge qubits: the Cooper-pair-box basis is associated with different numbers of excess Cooper pairs on a small superconducting island, not with current-flow thresholds. The **transmon**, for "transmission-line shunted plasma oscillation qubit", operates the Cooper-pair box at large E_J/E_C, strongly reducing charge dispersion and charge-noise sensitivity at the price of smaller anharmonicity [467].

The nonlinear Josephson element renders the circuit oscillator weakly anharmonic, and the two lowest eigenstates are used as the computational basis. Transmons are used by IBM, Google, IQM, Rigetti and many others. They remain the dominant commercial superconducting modality and achieve very low errors at scale, although selected fluxonium experiments can now show still lower gate errors and longer coherence. Their relatively small anharmonicity constrains pulse bandwidth and increases leakage risk when gates are made too fast.

Transmons may use a single Josephson junction for a fixed-frequency design or a SQUID made of two junctions for flux tunability. Vendor implementations evolve. The name refers to a transmission-line-shunted plasma-oscillation qubit. Here "plasma" is the Josephson plasma mode of the nonlinear superconducting circuit, not to the ordinary free-electron plasmon of a normal metal. The large shunt capacitance reduces sensitivity to offset-charge noise.

Then, you have many variations with the **dimon-coaxmon** (OQC) and **unimon** (IQM), the **merge-mon** or merged element transmon where the Josephson junction is engineered to act as its own parallel shunt capacitor, reducing the size of the qubit [470]. Here, the split junction is based on a SQUID geometry, equivalent of a tunable Josephson junction. It is very convenient, but sensitive to flux noise. There are other variations like the **Blochnium** [471] and the **quartic Blochnium** [472, 473], with large inductances made of many Josephson junctions, enabling better anharmonicity, the Harmonium with good bit-flip protection, from MIT [474, 475], **van-Der-Waals** qubits using a $NbSe_2$–hBN–$NbSe_2$ junction with a smaller footprint

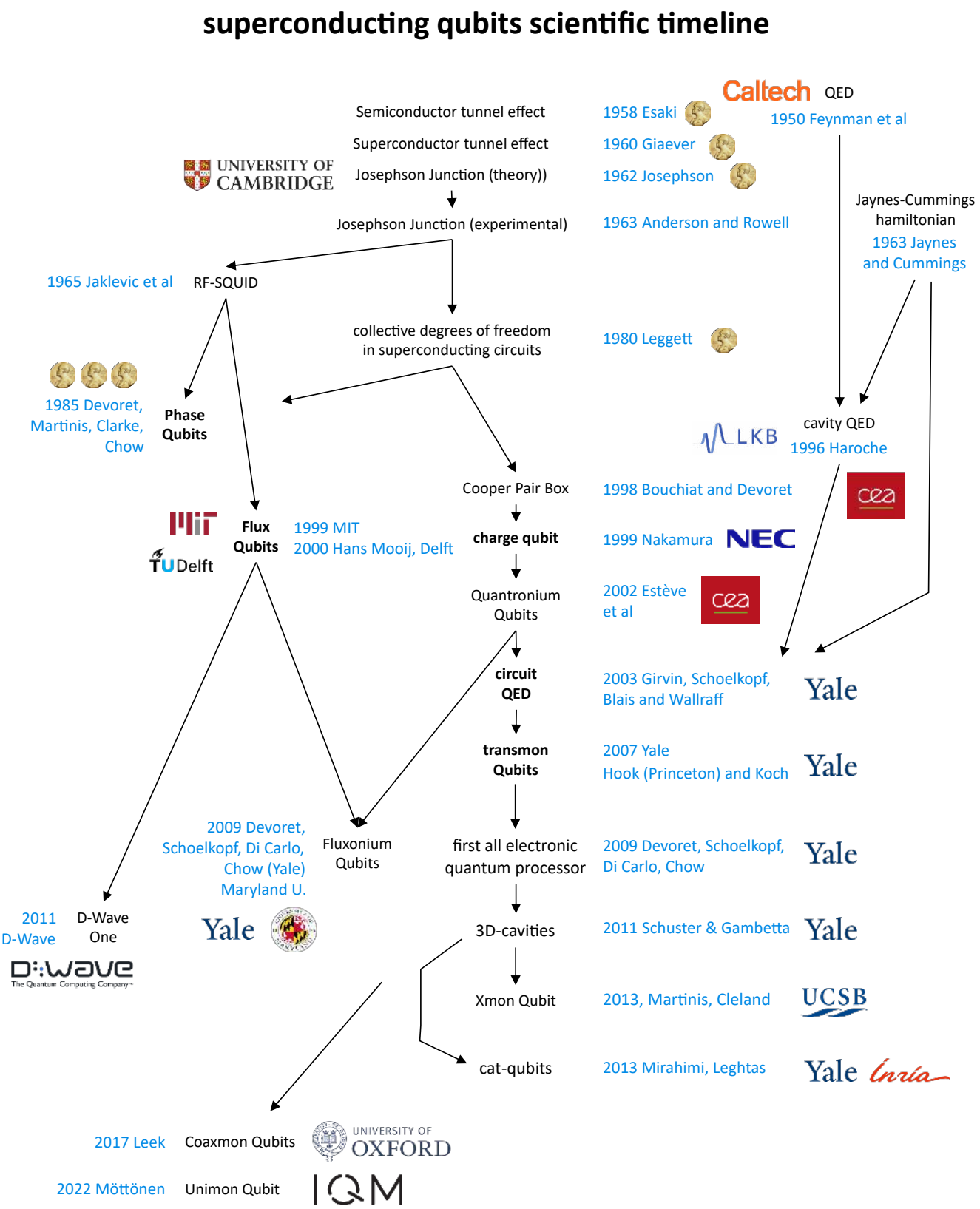

Figure 22: Historical timeline of superconducting qubits. The contribution of scientists at Yale University seems dominant here, thus the nickname of the "Yale gang". © Olivier Ezratty, 2022-2025.

[476], also from MIT, the **NMon** [477], the **Kinemon** developed in Russia, with inductively shunts transmons to improve the two-level system anharmonicity [478], and even using quantum batteries which store energy at the quantum level and enable dissipation-less unitary gates [479].

Bosonic qubits encode one qubit, or sometimes a higher-dimensional logical system, in states of a bosonic

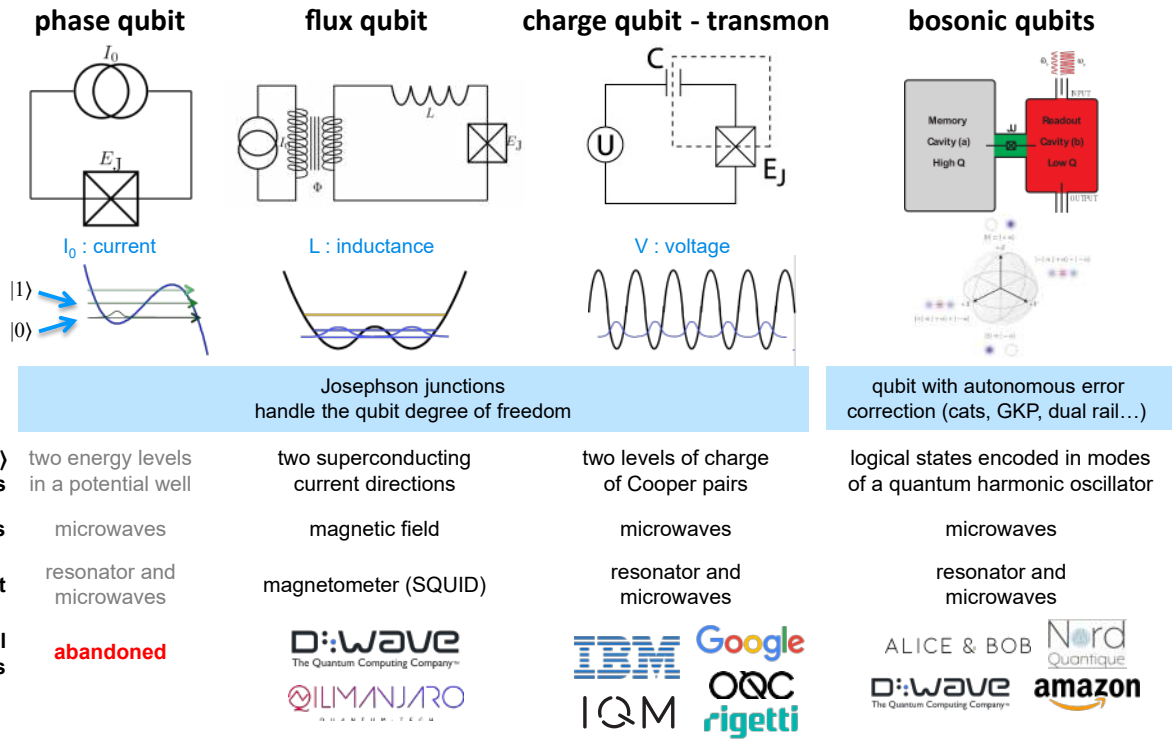

Figure 23: Different types of superconducting qubits and the related industry vendors. inspired by [468, 469]. Updated in 2023-September 2026.

mode such as a superconducting microwave resonator. Their purpose is to engineer the noise so that a dominant error channel is suppressed or becomes easy to detect and correct, potentially reducing the total hardware overhead of QEC [382]. Autonomous stabilization or autonomous QEC is implementation-dependent rather than a defining property of all bosonic codes. Cat qubits can exponentially suppress bit flips as photon number increases while leaving phase errors to be corrected by an outer code. GKP codes protect against small phase-space displacements but still require repeated syndrome extraction and correction. Some implementations use engineered dissipation [480], 3D cavities and transmon or fluxonium ancillas [481, 482], as well as fully planar architectures pairing fluxonium control with on-chip high-Q spiral resonators [483].

The main types of known bosonic qubits are **cat-qubits** and **GKP codes** [384, 484–487], **cos(2θ)** *aka* **cos(2ϕ)** qubits [488, 489], the **Kerr-cat** that are studied at Berkeley, Chapman University and in Germany, [490–492], and other variants [493–495]. See a comparison in Table 3, including nanomechanical oscillator and ancilla defect spin-based cat-qubits [496].

Other types of qubits include **dual-rail** encodings. They do not replace all Pauli errors by erasures. Rather, they are engineered so that dominant loss events leave the computational subspace and can be heralded as erasures, while residual dephasing and other Pauli errors remain. Located erasures can be corrected at substantially higher thresholds than unlocated Pauli errors. They are studied at Yale University, Orford University [385], in China [531, 532], and used by Quantum Circuit Inc (at D-Wave since 2026). A variant of dual-rail qubits named DRCC (dual-rail cat codes) combines dual-rail qubits and concatenated bosonic encoding and was proposed by Giulia Ferrini from Chalmers University in 2026 [533]. However, transmon qubits can also be converted into erasure qubits [534].

cat-qubits are cavity-based qubits connected to a transmon qubit used only for their preparation, readout and/or correction depending on the implementation. The cat-qubit technique was devised by Mazyar Mirrahimi and Zaki Leghtas around 2013, particularly during their work at Yale University with Michel Devoret. Cat-qubits are investigated in research labs like **RIKEN** in Japan [535] (on top of regular transmon qubits with a record prototype chip of 100 qubits [536]), **RWTH Aachen University** and **FZ Jülich** in Germany [537], at EPFL which collaborates with Alice & Bob [538, 539], and even in China [540–542]. Bosonic qubits are usually directly aiming at FTQC architectures but to some extent, they could be used for NISQ applications [543]. The cat-qubits approach is chosen by **Alice & Bob** (France) [525, 544], while **Nord Quantique** (Canada) and **AWS** (USA) are using GKP codes while also testing cat-qubits and dual-rail qubits [511, 545] and **QCI** (USA) is using dual-rail qubits. Then we also have **zero-π qubits** by Peter Brooks, Alexei Kitaev and John Preskill which use two Josephson junctions, and the **bifluxon** [546].

Hybrid superconductor-semiconductor qubits (S-Sm) replace the fixed tunnel junction of a transmon

Cat-qubits	GKP codes	Dual-rail qubits
Pros		
Bit-flip suppression: its rate decreases exponentially with the mean photon number $\bar{n}$. Measured bit-flip times reach 100 s in a two-photon dissipative oscillator and above 10 s under full qubit control [497–500]. **Hardware-efficient QEC**: only phase flips are corrected by a 1D repetition code or an LDPC-cat code which replaces a full 2D surface code up to some circuit scale (10^7). [501–503]. **Autonomous stabilization**: two-photon driven dissipation pins the state to the cat manifold with no measurement or decoding latency [498, 504, 505]. Concatenated QEC demonstrated with 5 cat modes and 4 transmon ancillas at a distance-5 repetition code, for about 1.65% logical error per cycle [506].	**Protection in both quadratures**: grid states correct small displacements in position and momentum, so photon loss and dephasing are addressed by a single encoding [484, 507]. **Maximal hardware efficiency**: one qubit lives in a single oscillator. Real-time QEC beyond break-even demonstrated in circuit QED, and autonomously with reservoir engineering [384, 508, 509]. **Enables magic states**: Clifford gates and GKP error correction generate distillable magic states [510–512]. **High concatenated thresholds**: the analog syndrome holds the size of the measured displacement, which increases the threshold of the concatenated surface code [513–515].	**Erasure conversion**: the dominant single-photon loss takes the state out of the $\{\|01\rangle, \|10\rangle\}$ subspace, where it is heralded. It becomes a located erasure [385, 516, 517]. **Much higher tolerance**: topological codes tolerate located loss up to 24.9%, against the roughly 1% threshold for regular transmons [518–520]. **Two hardware routes**: the same encoding works with photonic modes or with two coupled superconducting cavities or transmons [385, 516, 521]. **Demonstrated primitives**: erasure-detected logical measurement [522], long-coherence transmon dual-rail [521], and a 500 ns entangling gate at about 99.60% Bell-state fidelity in which erasures dominate residual Pauli errors [523].
Cons		
Phase flips grow with $\bar{n}$: the phase-flip rate rises roughly linearly with $\bar{n}$ while the bit-flip rate falls exponentially [501, 524]. **Preparation and control overhead**: stabilization needs a nonlinear element such as an ATS, continuous pump tones and more control lines per qubit [157, 498, 505]. **Non-Clifford cost**: bias-preserving gates and magic-state preparation remain the bottleneck, at 53 to 175 physical qubits per T state depending on the noise bias [525–527].	**Squeezing requirement**: the code only pays off above roughly 10 dB of effective squeezing, which is demanding for a microwave oscillator coupled to a lossy ancilla [513, 515]. **Demanding oscillator control**: preparing and stabilizing finite-energy grid states requires fast conditional displacements and a high-fidelity ancilla [486, 487, 494]. **Ancilla back-action**: ancilla errors propagate into the oscillator. The best SPAM figures, below 7×10^{-4}, still rely on postselection with only 9% acceptance [511, 528]. **Modest gains**: autonomous QEC of a single-mode GKP qubit improved the lifetime by about 14%, to roughly 208 μs [509].	**Loss is relabeled, not removed**: the physical loss rate is unchanged. Erasure rates is one to two orders of magnitude above residual Pauli errors, so the outer code spends most of its budget on frequent erasures [517, 521]. **Residual Pauli errors persist**: correlated dephasing and leakage escape the erasure check and still need an outer code [385, 529]. **Hardware doubling**: two modes plus a mid-circuit erasure check per qubit, and the check itself must be fast, QND and high fidelity [522, 530]. **Early scale**: demonstrations done for a few encoded qubits [523, 531].

Table 3: Comparison of cat-qubits, GKP codes and dual-rail qubits. The three encodings trade the same quantity differently: cat-qubits benefit from an exponentially biased noise channel with low flip error at the price of higher phase noise, GKP codes get symmetric protection at the price of oscillator control and squeezing, and dual-rail qubits get located errors at the price of two modes per qubit and an unchanged loss rate. None of the three removes the need for outer error correction codes. ©Olivier Ezratty, 2024, updated in September 2026.

by a semiconductor weak link, usually with some III/V compounds (InAs, InAlAs, InSb) or graphene nanostructures, nearby an adjacent superconductor.

Two main qubit encodings are investigated:

- **Gatemon qubits** which keep the collective electromagnetic mode of the transmon circuit and only makes its Josephson energy tunable with a gate voltage [547–553].

- **Andreev spin qubits** (ASQ) which encode in a microscopic excitation, either the spin of a quasiparticle trapped in an Andreev bound state or the fermion parity of that state. They rely on a localized excitation of the BCS condensate that natively has two levels, not on a collective excitation of the superconducting circuit. ASQ were proposed at Chalmers in Sweden [554, 555] (funded as a H2020 program from 2019 to 2023 [556]), with coherent manipulation of Andreev levels first shown at CEA Saclay in atomic contacts [557, 558], the first ASQ at Yale [388], and direct spin manipulation and two-qubit coupling at QuTech in the Netherlands [389, 559, 560]. The superconducting singlet-triplet (SST) variant proposed by Lotkov, Loss and coauthors in 2026 uses parallel-aligned double quantum dots in Josephson junctions, with tunable all-to-all connectivity as the main benefit [561]. Another variant named FerBo, combining Andreev and fluxonium states, was proposed by CEA in 2026 [562].

The main benefit of S-Sm is simplified electrical control. Josephson coupling becomes tunable with an electrostatic gate voltage, which removes the static dissipation and the long-range inductive crosstalk of usual transmon flux bias lines. In a flux-tunable transmon, control is a low-impedance current drive of order 1 mA that cannot be filtered without losing control drive. With S-Sm, gate control is a high-impedance voltage drive into an insulated gate drawing only picoamps, so it can be filtered and thermalized easily, which enables a greater wiring density. These devices also tolerate in-plane magnetic fields of 0.1 to 1 T, enabling spin manipulation [563]. All-to-all connectivity with selective pairwise coupling has also been proposed for ASQs, at the cost of serialized gates [564].

Recent experiments remain proofs of concept, with Sn-InAs nanowire transmons reaching tunable anharmonicity beyond the short junction limit [565], and an Andreev molecule, two junctions sharing bound states, used to read fermion parity through a nonlocal Josephson effect, a key primitive for parity qubits and Kitaev chains [566]. A separate hybrid thread couples superconducting circuits to spin ensembles for quantum memories [567] and pushes microwave detection toward single electron spins [568], with transducer leakage suppression as a networking prerequisite [569].

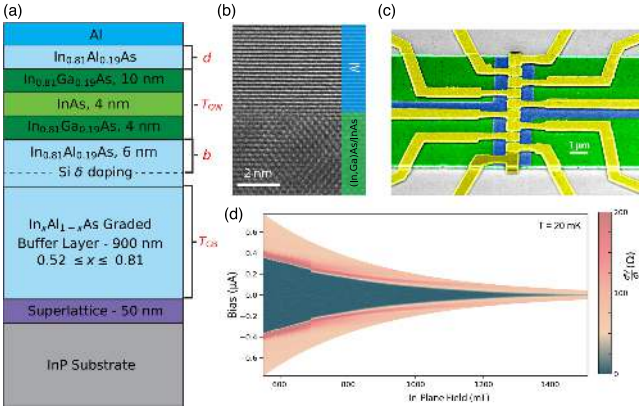

Figure 24: The material platform shared by all S-Sm qubit encodings. (a) an (In, Ga)As/InAs/(In, Ga)As quantum well grown on an InP substrate, lattice matched through a step-graded $In_xAl_{1-x}As$ buffer, with a thin $In_{0.81}Al_{0.19}As$ layer serving as a diffusion barrier between the aluminum and the quantum well. (b) transmission electron micrograph of an atomically clean $Al/In_{0.81}Ga_{0.19}As$ interface, whose quality sets the hardness of the induced gap and therefore the quasiparticle poisoning rate. (c) gated planar Josephson junction fabricated on the heterostructure in (a), where multiple independently tunable gates spatially modulate the topology of the junction through the chemical potential. (d) differential resistance versus in-plane field, showing a 1.4 T critical field enabled by an aluminum film thinner than 10 nm. Source: Fig 2 in [570], a perspective on topological Josephson junctions.

The caveats differ by encoding. Gatemons were benchmarked as early as 2016 with single-qubit gate errors below 0.7% and a controlled-phase two-qubit gate with 91% fidelity [549], and those figures have not caught up with transmons because coherence has not, with 2DEG gatemons measuring only about 2 μs, limited by dielectric loss in the substrate [571]. For Andreev spin qubits, a longitudinal coupling between two distant qubits tested [560], but no entangling gate fidelity has been benchmarked yet. Coherence is the real bottleneck, with T_2 reaching 390 ns [563] against 100 μs to 1 ms for leading transmons. A transmon with 30 ns gates allows some $3 \cdot 10^3$ operations, an ASQ with nanosecond gates barely 10^2. Material disorder and the low yield of InAs and hybrid nanowires remain problematic across multiple III/V layers (see Figure 24), and topological protection is still not experimentally established.

Analog simulations. Superconducting qubits can also be used to run quantum simulations at the native level, thanks to low level analog control of inter-qubit connections. Various experiments are testing this model [572–574]. It is not a common practice, one of the reasons being the lack of generic long-range connectivity that could enable some direct entanglement between all qubits. It would require a different physical arrangement of the qubits and to create specific long-range connections between the qubits. Cross-resonance gates do not provide generic long-range coupling. They use a microwave drive to activate an effective interaction between qubits that are already physically coupled, typically through a bus resonator or direct capacitive network. Long-range analog interactions instead require an explicit bus, resonator network, tunable coupler, router or other non-local coupling architecture.

Another option is to use superconducting programmable switches [575]. Yale University published a preprint on a hybrid scheme in September 2024 to simulate mixed fermionic-bosonic quantum systems [576] and another one for chemical simulations using a custom bosonic superconducting Kerr-cat device [577]. Another academic proposal from Israel and South Korea is based on a circuit QED circuit based on flux tunable qubits in resonance with an electromagnetic mode in a resonator to simulate relativistic Dirac Hamiltonians [578]. Yasunobu Nalamura's team in Japan and Google are also studying the potential of superconducting qubits based analog simulations [579, 580]. It is also tested by Google (see their related part later in the vendors list) as well as with fluxonium based qutrits [581].

1.3.2 Science

We will focus here on transmon qubits that are the most common and exploited by IBM, Google and IQM. They are based on anharmonic and therefore nonlinear oscillators. Their nonlinearity comes from the Josephson junction which better separates two energy states of the superconducting loop, on the right in Figure 25.

In a quantum harmonic oscillator (QHO), the energy levels are spaced equally and are multiples of the first energy level ($\hbar\omega_r$ in Figure 25). The capacitance has

an electrical energy (kinetic) and the inductance has a magnetic energy (potential) [582].

With a transmon, the Josephson junction replaces the linear-inductor potential by the nonlinear Josephson potential $-E_J \cos\phi$, producing unequally spaced energy eigenvalues. It is the oscillator energy that is quantized. Charge and phase are conjugate quantum variables, while the circuit current is an operator whose expectation value depends on the state. Transitions are typically driven by microwave pulses in the few-gigahertz range. Coupling these artificial atoms to quantized microwave resonators is the domain of **circuit quantum electrodynamics**, or cQED [558, 583].

A transmon state can be any superposition $\alpha|0\rangle + \beta|1\rangle$ of the two lowest circuit eigenstates. An equatorial state such as $(|0\rangle + |1\rangle)/\sqrt{2}$ undergoes free phase evolution at the qubit transition frequency. **Rabi oscillations** are driven oscillations of the state populations produced by a near-resonant microwave field. Their Rabi frequency is set by the drive amplitude and is commonly in the MHz to tens-of-MHz range, whereas the carrier frequency $\omega_{01}/2\pi$ is typically a few GHz.

These frequencies must be separable from the following ones. This separation is made possible because the (microwave photon) energy sent to move from one level to the other is different from one of these levels to other higher levels (Figure 27). Since the upper levels are less spaced, their related transition energy is lower. As the qubits are activated by microwaves, they are no longer likely to switch to a higher energy level. The anharmonic oscillator in the Josephson loop is provided by a nonlinear inductance L_j. The energy level between $|0\rangle$ and $|1\rangle$ of $\hbar\omega_{01}$ is higher than the energy levels needed to reach upper levels $\hbar\omega_{12}$ and $\hbar\omega_{23}$. It is also compatible with the cooling temperature of the processor and the ambient noise.

A 5 GHz qubit transition corresponds to $hf/k_B \simeq 240$ mK, much higher than a typical 10–20 mK mixing-chamber temperature. The usual few-GHz operating range is an engineering compromise among thermal excited-state population, dielectric and quasiparticle losses, frequency crowding, available microwave electronics, resonator design and control bandwidth. Lower frequencies increase thermal occupation, while simply increasing frequency is not free of materials and control penalties.

Quasiparticles are generated when Cooper's electron pairs are broken [585]. They are usually not created by the microwaves brought in unless they are very strong [586], but by higher frequencies and infrared light passing through all microwave lines or entering the cryostat, thus the need for filters, attenuators, and various shielding around the qubit chip [587].

There is also a large separation between the qubit transition energy and the energy required to break Cooper pairs. For aluminum, the superconducting gap is approximately $\Delta/h \sim 44$ GHz at low temperature, while the single-photon pair-breaking threshold is $2\Delta/h \sim 88$–90 GHz. Thus ordinary 4–8 GHz qubit-control photons are far below the pair-breaking threshold. Nonequilibrium quasiparticles can nevertheless be generated by stray infrared radiation, cosmic and radioactive energy deposition, or sufficiently energetic nonequilibrium processes [588].

What differentiates phase, charge (transmon) and flux qubits are the relative values of the charge energy (E_C, *aka* Coulomb charge energy), the Josephson coupling energy (E_J) and the qubit inductance energy (E_L) [589] (Figure 29).

E_J/E_C \ $E_L/(E_J - E_L)$	0	$\ll 1$	~ 1	$\gg 1$
$\ll 1$	cooper-pair box			
~ 1	quantronium	fluxonium		
$\gg 1$	transmon			flux qubit
$\gg\gg 1$			phase qubit	

Figure 29: Periodic table of superconducting circuits. Source: [590].

Then, just with transmon qubits, you find other variations with:

- Fixed (IBM (until Eagle in late 2022), MIT [591]) or tunable (Google, IBM starting with Heron in late 2023) qubit frequencies.
- Single or double tunable couplers (Google, IBM, Rigetti, Raytheon BBN [381], RIKEN [592]). Couplers are usually turned on and off, reducing crosstalk between qubits. Tunable couplers could also be implemented using a fluxonium qubits [593]. A 2026 proposal from Shengyu Zhang's Tencent team in China consists of stacking vertical tunable couplers and two superconducting chips [594] (Figure 30).
- Controlled-phase gates with variable amplitude and frequency which could significantly reduce the depth of quantum circuits particularly for implementing a quantum Fourier transform required in many algorithms like Shor, HHL and QML (C-R_θ) [595].
- New techniques to implement faster qubit readout [596, 597].
- Operating superconducting qubits at higher temperatures, around 1K, by replacing aluminum by niobium and using 75 GHz microwaves [598, 599].
- A Princeton 2D transmon with lifetimes and coherence times reaching 1.67 ms, a level usually obtained only with fluxonium qubits. It is obtained using high-resistivity silicon in the bulk substrate under a tantalum base layer used for resonators and other elements, to reduce losses. Single qubit gate fidelity is 99.994% [600].
- Mixing digital and analog superconducting computing [602, 603].

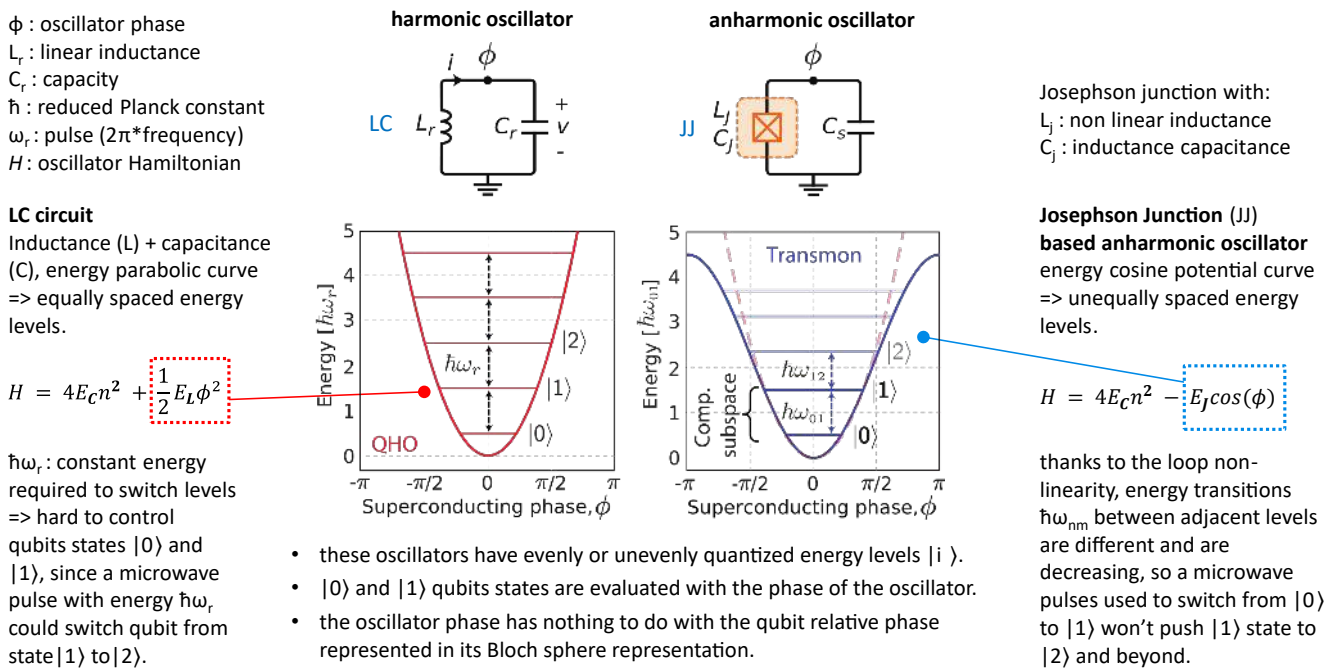

Figure 25: Why superconducting qubits use an anharmonic oscillator. © Olivier Ezratty, 2022-September 2026, reusing a schematic coming from [584].

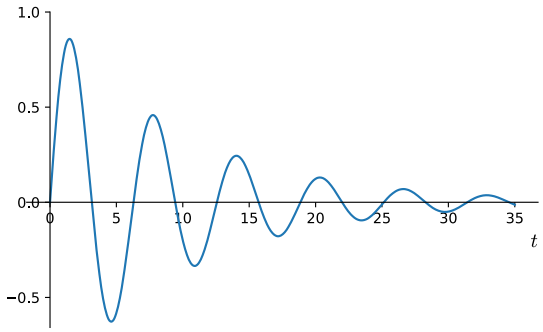

Figure 26: Driven Rabi oscillation of the qubit population under a resonant microwave pulse. The Rabi frequency is typically in the MHz to tens-of-MHz range and is distinct from the several-GHz qubit transition frequency.

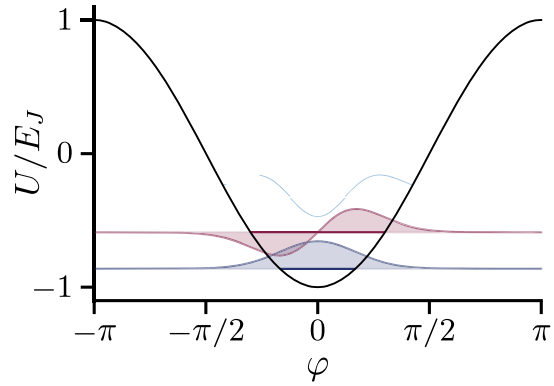

Figure 27: |0⟩ and |1⟩ wave function giving the probability of phase φ in blue and green. Source: [493].

- The Arm qubit proposed by the MIT which combines a fluxonium-like data storage mode and large capacitance in the transmon-like arm mode used for coupling between qubits. It enables faster, higher-fidelity entangling gates and qubit readout. Simulations show single-qubit errors below 1×10^{-5}, CZ two-qubit gates with error rate of 8.6×10^{-5} in 17 ns, and readout error of 1×10^{-4} in 27 ns, which are excellent. On top of that, the amplitude-based readout enables readout using a Josephson photomultiplier which is much simpler to implement [601].

- A proposal by RIKEN to use an artificial giant atom from waveguide quantum electrodynamics (wQED) to tailor the interaction between a transmon qubit and its environment. Based on another Josephson junction, it exhibits both frequency and power selectivity for photons. It reflects the single photons emitted by the qubit and remains transparent to strong microwave signals used for qubit readout and control. This design multiplies the qubit's lifetime by ten [604].

- Using qutrits instead of qubits, with Rigetti and others [386], including for creating GKP logical qutrits and ququarts [387].

Of course, many researchers are looking for ways to improve qubits fidelities with better materials and designs [605, 606].

In some cases, researchers invent useless things like trying to entangle superconducting qubits with tardigrades [607–610]. But the physics of a superconducting qubit

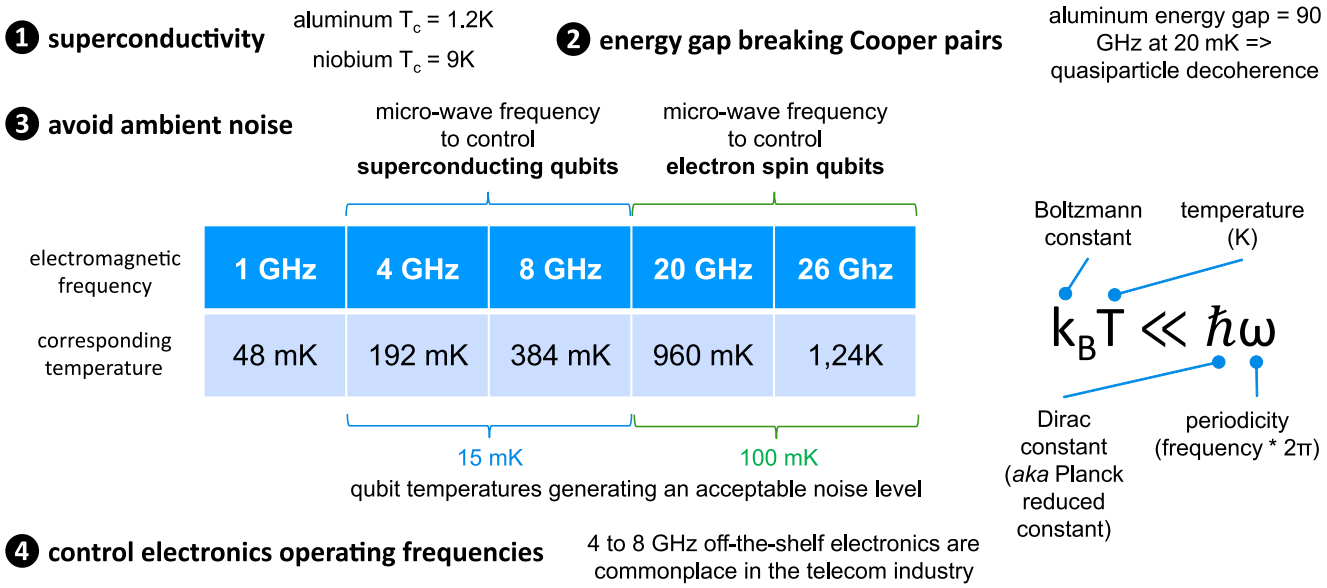

Figure 28: Rationale behind the 15 mK operating temperature of superconducting qubits. Many reasons explain why these qubits are operated at this low temperature. It is not just about materials superconductivity limits. ⓒ Olivier Ezratty, 2021-2024.

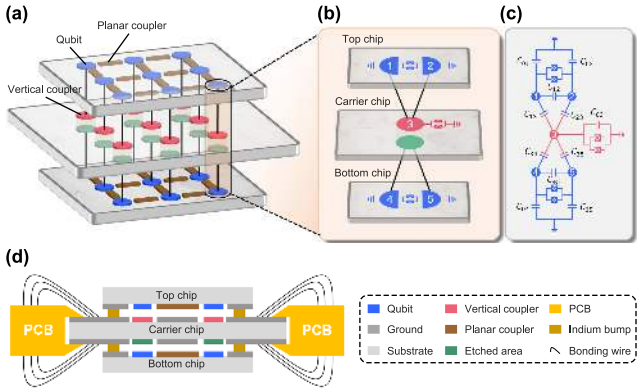

Figure 30: Tencent's vertical tunable coupler proposal using an intermediate chip between two superconducting qubit chips. Two-qubit gates have a fidelity of 97.5% within each chip and between chips, which is average. Source: [594].

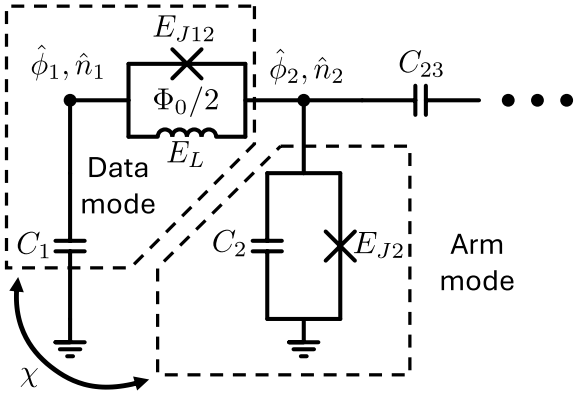

Figure 31: The Arm qubit proposed by the MIT in 2025, with a fluxonium-like qubit for data storage and a transmon like arm mode used for coupling qubits. Source: [601].

is much more complicated than that for the neophyte. The qubit itself is coupled to a cavity containing a resonator usually implemented as a **coplanar waveguide** (CPW) resonator on a superconducting circuit. A CPW is a type of transmission line used to guide electromagnetic waves, commonly at microwave frequencies, which consists of a central conducting strip, usually a superconducting material like niobium, flanked by two ground planes, all lying on the same plane, typically on the surface of a dielectric wafer substrate like silicon oxide or sapphire. Its length usually corresponds to a quarter-wavelength or the resonator drive frequency. With a 6 GHz drive frequency, it turns into a 1.25 cm resonator that is usually squeezed in a serpentine layout.

The qubit-resonator subsystem is often approximated by the **Jaynes-Cummings Hamiltonian** when the transmon can be reduced to two levels and the rotating-wave approximation is valid [611–614]. Its eigenstates in the interacting system are dressed qubit-photon states, not simply the bare qubit energy levels. In the dispersive regime, where qubit and resonator are sufficiently detuned, their interaction shifts the resonator frequency in a qubit-state-dependent way and enables QND-like readout [615–617].

Many parameters define a superconducting qubit's characteristics, including its **quality factor** Q. For an energy-relaxation-limited mode, $Q \simeq \omega T_1$, so a larger intrinsic Q corresponds to a longer relaxation time [618, 619]. A high qubit Q is not intrinsically detrimental to noise sensitivity. The relevant tradeoff occurs for deliberately coupled resonators: for example, an excessively high readout-resonator Q can slow measurement, while a lower external Q increases coupling to the measurement

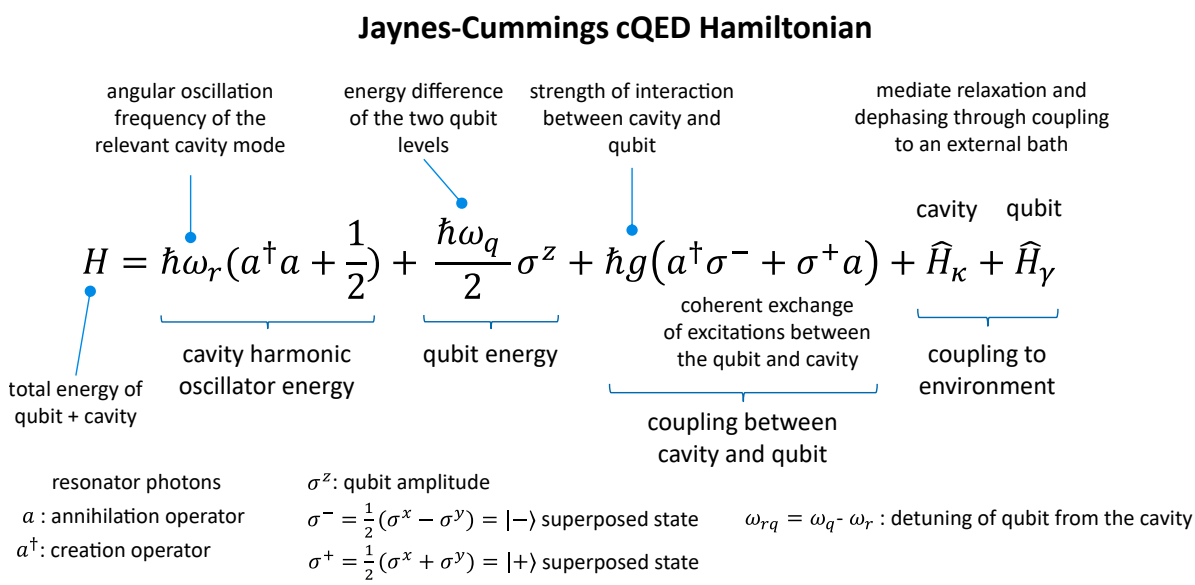

Figure 32: Jaynes-Cummings cQED Hamiltonian. Olivier Ezratty, 2022-2025.

line. Reported effective qubit Q values span roughly 10^5 to 10^8 depending on frequency, modality and device.

The sources of noise in superconducting qubits are multiple and the research literature is still sparse with regards to consolidating quantitative estimations of all sources of noise [620, 621], besides the ones coming from cosmic radiation that we already covered earlier when discussing quantum error correction.

Noise sources are numerous and, hopefully, can most of the time be mitigated. This laundry list is still impressive. It is organized here in three categories, material issues at the qubit level, measurement related noise and external influences. I do not provide such details for other qubit modalities for many reasons. Sometimes, noise sources are not as numerous because the qubits are well isolated like with cold atoms. Sometimes, it is due to a lack of maturity in the related research domain. Otherwise, it is just linked to a lack of information on my side.

- Material and interface-related losses within the qubits:
  - Two-level systems (TLS) losses, including dielectric losses from bulk substrates due to tunnel effect and which tends to increase with the number of qubits [622–625] or etching imperfections [626, 627]. Dielectric losses can be detected with THz nano-imaging and spectroscopy [628, 629].
  - Qubit coupling to material defects coming from interactions between qubits and material defects in substrates or films [630].
  - Charge noise from motion of charges in the qubit dielectrics and oxides.
  - Piezoelectric effects between the qubit and the silicon or sapphire wafer substrate [631, 632].
  - Paramagnetic spins fluctuations in the superconducting loop insulator interface.
  - Other spin and current artifacts at the Josephson junction in the circuit substrate [469, 633].
  - Radio-frequency losses in niobium resonators [634].
  - Residual energy dissipation originating from a universal density of nonequilibrium quasiparticles trapped within disorder-induced spatial variations of the superconducting gap. It influences the choice of materials, favoring niobium despite the above caveat [635].
  - Quasiparticle poisoning from the tunneling of single quasiparticles in and out of the superconducting island [636]. So far, it has been handled with gap engineering at Google [637] and with infrared filtering in Taiwan [638].
  - Ohmic losses due to quasiparticles residing in superconducting wires away from the junctions [639]. 1/f flux noise corresponding to the motion of trapped vortices in superconductor circuits. The 1/f noise is a low-frequency magnetic-flux noise showing up in the qubit that has a 1/f power spectral density [640].
  - Critical current noise coming from the motion of charges in the Josephson junction.
  - Various other tunneling effects in amorphous materials [641], partly due to defects introduced during the liftoff process after angle evaporation of the Josephson junction materials [642].
  - Other material defects in the Josephson junctions like oxygen vacancies [643] and also Josephson junction aging [644].
- Measurement related noise:
  - Measurement-induced state transitions with temporal fluctuations [645].

- Readout fidelity affected by standing waves that significantly worsen the spread of resonator linewidths and require added infrastructure for impedance matching [646].
- Measurement induced crosstalk [458, 647].

- External environmental influences:
  - Perturbations coming from the low frequencies generated by the compressors and pulse tubes that are cooling the cryostat at 4K [648].
  - Frequency collision *aka* frequency crowding affecting fixed frequency transmons [36], those using tunable couplers for two qubit gates [649] and even those using microwave pulse parametric modulation [650].
  - Influence of external circuits connected to the qubit (resonators, filters, ...).
  - Control electronics and qubit variability requiring frequent calibration, which can be optimized [651–654], even during a FTQC circuit execution and using data coming from quantum error correction as proposed by the DoE and Google [655, 656], and which was demonstrated as being efficient by Harvard researchers in August 2026 [657]. This variability can also lead to circumventing the malfunctioning qubits while implementing error correction codes [658].
  - Crosstalk between qubits created by their control signals and their routing [659–663].
  - Cosmic rays like gamma rays and muons, already mentioned in the error correction part of this book [664]. They create phonon bursts which generate quasiparticles consisting of broken electron Cooper's pairs, with electron charge and holes. It drives decoherence with the qubit losing energy to the quasiparticles, dephasing, charge-parity jumps modifying the qubit state and correlated errors, or correlated noise, when a single cosmic ray impact generates a burst of quasiparticles that affects multiple qubits simultaneously in the qubit chip [586, 665, 666]. These errors can be mitigated with the gap engineering method pioneered at Google in 2024 [637, 667]. Correlated errors can be generated on-demand by particle accelerators, which facilitates their study and mitigation [668].
  - Correlated noise coming from qubit control [669].

- Internal environmental influences:
  - Vacuum quantum fluctuations induced decoherence, considered minimal at this stage [670].

- Leakage errors correspond to the qubit escaping its computational $\{|0\rangle, |1\rangle\}$ subspace towards $|2\rangle$ and higher anharmonic oscillator energy levels. Leakage is not a noise source per se but an error channel fed by several of the mechanisms listed above and with the following effects:
  - Qubit control-induced leakage due to the spectral content of fast single-qubit pulses overlapping the $|1\rangle \rightarrow |2\rangle$ transition, mitigated with DRAG shaping which brings leakage down to the 10^{-4} range [671].
  - Two-qubit CZ gates leakage of about 0.1% per gate, out of the computational subspace due to parasitic coupling between the states $|11\rangle$-$|02\rangle$.
  - Readout-induced leakage, also labeled measurement-induced state transitions (MIST) or transmon ionization, appearing above a threshold resonator photon number [672–677].
  - Environmentally-induced leakage coming from quasiparticle poisoning and from cosmic ray induced phonon bursts, which populate higher levels across many qubits at once. See the corresponding items above and below.

  Leakage mitigation relies on multi-level reset protocols and leakage reduction units applied at every cycle, which bring the steady-state data qubit leakage population below 10^{-3} [678, 679], by applying a Rabi drive on the computational transition during dispersive readout as proposed by Yasunobu Nakamura in July 2026 [680], and on leakage detection schemes feeding error correction decoders [681].

1.3.3 Qubit operations

The general principle of superconducting qubits operations is as follows:

Qubit quantum state in the generic case of a transmon is a two-level charge of Cooper pairs that correspond to a nonlinear oscillator containing at least a Josephson junction and a capacitance laid out in a current loop. A flux bias (direct current pulse) can be used to individually control each qubit resonant frequency if it is frequency tunable. It can help reduce control frequency crosstalk between qubits but at the cost of a lower lifetime (T_1). Fixed-frequency qubits can reduce flux-noise sensitivity, whereas tunable qubits can mitigate frequency collisions and enable more flexible gates. Qubit initialization and reset must be as fast as possible, and some research is going on to optimize it [682–685] and even to conduct demolition readout (readout with reset) to speed up operations [686].

Single-qubit quantum gates are generated by microwave pulses sent via coaxial cables on the qubits. Their frequency is adjusted to the energy level $\hbar\omega_{01}$ mentioned above. This frequency is calibrated to be different on adjacent qubits to avoid crosstalk effects. A precise calibration of these frequencies is also necessary because of the variability of the behavior of Josephson junctions, which are different from one another due to imprecise manufacturing techniques. This variability does not exist for qubits based on trapped ions and cold atoms [687]. Static ZZ crosstalk is the one many researchers are working to suppress [688]. Static ZZ

coupling is an unwanted conditional frequency shift represented by a $Z \otimes Z$ term in the effective Hamiltonian. ZX or ZY errors are linked to the amplitude of a qubit influencing the phase of other qubits [689, 690]. The microwave pulse amplitude controls the rotation angle, and its phase adjusts the axis of the gate rotation operation. This makes it possible to create T, S and even R gates with an arbitrary phase. These R gates are used only in NISQ systems since they can't be handled fault-tolerantly, and are created in FTQC QPUs with combining Clifford (H, X) and non-Clifford gates like the T gates, which is itself generated by magic state factories and teleported on target logical qubits by lattice surgery or with transversal gates which we described in the quantum error correction part of this book. These gates can be optimized by modulating the pulsation in an optimal way with the capacity to generate single-qubit gates in 1 ns, against a current minimum of around 20 ns [691]. In practice, two arbitrary waveform generators create a wave form for "in-phase" and "quadrature" (I and Q) signals which are two microwave pulses that have the same (local-oscillator originated) frequency and are 90° out of phase, as shown in Figure 33.

The I signal is a cosine waveform and the Q signal is a sine waveform. These signals are combined in the mixer to create a pulse signal with an arbitrary phase depending on the relative amplitudes of the I and Q waveform signals [693]. The mixer then adds the local oscillator signal to the resulting signal. Another option consists of mixing the LO signal separately with the I and Q signals and then merge the resulting signal, removing unwanted spurious frequency components [694].

At 5 GHz, an LO pulse lasts 0.2 ns. Most single qubit gates last at least 10 to 20 ns. It means in that case that a generated microwave packet contains about 50 to a hundred 5 GHz photonic pulses shaped by their wave form. Microwave pulses generated at ambient temperature are progressively attenuated and filtered at every stage of the cryostat so that only a couple hundred microwave photons reach the qubit.

The attenuators eliminate photons proportionally to the cooling budget available at each cold plate stage. There are many investigated ways to tune and calibrate the pulse shapes to minimize single qubit error rates, including techniques involving deep learning [695].

Qubit designers must manage complicated trade-offs with regards to single qubit gate times as "*increasing the fidelity of single-qubit gates requires a combination of faster pulses and increased qubit coherence. However, with resonant qubit drive via a capacitively coupled port, these two objectives are mutually contradictory, as higher qubit quality factor requires a weaker coupling, necessitating longer pulses for the same applied power*" [696, 697]. But the slowest gates are the two-qubit gates which are about 10 times slower than single-qubit gates in many designs.

Qubit gate drive requires at least one to two wires per qubit which can quickly be cumbersome as you exceed a hundred physical qubits. There are two potential options to get rid of this cabling. One consists of using qubit drive frequency multiplexing in the microwave regime [83] and the other, to convert microwaves to optical photons that are multiplexed and transferred in an optical fiber and then demutiplexed near the qubit chip [84]. Some commercial companies like Viqthor (France) are working on it, but it's not available yet.

Two-qubit quantum gates are realized with a coupling circuit positioned between the two qubits, which can be a simple capacitor or a dynamically controllable system, *aka* a tunable coupler. This coupling is managed with an intermediate qubit in Google's Sycamore processor and their equivalents in China. IBM was using cross-resonance gates in its 127-qubit Eagle generation but ended-up adopting tunable couplers in its Heron generation launched in December 2023 and subsequent chips like Nighthawk, announced in 2025. One concern is to have short two-qubit gate times. They were historically about one order of magnitude slower than single qubit gates but nowadays, they can be short, down to about 20 ns, depending on the qubit designs [145].

Two-qubit gates have different implementations depending on the gate type. With the old IBM cross-resonance CNOT two-qubit gate with fixed frequency qubits, the control qubit was sent a microwave pulse at the frequency of the target neighboring qubit. Variants use pulses sent to both qubits [698]. The most common CZ gate implements a conditional phase shift with no energy exchange between the related qubits. There, a short microwave pulse briefly changes the control qubit's frequency, which modifies its interaction with its neighbor target qubit. The iSWAP gate, used by Google in one of its Willow 105-qubit chips, brings the related qubits into exact resonance and uses energy exchange. iWAP gates using a double-transmon coupler were theoretically designed by Hayato Goto from Toshiba in 2022 [699], then architected by Kentaro Kubo and Hayato Goto in 2023 [700], and then experimented in 2026 [701, 702].

It is also possible to create CZ gates with arbitrary phase, but again, only for NISQ QPUs [703]. Some academic setups also support native three-qubit gates like CCZ, iToffoli or the Fredkin gate [704, 705].

Qubits readout depends on its type. With transmon qubits, a resonator is coupled to the qubit. It transmits a microwave pulse in a resonator that is coupled with the qubit using microwave reflectometry. The qubit state slightly affects the resonator frequency and phase. These readout microwaves are usually amplified in several stages. The method is called "dispersive readout" using a dispersive cross-Kerr coupling between a qubit and its readout resonator, where for a fixed microwave drive frequency, the resonance frequency of the waveguide resonator shifts depending on the qubit measured state [706, 707] (Figure 34). On top of that, a Purcell

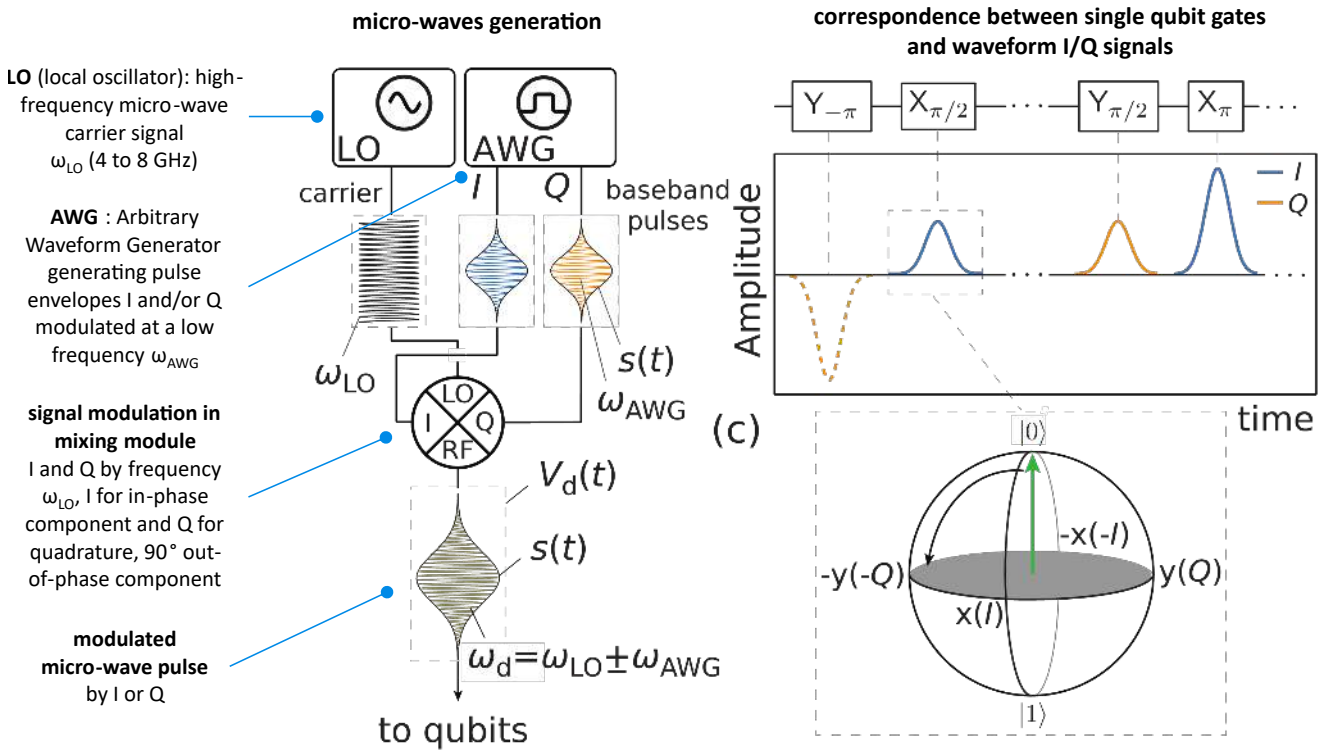

Figure 33: Qubit drive microwaves generation. LO stands for local oscillator which generates a stable tone pulse that is then merged with the waveform generated by the AWG in phase (I) and quadrature (Q) in the mixer. In 2026, Will Oliver's MIT team proposed a theoretical framework to add frequency modulation in the pulse generation to drive fixed frequency qubits, to improve single qubit and two-qubit gate fidelities [692]. Source: [584]. Captioning by Olivier Ezratty. 2021-2025.

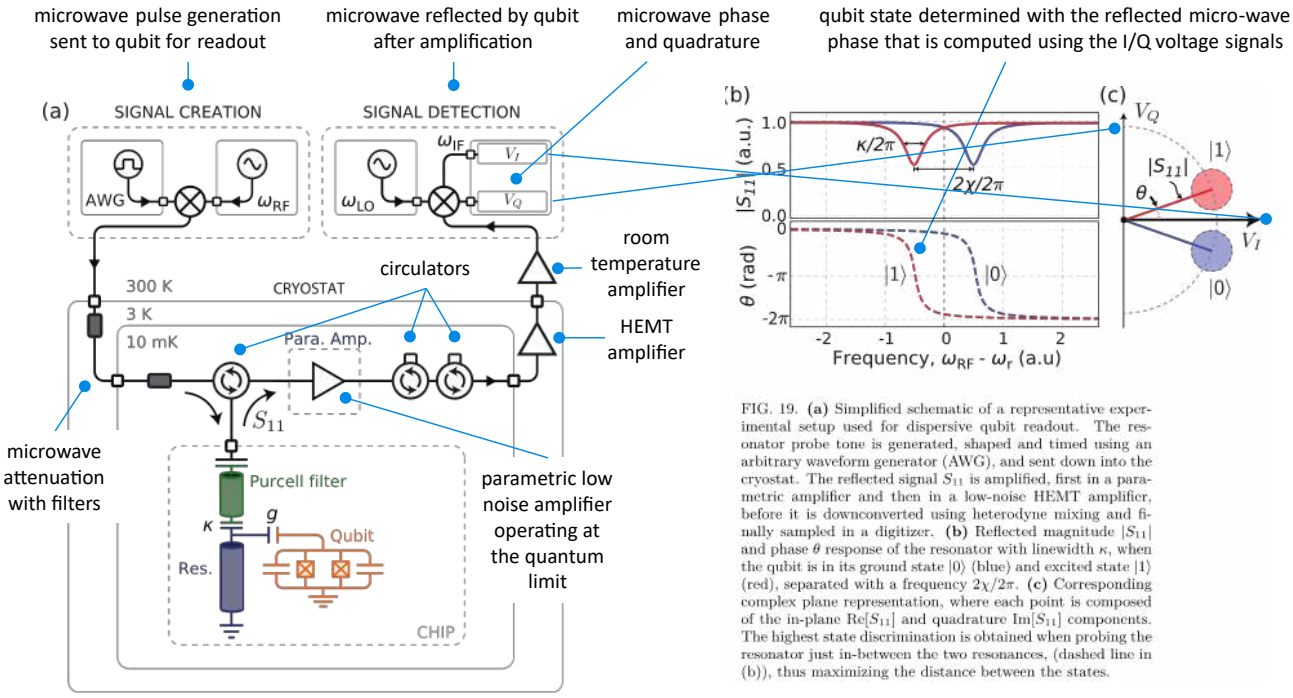

FIG. 19. **(a)** Simplified schematic of a representative experimental setup used for dispersive qubit readout. The resonator probe tone is generated, shaped and timed using an arbitrary waveform generator (AWG), and sent down into the cryostat. The reflected signal S_{11} is amplified, first in a parametric amplifier and then in a low-noise HEMT amplifier, before it is downconverted using heterodyne mixing and finally sampled in a digitizer. **(b)** Reflected magnitude $|S_{11}|$ and phase θ response of the resonator with linewidth κ, when the qubit is in its ground state $|0\rangle$ (blue) and excited state $|1\rangle$ (red), separated with a frequency $2\chi/2\pi$. **(c)** Corresponding complex plane representation, where each point is composed of the in-plane $\mathrm{Re}[S_{11}]$ and quadrature $\mathrm{Im}[S_{11}]$ components. The highest state discrimination is obtained when probing the resonator just in-between the two resonances, (dashed line in (b)), thus maximizing the distance between the states.

Figure 34: Superconducting qubit readout process. Source: [584] and caption adapted by Olivier Ezratty. 2021-2025.

low-pass and high-pass filter is used to protect the qubit resonator from readout resonator back-action on the qubit.

The dispersive readout and its Purcell filter suppress spontaneous emission through the readout line near the qubit frequency while preserving transmission near the resonator readout band at ω_r [708]. It amplifies the outgoing signal with the lowest added noise (near the quantum limit). The readout also creates a differentiated phase in the reflected microwave that is analyzed

after demultiplexing which generates the in-phase and quadrature signals (I/Q). Measuring the phase of the reflected microwave determines the collapsed state of the qubit after measurement without destroying it. It is a QND (quantum non demolition) readout.

One first stage can use a low-noise superconducting Josephson Parametric Amplifier (JPA) or Traveling Wave Parametric Amplifier (TWPA) operating at the quantum limit, then with a high electron mobility transistor (HEMT) amplifier running at the 4K stage and, at last, with a Low Noise Amplifier (LNA) running at room temperature.

Finally, the amplified microwave is converted in digital format with an ADC (analog to digital converter) and analyzed by a FPGA circuit to identify the qubit basis states $|0\rangle$ or $|1\rangle$ with a microwave phase analysis. The result is then exploited by some classical computer that will run some error correction code and drive other qubit operations afterwards. Frequency-based multiplexed readout can be achieved to simplify the wiring exiting the qubit chip. The readout microwave is modulated with a higher frequency than the quantum gates frequency, above 6 GHz. Other readout techniques are considered, such as the activation of qubit fluorescence. It is done by jumping from the $|0\rangle$ to the $|2\rangle$ state of the qubit, the transition to the $|1\rangle$ state not being possible with the fluorescence excitation photon [709].

Time-wise, superconducting readout is done in three steps: sending the pulse on the resonator (20 to 50 ns), the readout chain state discrimination including signal amplification and processing (50 to 200 ns) and then, the resonator ring-down, to let it decay and empty its photons (50 to 100 ns). The main trade-off here is leakage vs readout time. Some alternatives are investigated to implement a faster discrimination stage like the "bang-bang readout" theoretical proposal by Caltech in August 2026 [710] and some fine tuning proposed by Yasunobu Nakamura et al. in Japan in August 2026 as well, which could enable 98 ns readout times [711].

Qubit readout generates its own noise and errors, which can for example come from transmon ionization [675]. Many techniques could help reduce this noise, which can be particularly detrimental to mid-circuit measurements that are used in quantum error correction codes. One, developed at ETH Zurich and Institut Quantique at Sherbrooke University dynamically reduces the qubit-resonator detuning and increases the dispersive shift by bringing the qubit frequency closer to the readout resonator's frequency using a flux pulse. It increases the signal to-noise ratio (SNR) and assignment fidelity, reducing the single-shot assignment error to 0.25% [712]. Later, Sherbrooke University researchers improved the method by using some nonperturbative cross-Kerr interaction with coupling a qubit and a resonator via a Josephson junction. It removes the need for a Purcell filter and supports readout with fidelities exceeding 99.99% [713]. There, you need to optimize the number of photons used in the readout process [714]. One technique devised at RIKEN consists in using squeezed (microwave) light to improve SNR (signal noise ratio) [715]. Another one, from Google AI, associates predictive and heuristics data models [716], which sits in the more general machine learning assisted readout techniques field [717, 718]. A proposal from Yale and Cornell Universities is to increase the readout frequency up to twelve times the transmon frequency, to achieve QND measurement fidelity of 99.93% with low leakage probability. Readout is done at 9.227 GHz for a transmon running at a very low frequency of 0.758 GHz with a side effect of creating slow gates [719].

The current superconducting qubit readout technique is quite complicated with its digital-to-analog and analog-to-digital conversion processes, and their significant classical overhead, which becomes problematic when several hundred or thousand physical qubits are needed to build just a single logical qubit. One other issue is the size of the resonator, which is the largest artefact in a superconducting qubit [720]. Readout speed is another concern, with potential solutions to shorten it, which is of paramount importance for error correction [721]. There's a trade-off to make there: qubit readout is too slow when the used microwave photon numbers is low and if you increase it, the measurement becomes non-QND and can generate leakage errors.

Alternative Purcell filter designs

Even in the narrow field of Purcell-filter design, progress continues [722–725]. Alternative designs use a Purcell filter based on capacitively and inductively coupling a quarter-wavelength readout resonator and a filter resonator [726]. Also, Heng Fan et al. in China proposes to use frequency-tunable nonlinear Purcell filters made with a SQUID containing two Josephson junctions. It yields a readout fidelity of 99.3% without using a quantum-limited amplifier (JPA, TWPA) but at the price of a more complicated design and control [727, 728]. In 2026, Stefan Filip et al. from TUM and WMI in Munich moved the filter into a 3D flip-chip stack, resulting in a flat 1 GHz passband centered at 7.68 GHz and more than 45 dB suppression at typical qubit frequencies [729].

Thus, arises the interest of other tested approaches which would generate a 0/1 output in a simpler manner. One technique being considered is the activation of qubit fluorescence, done by jumping from the $|0\rangle$ to $|2\rangle$ state of the qubit, the transition to the $|1\rangle$ state not being possible with the fluorescence excitation photon. But it is probably destructive of the qubit state (non QND). Also, single microwave photon detectors are also tested [730–732] as well as cryogenic detectors using some microwave to photon conversion [733] and using an on-chip bolometer and DC current readout

still requiring some parametric amplifier [734]. These techniques have a much lower overhead but have yet insufficient readout fidelities to be considered in commercial QPUs. Readout fidelity can also be improved with the use of reinforcement learning [735].

Finally, another option would be to use some cryogenic on-chip qubit readout based on a Josephson digital phase detector (JDPD) associated with single-flux quantum (SFQ)-based digital circuitry, allowing fast and high-fidelity readout that is turned into a digital output directly at the mK stage [82].

Connectivity is an important feature of a quantum processor. The more qubits are directly coupled, the fewer routing SWAPs are usually required. Gate teleportation can also realize non-local logical operations when an entanglement resource is available [87]. IBM's 156-qubit Heron uses a heavy-hex lattice with 1-to-2 and 1-to-3 connectivity, while the 120-qubit Nighthawk family introduced in 2025 uses a square lattice with up to four nearest neighbors and 218 tunable couplers. The separate experimental **Loon** architecture adds 2 C-couplers per qubits for non-nearest-neighbor links, with up to degree-6 connectivity required by IBM's bivariate-bicycle qLDPC architecture.

Improving qubit connectivity relies on the use of multiple metal layers connectivity chips that are connected to the qubit chip with through-silicon vias (TSVs) vertical connectors [736]. The most recent designs from IBM and the MIT Lincoln Labs have between 3 and 7 metal layers. Another design is tested at IMEC using a special arrangement of resonators [737]. Researchers in China are also working on long-range qubit interconnect within chips [738]. Finally, an even more sophisticated approach uses a qubit reconfigurable connectivity router, as proposed in [739–742]. In 2025, William Oliver's team from MIT Lincoln Labs created a Hardware-Aware Layout runtime-efficient heuristic algorithm that automates and optimizes qubit placement and routing in multi routing layer chips with optimizing them for various error correction codes like the Gross bivariate bicycle code used by IBM [743]. It solves a graph optimization problem.

Characterization and calibration. These tasks are important to determine the actual performance metrics of superconducting qubits and calibrate their drive, particularly for implementing single and two-qubit gates as well as readout [744].

Digital simulations. Some software solutions are available to simulate the physical behavior of superconducting qubits at a low level. Among these, **CircuiQ** is a proposal from the MIT, ParityQC and the University of Innsbruck with the participation of Benoît Vermersch (LPMMC, Grenoble) [745]. It is a Python open-source toolbox that can be used for analyzing superconducting circuits at the physical level, using their Hamiltonian. It can help estimate the qubits T_1 under various noise mechanisms. There are other similar software packages like **scqubits**, developed by researchers from Northwestern University and **SQcircuit** from Stanford [746, 747].

1.3.4 Setups

In current state-of-the-art systems, the cryostats housing superconducting qubits are filled with many cables and microwave attenuators driving the qubits and with first stages amplifiers used in the qubits state readout [748] (Figure 38).

Implementing quantum error correction will require hundreds to thousands physical qubits per logical qubit, a number that depends on several parameters like the physical qubit fidelities, their connectivity, and the supported circuit size which can range between 10^6 to 10^{19} depending on the algorithms. Quantum chemical simulation algorithms are particularly demanding here. [42]. It will create significant challenges for scaling up the architecture at least, with the existing cabling and external microwave generation and readout systems. Thus, the need for cryogenic electronics and miniaturized microwaves coaxial cabling that we will investigate in the quantum enabling technologies section of this book.

With usual error correction codes like surface codes that implement fault-tolerance corrections, the key determinant of physical qubit overhead is also the number of T gates in the algorithm since these gates are the most expensive to correct. It will create significant challenges for scaling up the architecture at least, with the existing cabling and external microwave generation and readout systems.

Digital-to-analog converters, *aka* DACs and Analog-to-Digital converters convert microwaves at room temperature and handle a very large volume of outbound or inbound data of 8 to 14 Gbits/s as shown in the diagram in Figure 35 corresponding to Google's Sycamore. The controller processes this aggregate stream in real time. Whether the raw data are retained depends on the experiment, the calibration workflow and the control architecture.

The electronics used in research laboratory equipment is illustrated with the example in Figure 37 of a configuration used to test a 5-qubit superconducting chip in 2015.

It uses classical off-the-shelf equipment from **Rohde & Schwarz** or **Tektronix**. These external generators are appreciated for the quality of the microwave pulses they produce. For a larger number of qubits, multiple microwave generators are used coming from vendors like **Zurich Instruments**, **Qblox** and **Quantum Motion**. Others, like **SEEQC**, are attempting to miniaturize all or part of these components with superconducting electronics which have a much lower power drain and can work within the cryostat.

Superconducting qubits fidelities are not best-in-class compared to trapped ions but not that far as they made

some progress since 2022 in commercial systems. It may also decrease with the number of physical qubits. There is some progress being made to reduce qubit noise. It has several origins such as charge fluctuations, random electrons and materials impurities. Fidelity is currently not high enough to implement error correction codes. Some methods are also created to improve readout fidelity.

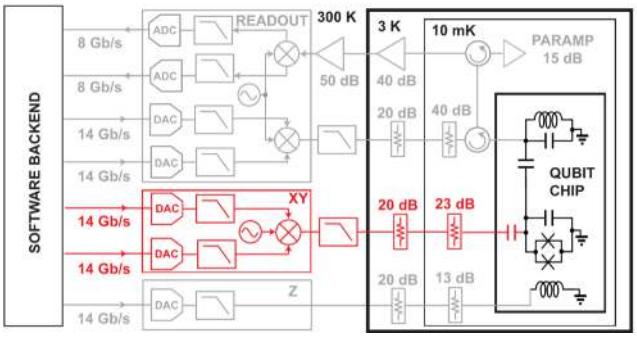

Figure 35: Google Sycamore's qubit control and readout architecture. Source: Google, 2019.

A team of Canadian and American researchers proposed in 2015 a miniaturizable optical measurement [749]. A variant came out in 2018 by Robert McDermott of the University of Wisconsin-Madison, with the objective of improving measurement fidelity to 99% [750]. We are now better than that.

The size of superconducting qubits is in the micron range, making it difficult to create large chips with millions of qubits. Miniaturization always seems possible, but it is difficult to manage because the quality of the superconducting qubits seems to decrease with a smaller size [113, 114].

Therefore, vendors like IBM, plan to create chips not exceeding 100 to 200 physical qubits and then connect several of these chips with microwave guides and/or entangled photonic links associated with microwaves to/from optical photons transduction techniques. These various quantum processor interconnect technologies currently have a very low TRL (technology readiness level) due to low efficiency, at around 1% end-to-end conversion efficiency. Fault-tolerant networking generally requires a much higher end-to-end efficiency, whose exact value depends on the protocol, the heralding scheme, detector performance and the code error budget, but at least way above 50% [86].

1.3.5 Manufacturing

Superconducting qubits are electronic circuits built with techniques that are not that far from how classical analog circuits are being produced like in the radar and electronics markets, with some similarities with digital electronics, *aka* CMOS chips.

We will describe later the specifics of the manufacturing of superconducting qubits. Most theses from superconducting labs contain a description of the manufacturing techniques being used although it changes over time [398].

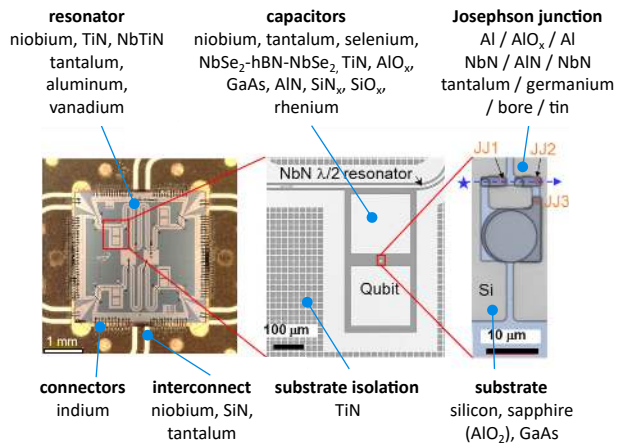

Figure 36: The various components and materials used in a superconducting qubit. Source: [751]. ⓒ Olivier Ezratty, 2022-2026.

Materials used for manufacturing superconducting qubits are different from CMOS chips. It includes:

- Aluminum for the Josephson junction, at least for the dielectric and sometimes, resonators [752]).
- Aluminum nitride for the junction sandwitched between niobium nitride with high operating temperature reaching 300 mK [753].
- Granular aluminum (grAl) is a highly disordered superconducting material made of nm-sized pure crystalline aluminum grains separated by thin amorphous aluminum oxide barriers. It operates as a dense, random three-dimensional network of nanoscale Josephson junctions. It can be used in resonators [754].
- Boron, as hexagonal boron nitride (hBN), used as a Josephson junction dielectric [755, 756].
- Tin (Sn), as a junction electrode material, investigated as an alternative to the Al/AlO$_x$/Al stack [757]).
- Tantalum, replacing aluminum in capacitor pads and resonator films, while the junction itself can remain Al/AlO$_x$/Al, for capacitors, resistors and resonators [78, 758–770] (Figure 36. It seems that tantalum is not that better compared to niobium [771] or just slightly better to reduce the effects of TLS [772]. A major source of loss is the presence of two-level systems (TLSs) in the surface tantalum oxide. Stanford University proposed in 2024 to avoid oxide formation by encapsulating the tantalum with noble metals that do not form native oxide [79].
- Tantalum nitride (TaN) can have multiple usages including for the non-superconducting barrier in Josephson junctions [773].

- Titanium nitride (TiN) for capacitors and resonators [774], with a better quality factor, and sometimes even for the Josephson junction [775, 776].
- Germanium, sometimes used in the Niemeyer–Dolan bridge from the Josephson junction [777], Figure 39.
- Niobium for capacitors and resonators [778–780] and sometimes the Josephson junction [781]).
- Vanadium for resonators [782].
- Selenium, as $NbSe_2$, associated with niobium and boron nitride in capacitors.
- Rhenium can also replace tantalum as shunt capacitor electrodes *aka* pads which are the large superconducting film patterned on the wafer substrate [783].
- Various organic resists and solvents are also used for the etching and evaporation process of the Josephson junction, like for the creation of a Niemeyer-Dolan bridge, which is a suspended resist bridge, and its removal after the etching process, during the lift off operation. The positive and negative resists are PPMA (polymethyl methacrylate), copolymer MMA/MAA, ZEP520A from Zeon Corporation (copolymer of methyl styrene and chloromethyl acrylate), SU-8 (bisphenol A Novolac epoxy resin) and HSQ (hydrogen silsesquioxane). They generate various contaminations that must be minimized [784, 785]. The main solvents used are acetone, IPA (isopropyl alcohol), methanol and MP (N-Methyl-2-pyrrolidone).
- Indium, for the chip connectors in so-called indium bumps.
- Silicon or sapphire (aluminum oxide) are the most common wafer substrate materials. GaAs is investigated in Taiwan due to its crystal structure matching the aluminum oxide structure [786]. Silicon-on-insulator is also an alternative wafer structure although specific techniques must be designed to remove parasitic losses between the silicon wafer and the silicon oxide layer [787].

3D chips are now commonplace, with at least a qubit chip on top of an interposer using the flip-chip technique [80, 789, 790], and a resonator and interconnect chip [791]. Future designs will interconnect several chips next to the other using a chiplet architecture [81]. As presented at the APS March meeting in Las Vegas in March 2023, the MIT Lincoln Labs also works on modified Dolan Josephson junction process flows. It is testing aluminum on silicon as well as connection using 7 stacked niobium routing layers using an interposer chip with TSV. It also showed good results with hydrofluoric acid treatments of the Josephson junction for cleaning surfaces, using aluminum on silicon substrates. These various advances still must be embedded in industry vendor processors.

While most deposition techniques generate polycrystalline structures [392], some are exploring the use of epitaxial deposition to create monocrystalline structures with CMOS-like manufacturing processes. IMEC already tested such processes avoiding lift-off and angled evaporation, all done with photolithography. They were part of the related EU project **MATQu** with CEA-Leti and others to build superconducting qubits on 300 mm wafers using existing CMOS fabs. IMEC was also testing the manufacturing of tantalum based resonators deposited on silicon [391]. CMOS-like superconducting qubits manufacturing is also tested at Fraunhofer EMFT in Germany on 200 mm wafers, with good output yields [792–794].

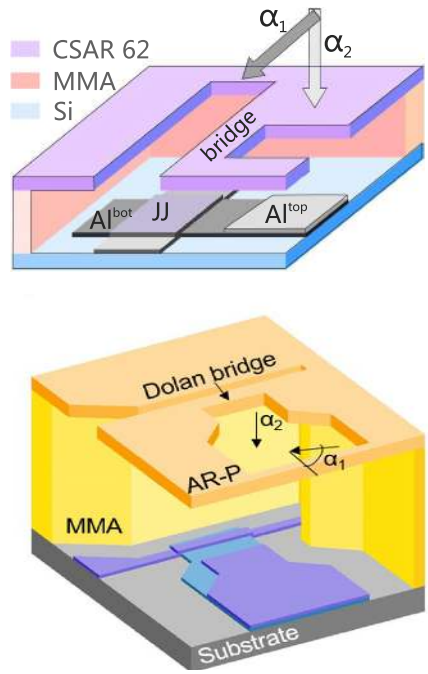

Figure 39: Two examples of Niemeyer–Dolan bridges, which are narrow suspended resist structures created during electron-beam lithography when manufacturing a Josephson junction. They are used in the double-angle shadow evaporation technique to define the tunnel barrier of a Josephson junction with good lateral precision. After the JJ is finalized, the bridge is removed with various solvents during the lift-off process. A Niemeyer-Dolan bridge is different from an airbridge which is a small superconducting metal arch that carries one on-chip line over another without touching it, with vacuum as the only separator in the gap [795, 796]. Sources: [797, 798]. See also [799]. Added in 2025.

Superconducting qubits miniaturization is an interesting area of research given they are currently quite large, mainly due to the size of their resonators. Coplanar-waveguide resonators often have an electrical length near one quarter of the guided wavelength at their resonance frequency, and compact lumped-element and slow-wave designs can reduce their footprint. It can exceed a size of 1 mm^2. Resonators could be as small as 0.04 mm^2 using special fabrication techniques [800, 801]. Similar efforts are undertaken to miniaturize capacitors with van der Waals materials ($NbSe_2$-hBN-$NbSe_2$) [802], using

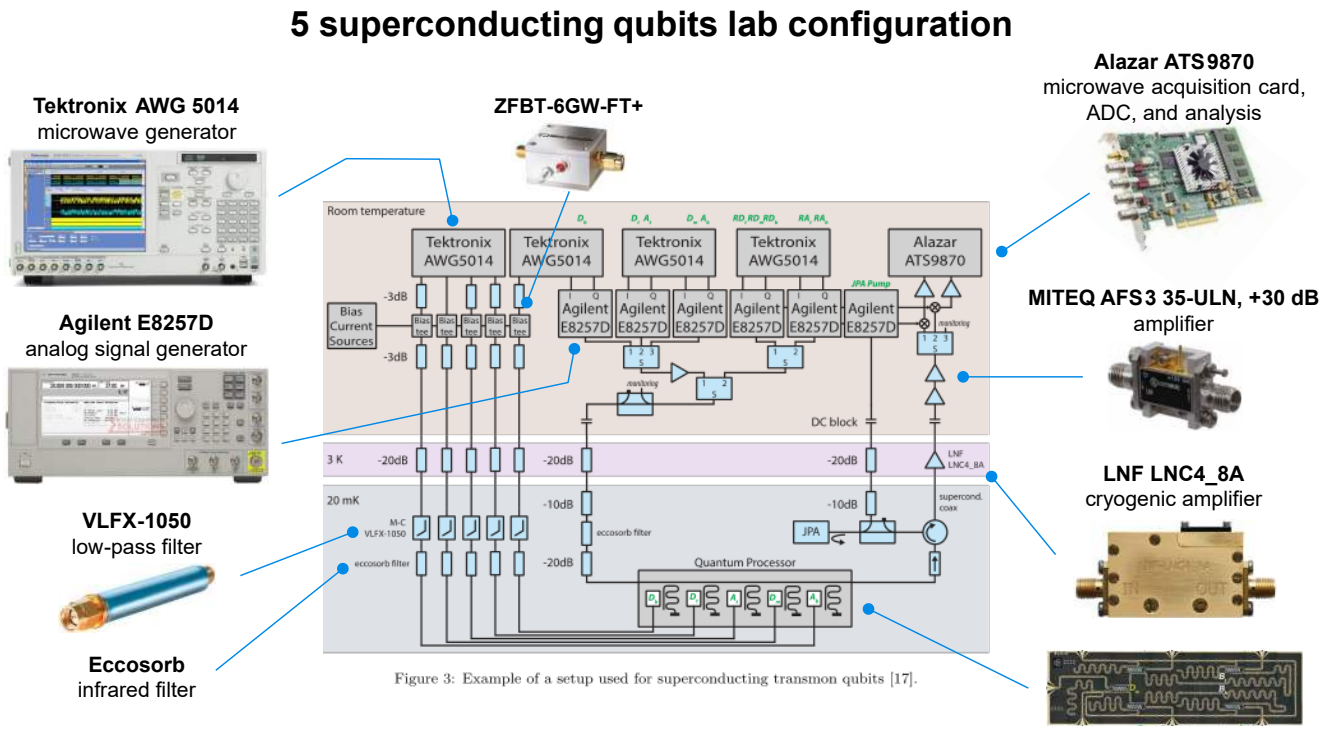

Figure 37: Superconducting qubits lab configuration. Source: [788]. I added visuals of the electronic components used in the configuration.

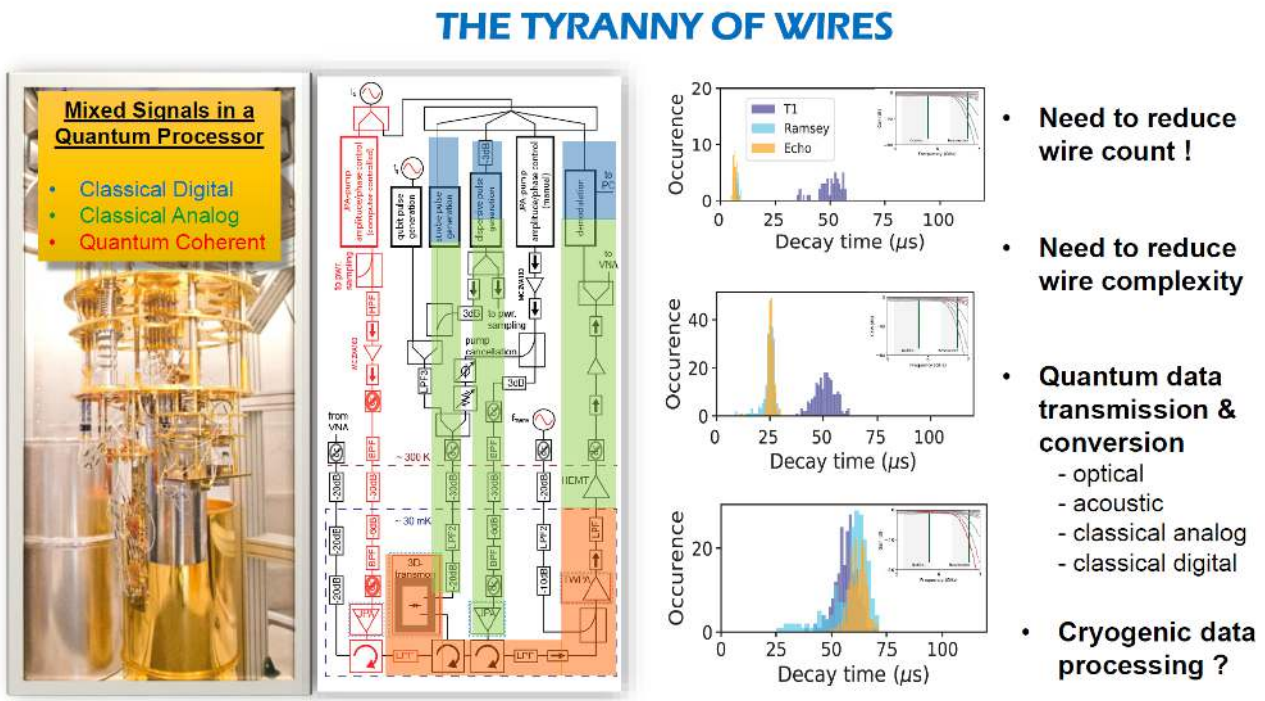

Figure 38: The tyranny of wires in superconducting qubits. Source: [748].

TSV (vertical "through silicon vias" traversing the chip) [803] and with parallel plate capacitors [804]. Another option would be to have remote resonators and an X-Y addressing scheme like with classical RAM, but with the inconvenience of serializing gate operations, and slowing down computing. It would route signals to the qubit resonators from the edge of the chipset, X and Y corresponding to two orthogonal edges. You would then polynomially reduce the number of resonators from N to $\sqrt{N}$ with N being the number of qubits of a square matrix layout chipset.

1.3.6 Research

A significant number of research laboratories are working on superconducting qubits all over the world. In the USA, at **Yale University** and **MIT** [805], in Europe and in Germany, in Sweden at Chalmers' **WACQT** [806], in France at the **CEA**, in Switzerland at **ETH Zurich**, at **VTT** in Finland [38] and in **Japan**. In 2019, VTT's goal was to support 50 to 300 superconducting qubits. VTT has its own circuit manufacturing unit with a 2600 m^2 clean room.

Other works aim at lengthening the coherence time of superconducting qubits, notably at Princeton in Andrew A. Houck's team [807]. Indeed, this coherence time of the order of one hundred micro-seconds (μs) is still quite limiting. It generates a constraint on the number of quantum gates that can be executed in quantum software, even if the accumulated errors become prohibitive before this limit threshold.

New records were broken in 2021 with 1.6 ms T_1 at Princeton and Sherbrooke University with a 0-π circuit (but with a 25 µs dephasing time, aka T_2) and 210 μs with transmon qubits at Yale [808, 809]. IBM reached the 1 ms T_1 barrier with one experimental planar transmon qubit in May 2021 as well (but the related paper is still pending). The best lab-level record was with a 1.48 ms T_2 coherence time on flux qubits at the University of Maryland in then Vladimir Manucharyan's team [810] (Figure 41). These records were obtained in small devices and have not yet been reproduced at processor scale.

Superconducting qubits lifetime record is still way above this, with 3D SRF cavities (for superconducting radio frequency cavities). These are developed by the DoE Fermilab and have a very high Q-factor. In 2020, they reached qubit lifetimes of about 2s with special materials design reducing the 2-level system losses. Fermilab researchers plan to implement qudits with these SRFs. The quoted equivalent of 63 to 128 qubits encoded in 9 SRF cavities is a Hilbert-space dimension count, not a set of individually controllable and error-corrected logical qubits. The measured observable is the cavity mode coherence time and the encoding dimension must be specified separately from any usable logical-qubit capacity. These cavities are bulky, the size of the device being about one meter long in Figure 40 [811–813]. Anna Grassellino's team proposed in August 2026 a modular 3D bosonic quantum processor architecture to assemble these qubits in 3D, but with an unclear computational benefit [814].

Other researchers look at implementing superconducting qudits with various means using three or four levels, but so far with gate fidelities well below those of the two-level encodings [386, 815–819]. Researchers from the University of Rochester even proposed to use 8-level qudits on which a spin-7/2 system is mapped [820]. A record of a 12-level qudit was achieved in 2024 by the University of Rochester [821]. Research is also going on in that domain using Schrödinger cat states at UC Berkeley [822].

Figure 40: The huge SRF superconducting qubits from the DoE Fermilab. Source: [811].

However, superconducting qudits are more subject to decoherence than qubits due to increased loss channels, noise sensitivity, and crosstalk, requiring the use of some dynamical decoupling protocols [823].

Other researchers work on using various qubits materials like titanium nitride and tantalum on sapphire substrates, at Princeton, ENS Lyon and Alice&Bob among other locations. These are used in complement to the Al/AlO/Al Josephson junctions, for various other parts of the qubit circuits (isolators, capacitances, resonators) [824]. But tantalum easily oxides, which may require the addition of some isolating layer like with magnesium [825]. Niobium also oxides and may also require some isolation layer [826].

The Quantronics team at CEA-Saclay uses transmons for its quantum circuits, but now explores another route based on high coherence impurity spins in insulators for making qubits, with superconducting quantum circuits for controlling them. The rationale is that the electro-nuclear spin levels of such systems may indeed provide more robust qubits for which quantum error correction could be more easily manageable than for transmon qubits.

Other research conducted at the CEA associates superconducting qubits with NV centers, linked by microwaves, to be used as quantum memory as well as a means of more precise readout of superconducting qubits. NV centers spins can serve as quantum memory thanks to a spin coherence time that is 1,000 times longer than that of superconducting qubits (100 milliseconds vs. 100 microseconds). Another field of research is the coupling of superconducting qubits with nuclear spins (instead of electron spins, on phosphorus or bismuth nuclei) via electron spins.

As with many solid-state qubits, one of the key research goals is to transform these microwave photons into photons in the visible/infrared band to allow their long-distance transport, in particular via fiber optic-based telecommunication, which would become the basis of distributed quantum computing [828].

There is another interesting field of research aimed at simplifying qubit readout that may avoid the burden of parametric microwave amplification and circulators at the 15 mK stage. One of these uses microwave photons counting and Josephson photomultipliers (JPM) that are embedded directly in the qubit chip [829, 830]. It

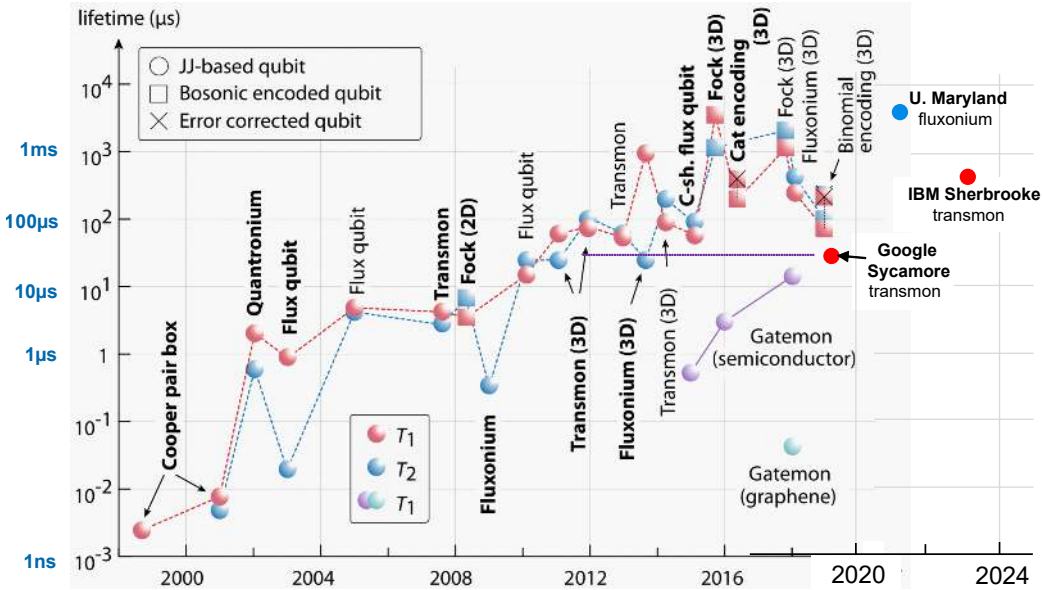

Figure 41: Logarithmic evolution of superconducting lifetime over time. Source: [827]. Updated in 2023.

has some shortcomings to overcome like crosstalk and loss of qubit fidelity over time.

China. Several academic teams in China are working on superconducting qubits. Haifeng Yu's BAQIS team in Beijing, Jian Wei-Pan's team in Hefei, Dapeng Yu's team in Shenzhen, and others elsewhere, working on fluxonium qubits. Keeping track of these QPUs is not an easy task. In May 2021, BAQIS team obtained a 300 μs T_1 with a transmon qubit [831]. The same year, Jian-Wei Pan's team created a 66 superconducting qubits QPU and claimed having reached another quantum advantage. In this **Zuchongzhi** 2.1 system, they reproduced the Google supremacy experiment with a 2D array of qubits with 13 additional qubits (66 vs 53), using 110 tunable couplers [832]. Their misleading communications mentions 176 qubits, which is not the way it is accounted for with Google and now IBM. We count only the data qubits, not the tunable couplers. Their qubit fidelities were not best-in-class with 99.86% for single qubit gates, 99.24% for two-qubit gates and 95.23% for qubits readout, on top of a rather low T_1 of 30.6μs. In their experiment, though, they did use only 56 of their 66 qubits, showing high fidelity variability [833]. In September 2021, Pan's team used 60 qubits on 24 cycles with an improved readout fidelity of 97.74% [834]. Pan's researchers also implemented in 2022 some quantum neuronal sensing application of quantum many-body states in this QPU [835]. In June 2023, Zuchongzhi-2 was released on the cloud by QuantumCTek, always with its misleading 176 qubit claim and with CZ entangling gates (Figure 42).

In November 2022, China research teams from Hangzhou, Beijing and Hefei launched two superconducting qubits QPUs with 121 and 36 qubits (11x11 et 6x6). The physical qubits worked with subsets of 68 qubits and 20 qubits with T_1=109.8 μs and T_2=17.9 μs (68 qubits) and T_1=137.5 μs and T_2=16.4 μs (20 qubits). Their single-qubit gates fidelities were respectively 99.87% and 99.91%, and two-qubit fidelities are 99.4% (see charts in Figure 43). These qubits were used to create topological logical qubits using toric quantum error correction codes. using non-abelian anyons. These teams are working on large scale and long range tunable couplers using capacitively connecting pads and a flip-chip bonding process. It implements CZ coupling gates with 96.2% fidelities. This coupling can be capacitive or inductive [836]. In September 2024, the same team published a paper showcasing two-qubit gate fidelities of 99.68% on a 1D 18-qubit line in this 121 qubit chip [837], and in 2025, used if to some time-crystalline order simulation [838].

Haifeng Yu's team from BAQIS is working on improving single qubit gates errors to a 10^{-4} record [839] and, to reduce crosstalk errors [840]. Thanks to calibration, it also exceeded a record 99.9% CZ two-qubit gate fidelity in 2026 with 84 qubits, although with a media fidelity of 99.25% [841].

Dapeng Yu's Shenzhen team is working on stabilizing multiple qubits entangled states [842].

CAS created in 2024 a prototype 504-qubit QPU named Xiaohong to be used as a testbed of enabling technologies by QuantumCTek with probably very bad fidelities. It is a similar approach than the one IBM pursued when designing Osprey (433 qubits) and Condor (1,121 qubits) mainly for the test of scalable control electronics and cabling [843]. Later in December 2024, the Xiaohong was due to be integrated in China Telecom's Tianyan-504 QPU cloud platform (link). It happens that this QPU has seemingly no entangling gates according to Brian Siegelwax [844]! On the Tianyan platform, the Tianyan-176 is the Zuchongzhi-2.

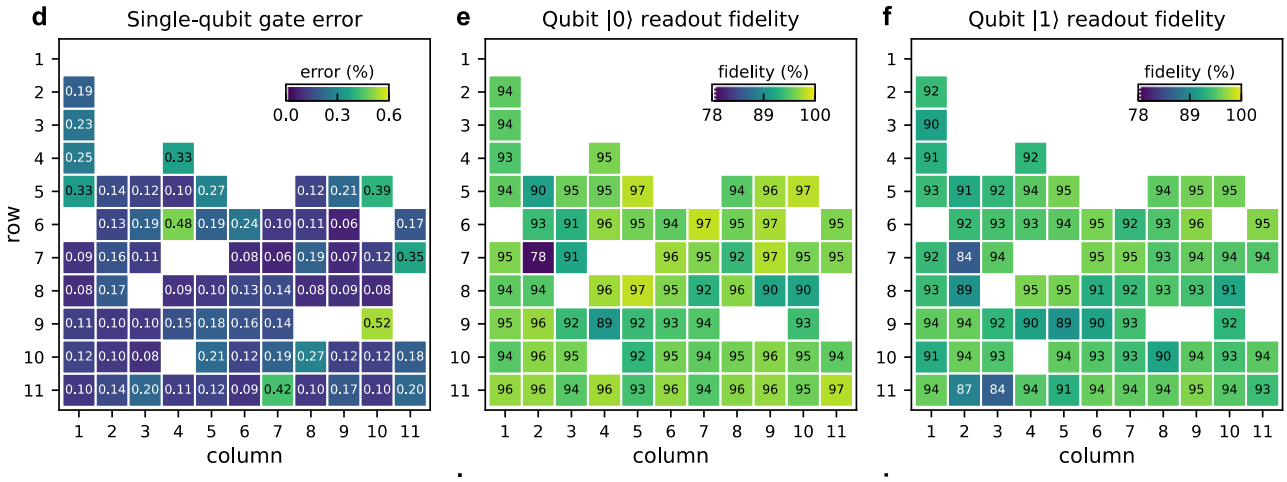

Figure 43: China's 68 qubit fidelities variability, from a 121-qubit QPU. Source: [846].

Figure 42: A rare glimpse on a China Zuchongzhi 2.1 QPU in 2023. Source: [845].

In December 2024, Pan's team published a paper on an experiment on a single transmon superconducting with a record qubit readout fidelity of 99.9% [847], but not an average one. At the same moment, Pan's team released the Zuchongzhi 3.0 QPU with 105 physical qubits, the same number of qubits than Google Willow. Their fidelities were just below Google's Willow: 99.90% for single qubit gates, 99.62% for two-qubit gates and 99.18% for readout. A bit like Google, they then published a "quantum supremacy" experiment using some cross entropy benchmark, claiming it was million times faster than Google Sycamore [131]. Meanwhile, Google had updated its experiment with Google Willow the same month with more physical qubits, superseding the claimed record under the stated XEB comparison, although the two experiments used different systems and parameters [848]. In December 2025, Pan's team implemented an experiment similar to Google's Willow in 2024, correcting a logical memory qubit with some leakage detection-based QEC on Zuchonzhi 3.2, using 97 out of 107 qubits and a distance 7 surface code [849]. It was extended in 2026 with an experiment of state routing between different surface code patches on the same 107-qubit processor [850]. In 2026, Ying Li's team in Beijing did experiment lattice surgery to connect two distance-3 surface code logical qubits on a 125-qubit experimental processor [851].

China's BAQIS Dongling superconducting qubits QPU released in 2025 has 104 functional qubits out of 169 (13*13) [852].

Heng Fan's team from Beijing and Hefei published in October 2024 the results of the characterization of a 20 and 21 qubits chip arranged in 1D with record fidelities thanks to improved tunable couplers: CZ and iSWAP gates with fidelities of 99.61% and 99.82%. A CPhase Pi/8 (T) gate has 99.94% fidelity on the 21 qubit chip [853]. Heng Fan's team also collaborates with German academics. It released in 2025 a 78 qubits and 137 couplers analog superconducting QPU, the Chuang-tzu 2.0 [854].

Jun-Jie Wu's team from the National University of Defense Technology is running characterization of Ramsey fringes in a 5-qubit chip using Pan's and Google's designs [855].

Finally, Lei Du's team from Tianjin University is working on bosonic codes superconducting qubits [856].

1.3.7 Vendors

IBM

USA, 1911

IBM is one of the few major players in the IT world that has been investing in fundamental research for a very long time in quantum computing. It runs one of the largest and longest-running full-stack quantum-computing programs, having focused on superconducting qubits for a while. IBM started to develop quantum computers a while ago. In 2001, they could factor the integer 15 using Shor's algorithm using a prototype liquid state nuclear magnetic resonance (NMR) 7-qubit chip

[857]. In 2012, IBM created a 3-qubit superconducting chip [858]. Its commercial inroads in the quantum computing world started in 2016 with the launch of its Q Experience offering in the cloud with a 5-qubit QPU, now branded Quantum Experience.

Organization. IBM's quantum activity is driven by Jay Gambetta (Director of Research for IBM since September 2025) with researchers in their Yorktown, Poughkeepsie, Almaden, Ehningen (Germany), Tokyo, and Zurich labs, partnering with various American and universities in other countries including ETH Zurich and EPFL in Switzerland and the University of Tokyo in Japan. IBM has both the most significant full-stack physics, hardware, software tools and cloud R&D investment and strong market presence. It has several hundred researchers working in the domain, on top of field operations (sales, marketing, support, services) totaling about 1,000 people as of mid-2026. Their in-house manufacturing capacity at Yorktown Heights (research fab, 200 mm wafers) and Albany (industry fab, 300 mm wafers) in New York state enables them to prototype and produce most of the components needed to build their machines, particularly for their qubit chips and part of their control electronics. Their most visible outside vendor is Bluefors, with the XLD used in IBM System One and KIDE used in System Two. IBM is quite open and reliable, publishing roadmaps and roadmap updates, generally meeting their planned milestones (although with some subtle updates from time to time) and with a steady stream of open research publications showcasing their contribution to the complicated quantum computing field even though it sometimes looks like a difficult to assemble into a single picture.

In 2025, IBM announced a plan to invest $150B in the USA to "*America to Accelerate Technology Opportunity*", including $30B "*in research and development to advance and continue IBM's American manufacturing of mainframe and quantum computers*" over 5 years [859]. Data wise, it looked like business as usual. In 2024, IBM made a total revenue of $64B. It spends about $8B in R&D every year. So, $40B over 5 years. They also have SG&A expenses of about $20B per year (Sales, General and Administrative expenses). Times 5 makes $100B. In 2026, IBM then announced it would invest $10B over 5 years just on quantum technologies, with some of this amount being booked for potential acquisitions. This contains the $2B amount allocated to the creation of the subsidiary Anderon in Albany which will manufacture 300 mm superconducting wafers, including $1B of grant from the US Department of Commerce. This comes somewhat in reaction to the acquisition of Skywater by IonQ. The $10B amount is unprecedented and shows how serious IBM is with its superconducting qubit processors investment.

System One and System Two. After creating laboratory computers, IBM ventured into creating packaged ones when announcing the Q System One in January 2019 at the Las Vegas CES, initially a 20-qubit system. Its design was created with the design studios Map Project Office and Universal Design Studio (UK) and Goppion (Italy), a manufacturer of high-end exhibition devices for museums, which notably designed the protective device for the Mona Lisa in the Louvre Museum and the Queen's jewels in the Tower of London. Nowadays, some other quantum computing hardware vendors rely on designers as well to craft nice looking QPUs like Quandela. Others create just large white or black boxes (IonQ, Atom Computing).

The Quantum System One is 2.75 m wide, about the size of a D-Wave quantum annealer. In Figure 44, you can see the Quantum System assembly workshop. IBM is implementing a pre-industrial approach to the production of its quantum computers, despite their very limited capacities and low volume economics. The casing front contains the suspended cryostat while the back contains all the computing, electronics and cryostat compressor and pumps. These systems are also self-calibrating.

IBM introduced its System Two roadmap in May 2023. The system packaging is much bigger than System One, using a Bluefors KIDE cryostat with 9 compressors and 3 dilutions to accommodate several chips, with the cooling capacity to support thousands of physical qubits, and then, large racks for control electronics sitting around the KIDE (Figure 47). System One QPUs are progressively being retired in favor of System Two units, and future larger systems (Starlinq, Bluejay).

IBM targets 200 logical qubits and 100 million logical operations with Starling in 2029. Its public materials describe approximately 10,000 physical qubits, consistent with Figure 46, but this remains a roadmap estimate that depends on the fidelities actually reached by then [7]. This roadmap was announced in 2024 jointly with a U.S.-Japan $100M partnership over 10 years [860, 861]. In 2024, the plan was to build this 100,000-qubit system out of four 25,000 qubits clusters interconnected by photonic links. Each of these clusters would use three high-power dilution fridges connected through long range microwave interconnections. The announced partnership involves the University of Tokyo and the University of Chicago. There may be some connection with IBM Japan Research team working on control electronics, which plays an important role to slowly scale the energy consumption of these QPUs [862]. The University of Chicago is working on error correction codes and photonic interconnection solutions. The $100M partnership is spread over 10 years across the USA and Japan, meaning the University of Tokyo probably receives less than $5M a year. At last, IBM announced the creation of a quantum research laboratory in France in May 2024, was to host about 50 researchers by 2025 in charge of quantum software engineering. In 2026, IBM announced it was working with Cisco on the development of photonic interconnect, on top of transduction mechanisms between microwaves and optical photons.

In June 2025, this plan was updated with more details provided on Starlinq (2029) and Bluejay (2033).

Figure 44: IBM System One during assembly. The white cylinder corresponds to the casing hosting the Bluefors XLD dilution refrigerator. The whole system contains the whole compressor and gas-handling system supplying the dilution refrigerator with helium 3 and 4, as well as all control electronics. Source: IBM.

Figure 45: IBM System One with packaging, as installed since 2023 at Cleveland Clinic, Ohio, in the USA. Source: IBM. 2023.

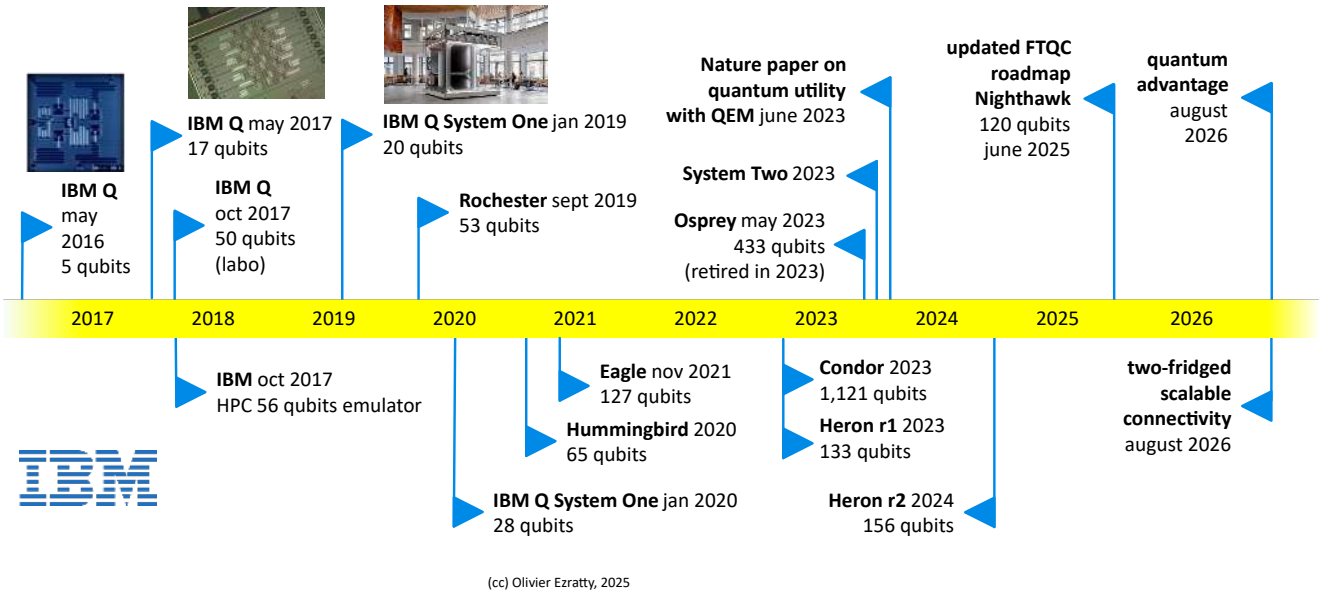

Figure 46: IBM quantum computing timeline. (cc) Olivier Ezratty, 2019-September 2026.

These systems will fit in a very large dilution fridge, looking like series of KIDE without doors connecting each "hexagon" with each other. This platform would enable them to use only microwave flexible couplers between chips instead of relying on photonic interconnect technology that would need some microwave to optical photons transduction.

Roadmaps. Since 2020, IBM has announced and updated its roadmap several times. In September 2020, IBM announced their plan to "scale-in" the number of qubits of their quantum computers [863–865] with a 127 qubits version ("Eagle") introduced in November 2021 [866], 433 qubits announced in November 2022 and online since May 2023 ("Osprey") and 1,121 qubits in 2023 ("Condor"). This roadmap was updated in May 2022 with the addition of new processors implementing a scale-out approach [867]. IBM's technology was then based on fixed frequencies transmon superconducting qubits. It was using cross-resonance two-qubit gates which applies a microwave drive to one qubit (the control) at the frequency of another qubit (the target), generating a ZX interaction that is mediated by a bus [868, 869]. Due to poor fidelities, with two-qubit error rates above 2%, both Osprey (433 qubits) and Condor (1,121 qubits) were retired and dismantled in 2023 to recover their spare parts (cabling, amplifiers, attenuators, cryostat) for other QPUs. Condor was even never really made available online. Another reason was IBM's shift to using tunable couplers based CZ gates in Heron, released in December 2023, which significantly reduced qubit crosstalk. But these take up some space on the chip. As a result, their 156-qubit Heron chip released around June 2023 was as large as an Osprey chip.

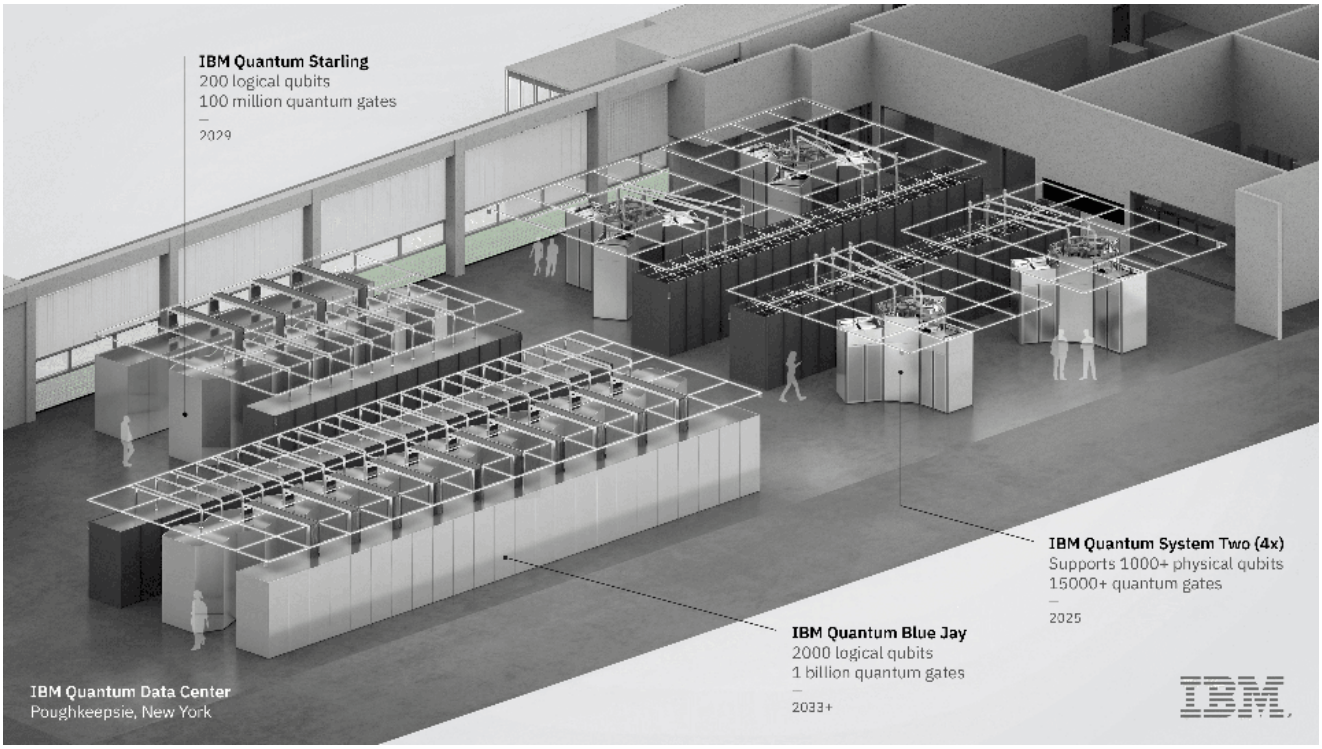

Figure 48: IBM Starling and BlueJay will support respectively 200 and 2,000 logical qubits by 2029 and 2033. Starling will require about 10,000 physical qubits. Source: IBM, 2025.

Figure 47: IBM Quantum System Two at Yorktown Heights, sitting in a showroom but being online in IBM quantum offering. Photo: Olivier Ezratty, February 2024.

IBM's 2022 roadmap update added a scale-out strategy with their QPUs on top of their scale-in roadmap announced in 2020 [172]. It was updated again in December 2023 [870]. Chips will be assembled in three-steps: first, Heron will be assembled in QPUs with many units running the same circuit in parallel, accelerating the thousands of runs that are necessary with NISQ systems algorithms. Second, Crossbill was to assemble three chips similar to Heron and accumulate 408 qubits in 2024. The plan is to tightly connect the chips with chip-to-chip short-range M-coupler qubit gates and packaged in a single multi-chip module, *aka* a chiplet. In March 2026, IBM even proposed to use some liquid metal coupling (in GaInSn, *aka* "galinstan"), which would enable easy defective chips replacement on chiplets [871].

Flamingo was to follow in 2024 with 1,092 qubits (7×156 Heron r2 chips) with three chip blocks interconnected through some longer range microwave-photonic link using flexible cables less than one meter long. Then, Kookaburra would assemble several blocks of three chips associating chip-to-chip micro-wave connectivity (M-couplers) and longer range microwave-based interconnectivity (L-couplers), plus quantum communication between distant qubits within the chip itself (C-couplers) (Figure 49).

The roadmap was again updated in June 2025, changing somewhat the chip scale strategy and adding a full-fledge FTQC roadmap covering all needs (error correction using the gross code, magic state distillation, etc.) (Figure 54).

Fidelities. IBM reached record fidelities in November 2022 with the 33-qubit Egret QPU, with two-qubit ECR gates fidelities of 99.66%, a result similar to what is now available with Heron with 133 and 156 qubits. They also improved coherence times on a regular basis within a class of systems processors (like Falcon for 27 qubits). Qubit readouts fidelity was also improved thanks to low noise amplifiers (QLA for quantum-limited amplifiers) [872]. IBM also continuously improve qubit physical properties [873], using laser annealing in their production [874, 875], with new materials design improving their purity and avoiding contaminations and computer aided design [876], and with improving chip vacuum isolation during its assembly [877]. Metallic superconducting nanowires could also be controlled by applying a moderate voltage to a nearby gate electrode. Switches using this effect would require very little power and could mitigate the well-known negative impact of phonons on the coherence of superconducting qubits [878].

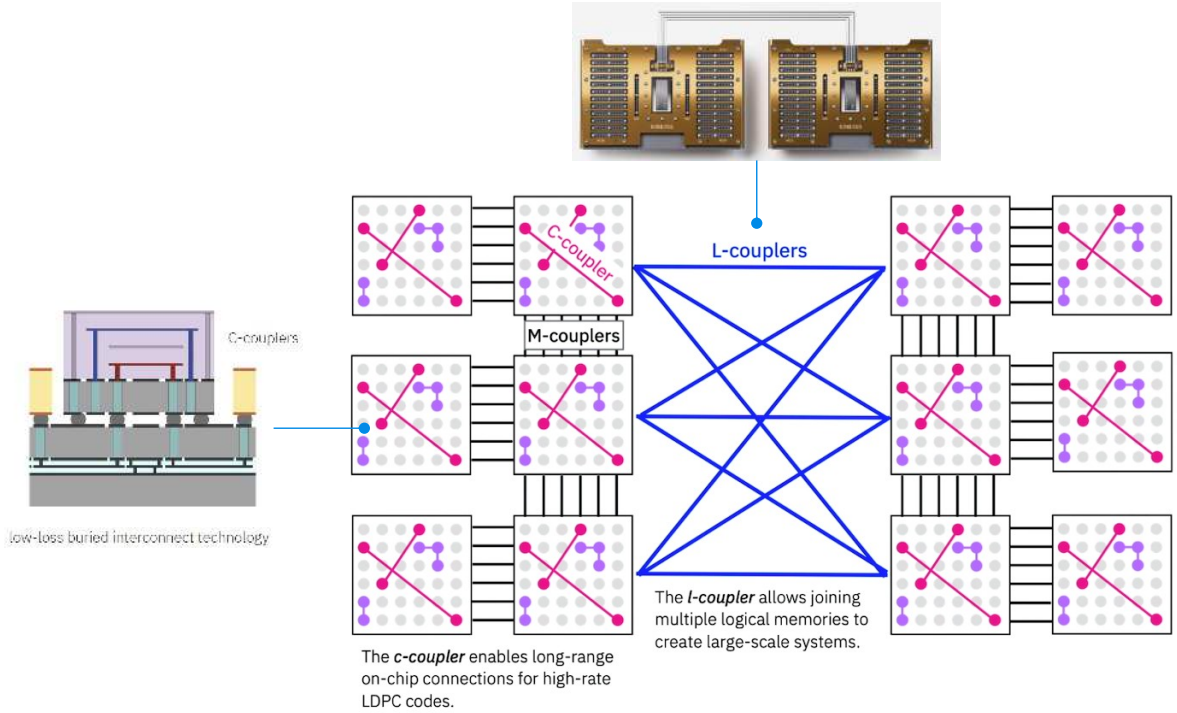

Figure 49: The three types of couplers interconnecting qubit superconducting chips. The C couplers are adding long distance coupling between qubits within the chip. This will create a 1-to-6 connectivity enabling qLDPC error correction codes. Then, the M-coupler connects chips on the same chiplet. At last, the L-couplers connect multiple distant chips with flexible cables. Source: IBM, 2024.

Qubit connectivity. In July 2021, IBM announced a generalization of their hexagon qubits topology. This heavy-hex lattice was the 4th version of IBM Quantum systems qubits topology and has been used upwards of its Falcon processor (27 qubits) until Heron generation chips. It used a hexagonal arrangement with an intermediate qubit on each side of hexagons. The topology was optimized for future implementations of quantum error-correcting codes, using custom hybrid surface and Bacon-Shor subsystem codes [879–881]. The hex lattice reduced the effect of frequency collision between qubits.

However, the heavy-hex layout was discontinued in 2025 with the introduction of the Nighthawk chip in June 2025, which adopts a 1-to-4 connectivity layout like Google Sycamore and Willow (Figure 50 and Figure 51). As a result, due to the increased number of couplers, the number of qubits went down from 156 with Heron r2 and r3 to 120 for Nighthawk. In addition, it will also adopt the 1-to-6 layout to enable qLDPC error correction and the gross code. The first tests with prototype Nighthawk 120 qubits showcase good fidelities for these distant connections (Figure 52 and Figure 53).

3D circuits. IBM started to stack pairs of chips separating qubits from microwave controls, using TSV (through-silicon vias) with their 127 qubit systems in 2021 [883]. This 3D chip layout introduced with Eagle (127 qubits) added multi-level wiring (MLW) on the backside of the interposer. Control and readout signals are routed as strip lines in the MLW and are well isolated from the interposer and qubit metal levels. Connections between the qubits and this MLW are implemented with superconducting TSVs (through-silicon vias). It reduced crosstalk when pairing qubits. They also improved readout multiplexing using 9 lines instead of 5 in Eagle. However, this degrades their CNOT gates fidelity due to collisions between qubit readout frequencies. The connectivity chip had 5 layers in Condor (1,121 qubits) and will have 7 layers in future versions. An additional layer will enable the long-range 1-to-6 connectivity of future chips (Figure 56, Figure 57 and Figure 55).

Qubit control. With microwave-signal multiplexing and intelligent filtering for qubit states readouts, starting with Hummingbird 65 qubits system in 2020. They are also using microwave flexible cables to reduce the space used by microwave cables in cryostats. They are also implementing tunable couplers to control qubits entanglement [884, 885]. With Osprey (433 qubits), wires density improved using 24-lines flexible cables and with control electronics of "generation 3", using custom-made FPGAs.

ibm_phoenix

Programmable qubits	Physical qubits	2Q error (best)	2Q error (layered)	Max circuits per second
120	458	9.55E-4	2.71E-3	109.7 kHz

Status	Region	QPU version	Processor type
Online Maintenance: 10/15	Washington DC (us-east)	1.0.0	Nighthawk r2

Basis gates	Pending jobs	2Q error (median)	Readout error (median)
cz, id, rx, rz, sx, x	0	2.10E-3	7.57E-3

CLOPS	CZ error (median)	SX error (median)	T1 (median)
2.0M	2.096E-3	2.513E-4	168.51 us

T2 (median)	Init error (median)
131.34 us	2.069E-5

Figure 50: Figures of merit of Nighthawk 2 "Phoenix" as of September 2026. Many indicators are provided which also show the variability of qubit performance within the chip, with readout, single qubit gate errors, T_1 and T_2. Source: IBM and [882]. Added in September 2026.

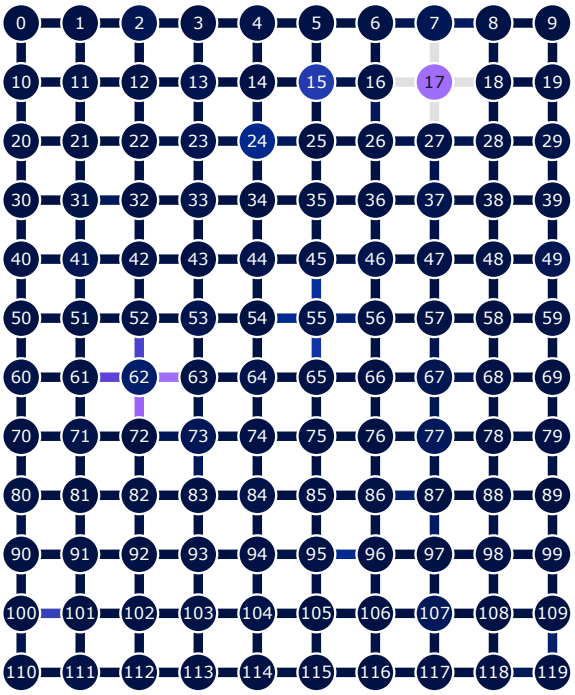

Figure 51: Nighthawk "Berlin" qubit map with its 1-to-4 connectivity. The circle colors represent the readout error rates (light meaning high error, the maximum being 20.4%), and the line representing CZ two-qubit gate errors. The median error is 0.209%, and the maximum 21% (light blue). Source: IBM. Added in 2026.

Scalability also comes from qubits miniaturization coming from various paths like a simplification of the readout electronics replacing the usual circulator with a "microwave-controlled qubit readout multichip module" (QRMCM) [883, 886].

IBM is working on cryo-CMOS control electronics to be deployed in future systems. Cabling optimization is also on the way. The Osprey system was using 24-lines flexible cables with a goal to reach 100 cables. Condor was tested with a similar setup supporting over a thousand qubits, still a record as of mid 2026.

In June 2025, IBM also announced starting partnering with SEEQC for the development of superconducting control electronics, leveraging some funding from DARPA. It doesn't mean IBM is adopting the related SFQ (single flux quantum) technology, but at least considering it.

Figure 55: IBM Loon experimental cryostat in 2026. The grey blox contain the readout circulators and TWPAs while the cylinder contains the superconducting chip. Source: IBM.

Cryogeny. IBM announced in 2020 that it was working on a giant home-made cryostat nicknamed Goldeneye, to host from a thousand to a million physical qubits. The device was 3m high and 2m wide with 1.7 m^3 of experimental volume and 10 internal plates. Its cooling power was 10 mW at 100 mK and 24W at 4K. [40]. It was due for 2023 after some tests were conducted in 2022 at 25 mK. It was to have about 12 pulse tubes and 6 dry dilutions with half of the dilution to be inverted at the bottom. The project was, however, put on hold while

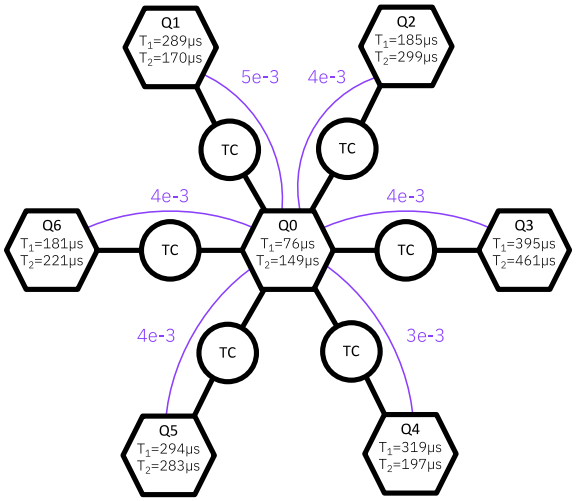

Figure 52: The fidelities of the 1-to-6 qubit connectivity prototyped in 2025. Source: IBM.

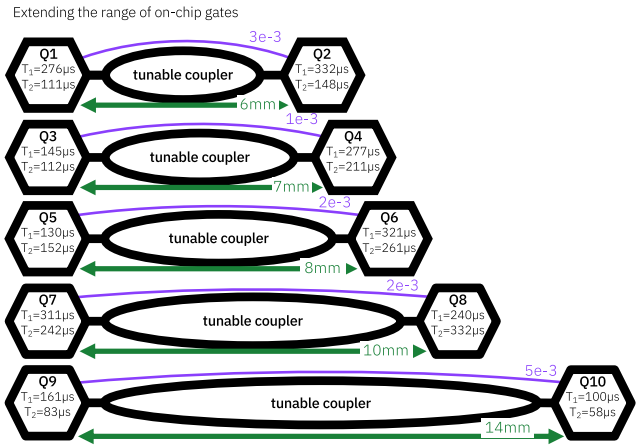

Figure 53: How two-qubit gates are eroding with distance in the 1-to-6 qubit connectivity prototyped in 2025. Source: IBM.

IBM's team was integrating Bluefors KIDE dilution fridges in its System Two. The current plan for Starling and Bluejay large systems is to create a large dilution system looking like series of KIDE. They plan to stage cooling differently to make it more efficient, with some first stage liquid ^{4}He cooling, before the dilutions, and using a modular setup (Figure 58).

Other qubit types. IBM is quietly studying other qubit types. Their Zurich research center is also investigating electron spins and Majorana fermions qubits at a fundamental research level, working on this with ETH Zurich and EPFL. Also, in February 2022, IBM invested $25M in Quantinuum [888]. These signals shouldn't be misinterpreted: IBM is full-steam invested in transmon superconducting qubits. In July 2026, IBM acquired HRL Labs (California) which gives them a more serious plan B option with silicon qubits, as well as an additional expertise in the development and manufacturing of cryo-CMOS control chips.

Serverless. As part of their May 2022 announcements, IBM explained it had adopted a "serverless" architecture, another name for a cloud service driving both classical and quantum computers with a pay-as-you-go pricing [889]. It involves three techniques: circuit knitting that leverages classical resources to cut a quantum circuit into smaller circuits to run on NISQ QPUs and use classical processing. This is interesting but reduces the quantum acceleration generated by the QPUs who will run quantum algorithms of smaller Hilbert space. They then use "quantum embedding" to re-frame a problem and split it between pieces running classically and others quantumly "*for only the classically difficult parts of the problem*". Finally, error mitigation is based on classical post-processing to reduce the impact of some classes of quantum errors.

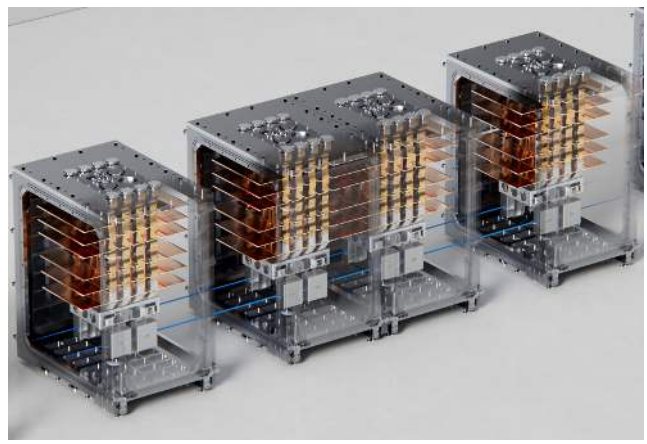

Figure 58: IBM's new modular quantum cryogenic architecture (MoQCA) presented in 2026, which supports connected cryogenic cells, with quantum processors interconnected using flexible-microwave-cable L-couplers. They use square cold plates. The specifications are a vacuum chamber volume of 2.75 m^3, a payload volume of 0.25 m^3 at below 20 mK. It has a cooling capacity of 32 μW at 20 mK, using 30 kW of input power, supporting up to 200 kg of hardware below 20 mK, the total module weighs 3000 kg. The picture lacks the shells around each cryogenic temperature level (50K, 4K, ...). It takes several days to thermalize the whole system. Photo source: IBM.

Metrics and benchmarking. IBM has over time pushed forward several metrics to benchmark its QPUs as their capabilities were expanding.

- **Number of qubits** define the scale of their system. This is a no-brainer, of course. Well, not that much when you consider some vendors who don't even openly communicate on the number of qubits of their QPUs (like OQC when then started).
- **Qubit fidelities** numbers and coherence times (T1/T2) have regularly been published by IBM as

Figure 54: IBM's updated roadmap in June 2025. One specific of this roadmap is that it shows no intermediate FTQC step until the advent of Starling in 2029. All steps before this are marginal improvements of NISQ variants of Nighthawk, which will enable larger NISQ circuits until 2028 with 15K gates, mostly thanks to gate fidelities and QEM improvements. Source: IBM in [7]. June 2025.

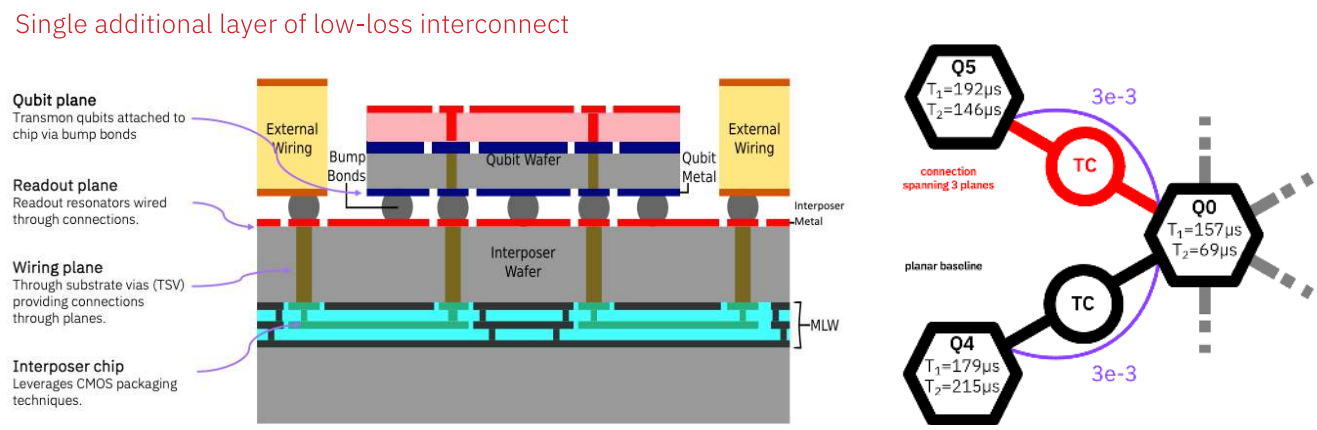

Figure 56: The IBM Loon chip layout will support 6 way connectivity to enable qLDPC correction codes. Source: IBM, July 2025.

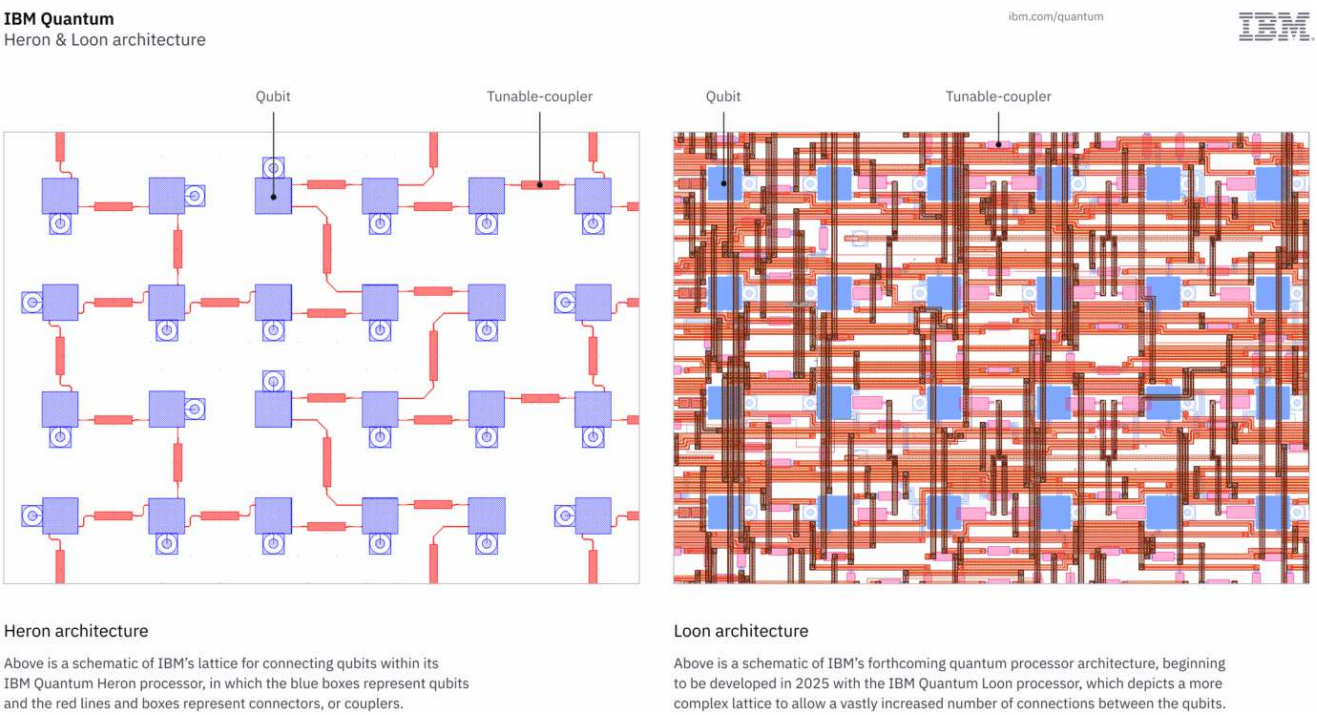

Figure 57: How connectivity evolved between the Heron heavy-hex connectivity and the Loon connectivity. Source: IBM and [887], June 2025.

new QPUs were released on the cloud. IBM communicates openly on its single and two qubit gate fidelities and readout fidelities, with average values and spread.

- **Quantum volume** (QV) was introduced in 2019 to cast their circuit size support in breadth and depth. IBM announced it would double every year. In April 2022, they obtained a record quantum volume of 256, corresponding to successful heavy-output generation on width-8 and depth-8 square model circuits under the QV protocol [890], which increased to 512, or $m = 9$, in May 2022 [891]. Due to limited qubit fidelities, IBMs QPUs quantum volumes have not really made progress since 2022. The metric has not been used for a while by IBM.

- **CLOPS** (circuit layer operations per second) were introduced in November 2021. It defines the speed of their QPUs, also labelled in Hz. It currently sits between 3,800 and 5,000 CLOPS with a record of 15K obtained on a prototype Falcon chip [892, 893]. The discrepancy between this speed and quantum gates durations (between 20 ns and 300 ns) comes from the CLOPS metrics accounting for all the classical preprocessing happening before running your quantum code. The CLOPS definition was updated in November 2023 with the CLOPS_h which accounts for a layer differently: "*rather than a layer representing a set*

of two-qubit gates acting across all random pairs of qubits at once, now a layer only includes the two-qubit gates that can be run in parallel on the system architecture". As of November 2024, IBM's Torino (Eagle r1 133-qubit chip) had a record 200K CLOPS while Fez (Eagle r2 156 qubit chip) reached 28K CLOPS, all thanks to data processing improvements [894].

- **Errors per layered gate** (EPLG) was introduced in 2023. It *encapsulates the entire processor's ability to run circuits while revealing information about individual qubits, gates, and crosstalk. It expands on a well-established way to benchmark quantum computers, called randomized benchmarking*" [895].
- **Number of operations** became a key metric starting in 2024. This is the number of circuit gates that are supported by a QPU. The June 2023 quantum utility experiment was implemented with 2,880 gates and the plan was to exceed 5,000 gates by 2024. It reached 6,000 in 2025. All of this, thanks to quantum error mitigation using a variation of the ZNE (zero-noise extrapolation) technique. IBM plans to reach 15K quantum operations by 2028 with improving both qubit fidelities and QEM techniques and using an improved version of its new Nighthawk 120-qubit chip. Thanks to faster qubit reset, it already improved Nighthawk circuit execution speed in 2026 with its second iteration [882].

Error Mitigation. Before fault tolerant QPUs are developed, IBM is betting on using quantum error mitigation and error suppression techniques [885]. Work is both done in-house and with partners like Q-CTRL, for the implementation of error suppression techniques. Internal research has also been published in 2025 on error detection, that can be useful with both NISQ QEM and FTQC setups [896].

FTQC and error correction. IBM plans to use qLDPC correction codes that will require long range connectivity between the qubits, to be implemented with an additional layer containing microwave couplers on top of the 7-layers connectivity chip used for feeding the qubits with drive microwave.

In August 2023, IBM published an important related preprint paper showing that, under the paper assumed circuit-level noise model and a physical qubit error rate of 0.1% (which remains to be seen at such scales), a 288-physical-qubit bivariate-bicycle block encodes 12 logical memory qubits with a projected logical error rate of 10^{-12}, a lower overhead than a comparable surface-code construction for that target. The comparison depends on the syndrome-round count, the decoder and the logical operation considered, and cannot be reduced to a universal per-logical-qubit ratio [88, 897]. They call this the gross code. The paper initially dealt with memory qubits and sub-Clifford group gate support, but the work was extended to computing qubits and a universal gate set [898]. A single QEC code is not enough to create an FTQC system, particularly for the support of T gates beyond a Clifford group of gates. IBM is exploring the use T gate distillation and lattice surgery with color codes [899, 900].

In June 2025, IBM made several technical announcements detailing how it planned to build FTQC QPUs Figure 59. It is detailed in a long paper for the QEC specialists [901] and in a detailed blog post [7]. They also documented in 2026 how they plan to fight correlated errors [902].

The architecture is based on the following key elements:

- Logical qubits in quantum memory using "bivariate bicycle" qLDPC codes (based on [88]). They correct 12 logical qubits with about 288 physical qubits. These codes are inspired from the work from Pavel Panteleev and Gleb Kalachev in Russia [903–907]. IBM has separately studied the detrimental effect of measurement (or readout) errors during idle times in logical quantum memories [908]. In 2026, IBM proposed to concatenate these codes to support larger quantum circuits with a reduced encoding rate [909]. Magic state distillation will be supported as well [910].
- These memory qubits are created with chips using 1-to-6 connectivity as described in Figure 56. This "Loon architecture" connectivity is split between 4 nearest neighbors and 2 additional distant qubits. This is enough to implement their qLDPC code.
- Their RelayBP error syndrome decoding is described in [393] and [911], BP standing for "belief propagation". Being highly precise and efficient, it will run in with an AMD FPGA, and later on a custom ASIC, and in real-time, as later prototyped in October 2025 [394]. In 2026, they proposed another faster Minimum-Weight Perfect Matching (MWPM) based decoder [912].
- Logical Processing Units (LPUs) handling logical operations and using lattice surgery [913]. They use universal adapters which use bridges to move logical quantum information between LPU and quantum logical memory modules [897, 914]. A process was also proposed to implement transversal Hadamard and CNOT logical gates using code switching [915].
- A separate magic state factory prepares magic states (with the equivalent of a T gate) which are then gate teleported on LPUs using long-range couplers between chips [89]. They are currently studying four different T factories: two using magic state cultivation [916] and two using distillation.
- In 2025, IBM and MIT researchers proposed an extractor system that transforms a standard qLDPC logical memory into an active computational block where all single-block Clifford gates are tracked virtually by the classical compiler. The physical hardware is left to execute complex multi-qubit logical Pauli

measurements which the extractor system physically enables in a single cycle and to process non-Clifford operations via magic states routed from a T-factory through bridge buffers [917].

- Some work is also done to reduce leakage [918].

IBM quantum cloud. IBM's QPUs have been running in the cloud since 2016. These are already used by thousands of researchers, students, startups, and corporations around the world. The IBM Quantum network was launched in 2017. It brings together major Fortune 500 companies, research laboratories and startups interested in developing quantum solutions. This network offered free access to quantum systems with 5 and 7 qubits. Commercial systems had respectively 16, 27, 33, 65, 127 and 433 qubits. At last, a quantum emulator (branded a simulator) supported 32 qubits. It was discontinued in May 2024. In September 2023, free access was expanded to 127-qubit systems, with the retirement of many QPUs using a lower number of qubits. As of August 2024, they had 14 quantum systems online with 127, 133 and 156 qubits. As of August 2025, only six QPUs remained, at least covering the US zone, with only one 127-qubit QPU, and others from the Heron family with 133 and 156 qubits. In 2025, the Quantum Experience cloud was migrated to the IBM Cloud.

In May 2025, IBM introduced its Flex Plan, a pricing scheme for the use of their online QPUs [919]. It starts with a pay-as-you-go plan at $96 per computing minute without a commitment, then the Flex Plan has an upfront fee of $28.8K which is your credit to use 500 minutes at $72 per minute computing time. Then a Premium plan is at $48 per minute and with an upfront fee of $250K for a minimum usage of 5,200 minutes.

Since 2020, IBM proposes a Quantum Credits program to academic researchers, with free access to IBM QPUs. After some evaluation, applicants can use up to 10 hours of compute time. As of mid-2025, the program led to the publication of over 160 peer-reviewed papers [920].

Quantum-Centric Supercomputing (QCSC) is an architecture IBM is promoting to optimize the association of quantum computers and HPCs including GPUs, depending on the workload. It was formalized in 2026 in [921] with covering both NISQ and FTQC scenarios. NISQ scenarios show the need to have a potential close connection between quantum computers and HPCs, like for variational algorithms like SQD. FTQC requires a close connection with the classical computers handling quantum error correction syndrome decoding.

Customer evangelism. IBM has been investing steadily since 2016 to build a worldwide community of developers and users. IBM launched a customer Quantum Computation Center in Poughkeepsie, New York, a quantum center in Montpellier, France, in 2018, and then a partnership in Germany with a Fraunhofer Institute in 2019 plus other quantum centers in Japan, Korea and Canada. Their task is to evangelize developers and researchers to encourage them to develop software on their Qiskit platform and their quantum systems sitting in the cloud.

QPU deployments. Besides the 40+ QPUs IBM has deployed (and retired for most of them) in its own data center, mainly in Poughkeepsie (New York State), IBM has sold and/or deployed QPUs in other locations:

- **USA**, at Cleveland Clinic in Ohio, where IBM announced a partnership of 10 years with Cleveland Clinic in the USA where a 127-qubit System One was installed in 2023 [922], at the Rensselaer Polytechnic Institute in New York [923] and in Chicago where IBM announced in December 2024 the creation of a National Quantum Algorithm Center in Chicago where a System Two Heron QPU will be installed.

- **Germany**. In April 2021, IBM finalized the deployment of a 27-qubit Quantum System in its own site in Ehningen, near Stuttgart, Germany, in relationship with Fraunhofer as an intermediate to reach out the developer community [924]. The access price for the 27-qubit System One was €11,621 and €9,770 per month for the industry and for R&D [925]. This "quantum data center" was inaugurated in October 2024, for running hybrid classical and quantum software under the umbrella of the GDPR privacy regulations [926]. It was to also host an Eagle 127-qubit system, and later on, an Heron 133 qubit QPU.

- **Japan** with multiple IBM QPUs installed at the University of Tokyo, the first one being a 27-qubit Falcon in 2021 which was updated to a 127-qubit Eagle in 2023. In May 2025, the University and IBM announced the upcoming installation of a 156-qubit Heron QPU. In June 2025, the first IBM System Two deployed outside the USA was installed at RIKEN in Japan with a Heron 156-qubit chip, being co-located with the Fujitsu Fugaku supercomputer.

- **South Korea** with an Eagle system installed at Yonsei University in 2024, to be replaced by a Nighthawk in November 2026.

- **Canada** with a QPU installed in Bromont, near Sherbrooke [927].

- **Spain** where a QPU was deployed in San Sebastian [928].

- **Switzerland** where a Nighthawk System Two deployment was planned to be deployed in 2026 at the Swiss National Supercomputing Center, in partnership with Lockheed Martin, armasuisse, Switzerland's Federal Office for Defence Procurement, and ETH Zurich. It seems related to Lockheed Martin's sale of F35 to the Swiss army.

- **India**. In May 2025, IBM and Tata Consultancy Services announced the upcoming installation of a Heron 156-qubit QPU at the Quantum Valley Tech Park in Amaravati.

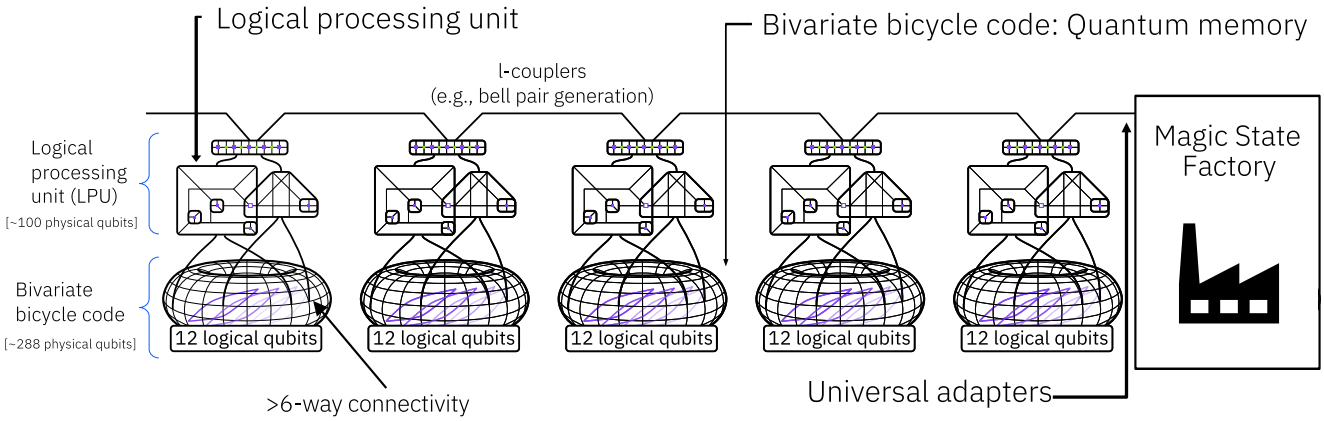

Figure 59: IBM FTQC architecture announced in 2025. It consists of several units of 12 logical qubits, each containing Logical Processing Units (LPU) and Quantum Memories implementing the bivariate bicycle code. The units are interconnected with L-couplers, made with flexible microwave cables. A separate magic state factory creates magic states (with the equivalent of T gates) which are then gate teleported on the LPUs. Source: assembled from multiple slides from IBM, July 2025.

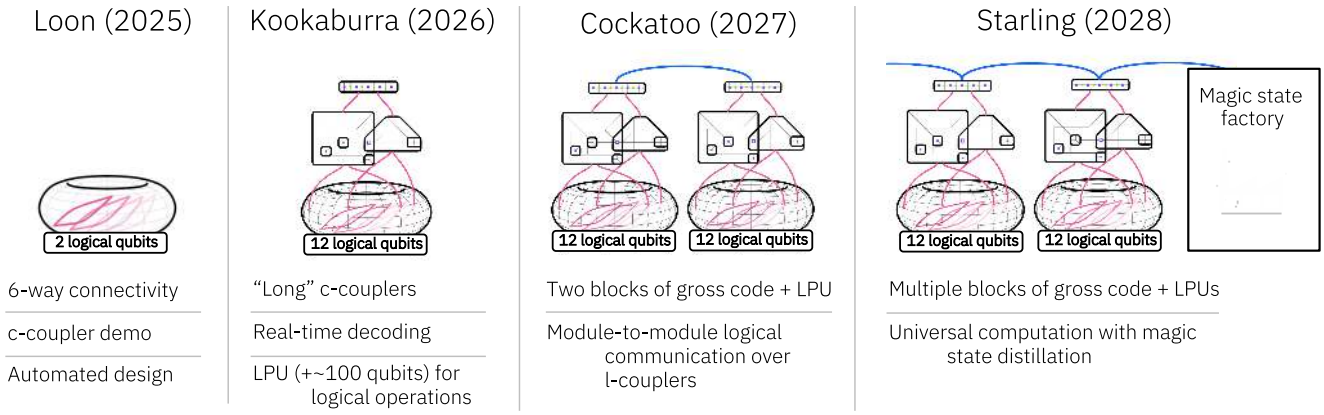

Figure 60: IBM FTQC roadmap announced in 2025 which will progressively build the architecture presented in Figure 59. Source: IBM, July 2025.

QPU name	Region	Qubits	2Q error (best)	2Q error (layered)	CLOPS	Status	Total pending jobs	Processor type
ibm_kingston	us-east	156	1.05E-3	3.62E-3	250K	Online	11	Heron r2
ibm_pittsburgh	us-east	156	8.42E-4	2.73E-3	250K	Online	12	Heron r3
ibm_fez	us-east	156	1.45E-3	5.43E-3	195K	Online	34	Heron r2
ibm_marrakesh	us-east	156	1.02E-3	3.85E-3	195K	Online	632	Heron r2
ibm_torino	us-east	133	1.26E-3	9.23E-3	210K	Online	5,301	Heron r1
ibm_brisbane	us-east	127	2.92E-3	1.79E-2	180K	Online	2,072	Eagle r3

Figure 61: IBM QPUs online as of late August 2025 and their related fidelities. Source: IBM.

In May 2025, IBM announced that it had generated $1B of revenue with its quantum computing business since it started around 2016. It probably comprises a significant share of hardware sales, complemented by cloud QPU access time and some consulting and training services.

Software. IBM's software platform is built around Qiskit and its many components. We describe it in detail in the quantum software tools section. Qiskit is currently the dominant development software platform according to a Unitary Fund/Foundation survey done in 2024 (Figure 62).

IBM research teams are also finding many ways, more or less efficient, to optimize algorithms run-time. For example, they are allowing more computations with the Bernstein-Vazirani algorithm run on 12 qubits, where

SWAP gates are replaced with resets, improving fidelity from 0.0007 to 0.80.

They also propose to use "circuit knitting" (already mentioned), i.e., combining smaller circuits to simulate larger problems using entanglement forging [929–933]. However, this technique has a strong tendency to strongly attenuate algorithm quantum advantage and parallelism.

IBM scientists introduced in February 2025 a framework to reduce quantum circuits depth using classical simulation algorithms based on Clifford perturbation theory (CPT), and reducing the error mitigation workload [934].

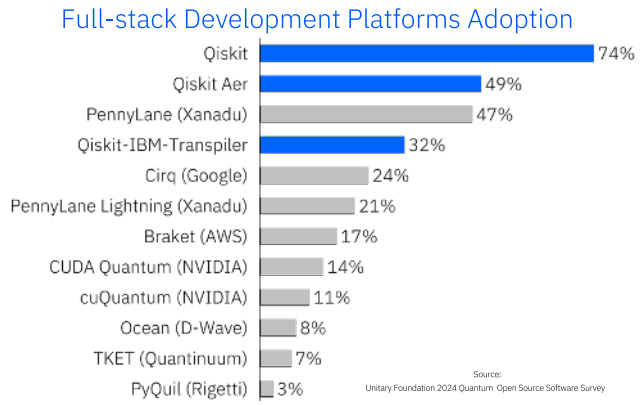

Figure 62: IBM leads the quantum software development ecosystem with its Qiskit adoption. Source: Unitary Fund survey mentioned in [935].

Case studies. In June 2023, IBM announced having reached some quantum utility with a 100 breadth × 60 depth circuit running on a Kyiv 127 qubit QPU implementing a kicked Ising model problem solving algorithm, thanks to using quantum error mitigation (ZNE). The performance was documented in a Nature paper [383] and with additional information found in Forbes [936]. The authors stated that they "*fully expect that the classical computing community will develop methods that verify the results we presented*". Back then, they didn't provide many insights on the types of problems that could be solved with some encoding into an Ising model.

It did not take long before efficient tensor based classical simulations of the Ising model were developed. A couple weeks later, Miles Stoudenmire et al. from the Flatiron Institute did publish a preprint showing a classical solution yielding an accuracy of $\sim 10^{-14}$ running faster than IBM's QPU, in less than 2 minutes. It could even run it with a better accuracy in less than 7 minutes to run on a single Intel Skylake CPU using 0.3 GB of memory [937]. A couple days later, a Caltech team did a similar experiment and could implement in emulation mode IBM's experiment on a simple laptop [938, 939] and a team from Google did the same in one second using a single GPU [940]. A research team in China arrived at a similar conclusion in August 2023 [941]. Then, an IBM team benchmarked these various classical solutions and found discrepancies in their results, of about 20% [942]. A team from Bar-Ilan University in Israel explained why IBM's performance could be achieved with such a noisy QPU [943], another international team created yet another efficient classical simulation of the IBM kicked Ising model [944] and a team led by Multiverse extended this to 433 and 1,121 qubits using another tensor networks variation [945]. This quantum/classical computing battle has not ended yet!

Afterwards, several other quantum utility case studies were published by IBM and academics. Academic case studies mostly relate to low-level physics simulations far from regular business needs, like Schwinger model vacuum simulation [946–948], Nishimori transition [949], scattering in quantum field theories [950], problems in Conformal Field Theories (CFTs), which is part of quantum field theories (QFTs) [951], proton transfer reaction simulation [952], simulating cosmological particle creation [953], simulating large spin chains [954, 955], spin lattices [956], simulating spin Heisenberg models [957], non-equilibrium thermodynamics [958], spin chain ground-state energy estimations via sampling from Krylov states [959] (Figure 63), higher-order topological lattices in condensed matter physics [960], a Fermi-Hubbard model [961], various small scale machine learning cases [962], and efficient calculation of Green's functions which are used to solve differential equations describing physical systems (scattering, energy levels, and many-body interactions) [963].

Publicized cases closer to industry needs are usually older and tested with only a few qubits like with AMGEN [964] or with raw resource estimates like with Woodside Energy [965]. Review papers in the fields of healthcare and life sciences, materials science [966], high energy physics, and optimization were also published although covering practically various breeds of QPUs (early stage, utility stage and FTQC) [967]. In quantum chemistry, Sample-Based Quantum Diagonalization (SQD), an alternative to VQE, was used in 2025 by Lockheed Martin who modeled the electronic structure of open-shell molecules that have unpaired electrons, which is useful for transition metal complexes and intermediate states in chemical reactions, starting with methylene (CH2) and using 52 qubits [968]. It was also used by IBM researchers to simulate the reaction between lithium and oxygen in Li-metal anode batteries with up to 76 qubits [969] and with Moderna for simulating photoreactive precursors using 64 qubits [970].

In July 2025, the discourse moved to the notion of quantum advantage, with IBM expected to be demonstrated by 2026 [971, 972]. Their definition is "*the ability to execute a task on a quantum computer with a correctness of the quantum computer's output that can be rigorously validated. And it is performed with some demonstrated superior efficiency, cost-effectiveness, or accuracy over what is attainable with classical computation alone*". They even launched a Quantum Advantage Tracker on GitHub [973, 974]. It is not easy to use for a business end-user.

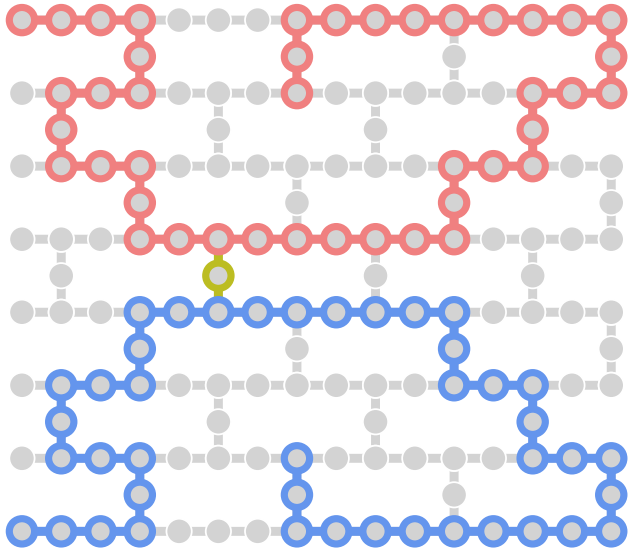

Figure 63: Mapping of a spin chain model on an IBM chip using 85 qubits out of 156, as implemented in 2025. The results were inline with classical DMRG tensor-network based methods, but seemingly not in a quantum advantage regime. Source: [959].

Since late 2025, IBM and their partners released several papers on quantum simulations running on their NISQ systems and the quantum advantage was not really there yet:

- IBM and RIKEN computed an approximate electronic structure of the [2Fe–2S] and [4Fe–4S] clusters beyond the reach of exact diagonalization with 77 qubits of the Kobe Heron processor coupled to the RIKEN Fugaku in a closed variational loop. The resulting accuracy is comparable to classical approximation methods, but with the classical share of computing being enormous [975].
- IBM and Cleveland Clinic created a fragment-based workflow to predict the relative energies of two conformers of the 300-atom miniprotein, using a by divide-and-conquer method with hard fragments solved by an SQD quantum algorithm and trivial ones by a classical FCI. SQD fragment results are benchmarked against classical methods. There is no quantum advantage [976].
- IBM and RIKEN improved accuracy over classical sparse ground-state solvers using a quantum computer with a potential quantum advantage on accuracy and no speedup [977].
- IBM and STFC (UK) implemented a tensor-network approximate quantum compiling protocol to build shallow circuits of 18 to 39 CNOT depth that prepare 100-site ground states of some Heisenberg chain in a regime that is still classically tractable [978].
- IBM, EPFL et al. used SqDRIFT, a randomized sample-based Krylov diagonalization algorithm to run a quantum simulation of a half-Möbius molecule C Cl at active spaces of up to 50 orbitals and 100 qubits, with no demonstrated quantum advantage [979].
- Q-CTRL implemented in 2026 a 1D Fermi-Hubbard dynamics with up to 120 qubits and as many as 90 Trotter steps, observing spin-charge separation from a vacancy defect. Computing time is up to 3000× faster than an optimized TDVP simulation, however, the comparison was made against a solver running on a single 32-vCPU, 64 GB AWS instance. This was not really fair [980]. The computing time gain was then reduced to 500×, 36× [981] in June 2026 then and <1 in August 2026 by Garnet Chan et al. using a classical MPO-based tensor network simulation and 160 GPUs with cost <$8M (less than an IBM QPU) and power of about 250 kW (higher than a single quantum processor IBM system), and potential scaling to a larger problem [982].
- IBM, RIKEN and Cleveland Clinic claimed in May 2026 to have simulated 12,000 atoms [983]. The problem is that the quantum part, Sample-Based Quantum Diagonalization (SQD), named TrimSQD, is simulable classically [984–986]. It splits the problem into small chunks of 30 to 45 orbitals. In the experiment, the QPU plays a very minor role with sampling some electronic configurations leading to some classical Hamiltonian diagonalization. The accuracy improvement vs state of the art methods come from the classical improvements running on GPUs.

In July 2026, like a Swiss clock, IBM announced having reached the promised quantum advantage, leveraging three key papers [987–989].

The first paper from IBM and the University of Chicago used some Doped Clifford Sampling (DCS) on an Heron R3 chip. They created a 70-qubit, depth-70 Clifford circuit using 468 T gates and 2,869 CZ gates, and 97 physical qubits to implement distance-2 error-detection codes based on post-selection (not QEC). They determined that the circuit is intractable for current tensor-network based classical comparables. The paper didn't demonstrate an application quantum advantage. However, it could help in generating magic states in the future.

The second paper from Qedma, RIKEN and BlueQubit, used Qedma's QESEM error mitigation software on a Heron R3 processor, for tracking how magnetization oscillates in a Floquet Ising model with up to 74 qubits. They reached the limits of exact statevector simulations starting at 35 qubits on the Fugaku HPC. They also tested the same thing on a Quantinuum H2 and Helios system.

The third paper from Algorithmiq and multiple academic partners used 56 qubits on a Heron chip to estimate an operator Loschmidt echo, which evaluates how information propagates in a disordered system. They used a Clifford circuit on a 1D chain of data qubits, encoding it with a distance-2 spacetime error-detection

code via adjacent ancilla qubits. These circuits couldn't be simulated classically.

All this reaches the limits of what can be done on NISQ systems before FTQC comes in. Error mitigation and detection has an exponential cost with the circuit size. It's a bit of a swan song.

Partnerships. IBM has many other technological ad-hoc partnerships in place. Let's mention a couple ones: with the University of Tokyo, AIST (Japan), with Fermilab's SQMS Center, with Algorithmiq (on NISQ chemical simulations), with Bloq Quantum in India (in finance, automotive, healthcare and logistics), ColibriTD (France, for solving partial differential equations), and with Q-CTRL and University of Sydney (on error mitigation and correction). In June 2021, IBM announced a five year $300M artificial intelligence and quantum computing research partnership with the UK. They plan to hire 60 scientists as part of the new Hartree National Centre for Digital Innovation (HNCDI) [990].

Google

USA, 1998

Google is clearly in "research mode" with quantum computing. It started to invest in quantum computing with testing some algorithms on a D-Wave quantum annealer installed in the joint QUAIL laboratory established with NASA at the Ames Research Center in Mountain View. Google's quantum team contains about 400 people.

Company. Google initially wanted to develop its own quantum annealer but then switched gears towards gate-based superconducting qubits quantum computing. In 2026, though, it also decided to explore the path of cold atom computing with the hire of Adam Kaufman's team in Colorado. We describe this in the cold atoms vendor part of this book.

Hartmut Neven has been managing the related quantum hardware and software effort since 2006. In 2019, he put forward an empirical law called Dowling-Neven according to which the power of computers doubles exponentially. This was exaggerated when you look at their evaluation method [991]! The number of qubits would increase exponentially, and the computing power would also double with each addition of a single qubit. All this, every six months. Unfortunately, it's not working like this. First, there is no doubling of the number of operational qubits every six months! Google announced 72 qubits in March 2018 and then 53 qubits in October 2019. It delivered 72 qubits only in 2022. In 2024, Google Willow reached 105 qubits. So be it for the Dowling-Neven law! Second, due to overhead of noise (in NISQ) and quantum error correction (in FTQC), the addition of one physical qubit doesn't double the system power.

Superconducting qubits hardware was developed by John Martinis et al. between 2014 and 2020. John Martinis resigned from Google in April 2020 after being demoted to a scientific advisory role mid-2019. He explained this in an exit interview for Forbes [996]. All this was done in connection with the University of Santa Barbara in California (UCSB), where he came from with part of his team.

In 2017, Google stated its ambition to obtain some quantum supremacy as defined by John Preskill in 2011 [997–1001]. In April 2017 came a 9 qubits chip followed in 2018 by their Foxtail 22 qubits chip. In March 2018, Google announced a 72 qubits chip named Bristlecone, promising a two-qubits gates fidelity of 99.56%. It seemed, however, to be a technological dead end and was abandoned. Then came the famous October 2019 so-called quantum supremacy with their Sycamore processor using 53 qubits interconnected with couplers. It used a random algorithm akin to the boson sampling algorithm imagined by Scott Aaronson in 2012 [1002–1006].

Sycamore engineering. Let's first have a look at Sycamore's engineering, at well as at its related supremacy benchmark and its updates over time leading to Willow in 2024:

- **Qubits couplers**. Sycamore used controllable qubit couplers, a technique pioneered by William D. Oliver's research team at the MIT Lincoln Labs [1007]. There are 86 of them, connecting the chip 53 qubits. These couplers are qubits whose frequency is controlled by a direct current line (DC). It allows the implementation of fast two qubits quantum gates, acting in an average 12 ns. This technique was later adopted by IBM in its Heron processor launched in 2023.

- **Qubits gates and fidelities**. Sycamore implemented CZ and CPHASE two-qubit gates. and two-qubit gates have an error rate ranging from 0.5% to 1.5% while single-qubit gates error rates fare between 0.05% and 0.5%. DC flux lines are used to create Z gates, or phase gates, which reduces the phase error usually observed with these gates. It 72-qubit Sycamore chip had 99.4% two-qubit fidelity. Qubit readout uses only a few microwave photons sent to the qubits. The result is amplified by 100 dB in several steps, one at the 15 mK processor stage and another at the 3K stage. The amplified microwaves are converted digitally by an ADC (analog-to-digital converter) and analyzed by a FPGA to detect their phase. Readout microwaves are multiplexed in the frequency domain with 6 qubits groups conveyed by a single cable, between 5 and 7 GHz. Sycamore implemented high fidelity qubits reset, allowing a reuse of qubits in quantum computations. Google is working on a model-based technique to reduce these readout errors [716]. In the 6-years since Sycamore's inception, Google improved its qubit fidelities to 99.67% (CZ) and 99.86% (iSWAP), depending on the chip variant used [122]. Google is currently partnering with researchers in Slovenia to work on the science

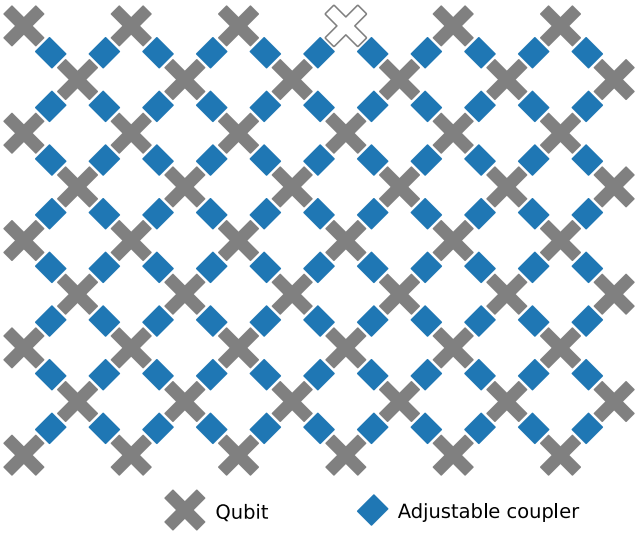

Figure 64: Google's 2019 Sycamore 53-qubit chip layout, with data qubits (in grey) and coupler qubits (in blue). It led to the first quantum supremacy experiment. Source: [992].

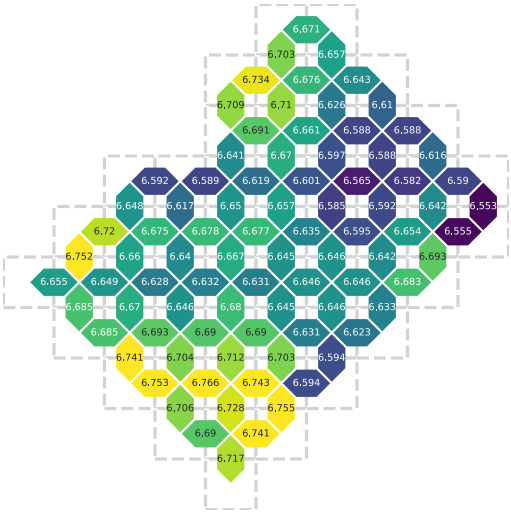

Figure 65: The interaction frequencies between each qubit pairs were calibrated and optimized using a machine learning solution. Source: [993]. The frequency allocation technique was later optimized to accommodate the creation of logical qubits, with the SNAKE optimizer [994]. Researchers in China published a paper on neural network based frequency tuning in 2025 [995].

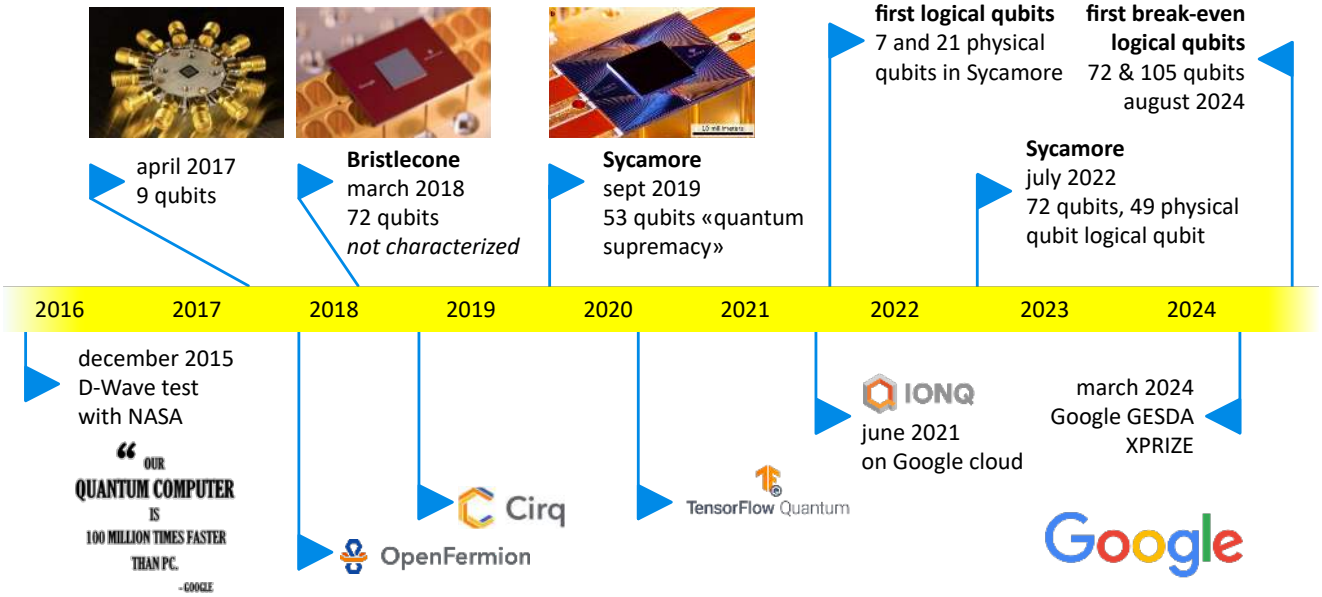

Figure 66: Google's quantum computing timeline. © Olivier Ezratty, 2022-2024.

of materials that is of paramount importance to improve qubit fidelities and on algorithms development [1008]. They are creating a research lab there to host local and Russian researchers.

- **Microwave generation**. Figure 67 shows the control electronics inside and outside the cryostat. Sycamore used 54 external microwave signal generators for the single-qubit gates (X and Y), 54 for qubit frequency control and 86 for qubit control (lest one since the first version of Sycamore had one dysfunctional qubit). This was completed by 9 readout microwave control signals, using frequency domain multiplexing readout by chunks of 6 qubits based on wideband parametric amplifiers operating at the 15 mK stage (an IMPA). The control electronics package includes 277 digital-to-analog converters occupied 14 6U rack-mount cases. There was a similar number of coaxial cables ending in the cryostat. Those numbers are of course larger for Willow and its 105 qubits.

- **Machine Learning based calibration**. Qubits and couplers are controlled with microwaves carried by coaxial cables, at frequencies ranging between 5

and 7 GHz, adjusted by a DC flux line. Google developed a deep learning-based qubit calibration code, which refines qubit microwaves activation frequencies to avoid crosstalk between neighboring qubits Figure 65). Scaling this calibration is a challenge for larger QPUs [994] since it needs several hours per day of calibration which is problematic when running long FTQC circuits. In November 2025, Google proposed a calibration technique using reinforcement learning that is handled during computing and error correction. Its scalability was simulated with up to a distance 15 surface code [656].

- **Isolation**. Qubit chips are protected by some Mu-metal shielding, another one in aluminum and a black coating to absorb infrared photons. The processor is made of aluminum and indium on silicon and includes two dies stacked on top of each other or next to the other (Figure 67).

- **Correlated noise**. Google also works on addressing cosmic radiation originated noise in circuits, lastly with some collaboration with Michel Devoret who joined Google as a scientific advisor in 2023 [637, 1009]. It paid off in the Willow chips presented in their logical qubit papers from August 2024 (arXiv) and December 2024 (Nature). In a similar line, Google and Devoret are working on understanding unwanted long-range qubit coupling effects [1010].

- **Supremacy experiment**. Google's supremacy experiment was officially detailed in Nature in October 2019 [1011], filing 70 pages when including the supplemental materials [993, 1012, 1013]. Google compared their qubits with the most powerful supercomputer of the time, the IBM Summit installed at the Department of Energy's Oak Ridge National Laboratory in Tennessee [1014]. Computing for 200 seconds on Sycamore would take 10,000 years once emulated on the IBM Summit. This comparison didn't make much sense as we discuss quantum supremacy and advantages in another part of this book. Sycamore showcased some energy consumption advantage, with a ratio of about one to a million. Its power consumption was about 25 kW as the ORNL IBM Summit was at 12 MW at peak charge, and the computing time ratio was 2.5 minutes vs. 2.5 days (1/1440) in the most favorable IBM Summit case. But this was about comparing apples and oranges given the supremacy doesn't relate to solving useful problems with input data and parameters.

- **Cross-Entropy Benchmarking (XEB)**. The benchmark algorithm combined a set of random quantum gates with a homogeneous distribution. This last part scans all the possible values (2^{53}) of qubits superpositions [1015]. In the supremacy regime, the estimated linear XEB fidelity was about 0.14%. Millions of samples were collected to estimate the output distribution and its correlation with the ideal probabilities, rather than to average away a wrong answer [993, 1016]. The XEB benchmark had a 20 quantum gates cycles. Randomized benchmarking used in Google's experiment is just some physical experiment that is hard to simulate classically, but is not doing computing per se, given it is not fed by some problem data nor outputting any useful data. This does not clearly establish some quantum computing superiority over classical computing [1017, 1018].

On October 21, 2019, IBM researchers published a paper in which they questioned Google's performance, stating that they could run their algorithm in 2.5 days instead of 10,000 years on the IBM Summit supercomputer [1019–1021]. This would require adding 64 PB of SSD to the supercomputer, which they had not actually tested. That's about 7 racks full of SSDs at 2019 capacity. IBM wanted to contradict Google's claim of quantum supremacy, which they turned into some sort of quantum advantage [1022, 1023]. Then, several tensor networks based emulations of Google's noisy qubits could replicate their 2019 supremacy experiment from 2020 to 2022. In 2022, Google upgraded its experiment using 70 of their latest Sycamore 72-qubit processor [1024]. The related paper did show that their 2019 supremacy was short-lived. It is now possible to emulate it classically in just 6.18 seconds, instead of the 2.5 minutes of the quantum experiment (Figure 68).

Exp.	**1 amp.**	**1 million noisy samples**		
	FLOPs	FLOPs	XEB fid.	Time
SYC-53 [9]	$6.44 \cdot 10^{17}$	$2.60 \cdot 10^{17}$	$2.24 \cdot 10^{-3}$	6.18 s
ZCZ-56 [10]	$6.24 \cdot 10^{19}$	$6.40 \cdot 10^{19}$	$6.62 \cdot 10^{-4}$	25.3 min
ZCZ-60 [11]	$1.32 \cdot 10^{21}$	$1.41 \cdot 10^{23}$	$3.66 \cdot 10^{-4}$	38.7 days
This work	$4.74 \cdot 10^{23}$	$6.27 \cdot 10^{25}$	$1.68 \cdot 10^{-3}$	47.2 yr

Figure 68: Google's 2019 supremacy experiment can now be classically simulated in 6.18 s on the DoE Frontier supercomputer instead of the initial estimation of 10,000 years on the IBM Summit supercomputer. With 70 qubits, the classical timescale reaches 47 years. Source: [1024].

Logical qubits. Google's quantum error correction plan is to use surface codes. Their mid-term goal was to create a "logical qubit" prototype with 105 physical qubits (done in 2024 with Willow), and then to extend it to 1,000 physical qubits [1025]. The end goal is to build logical qubits with error rates around 10^{-12}, a level that is required to execute many useful gate-based algorithms (Figure 69, Figure 70).

With surface codes, logical qubits are organized in squared arrays of about d^2 physical qubits (in blue, green ones are the qubit couplers) where d is the so-called code distance (5 in the example below). How did Google come out with the 1,000 physical qubit per logical qubit number? It comes from the empirically fitted error-suppression factor Λ, the ratio by which the logical error per cycle drops each time the code distance is increased by two, under a given circuit and noise

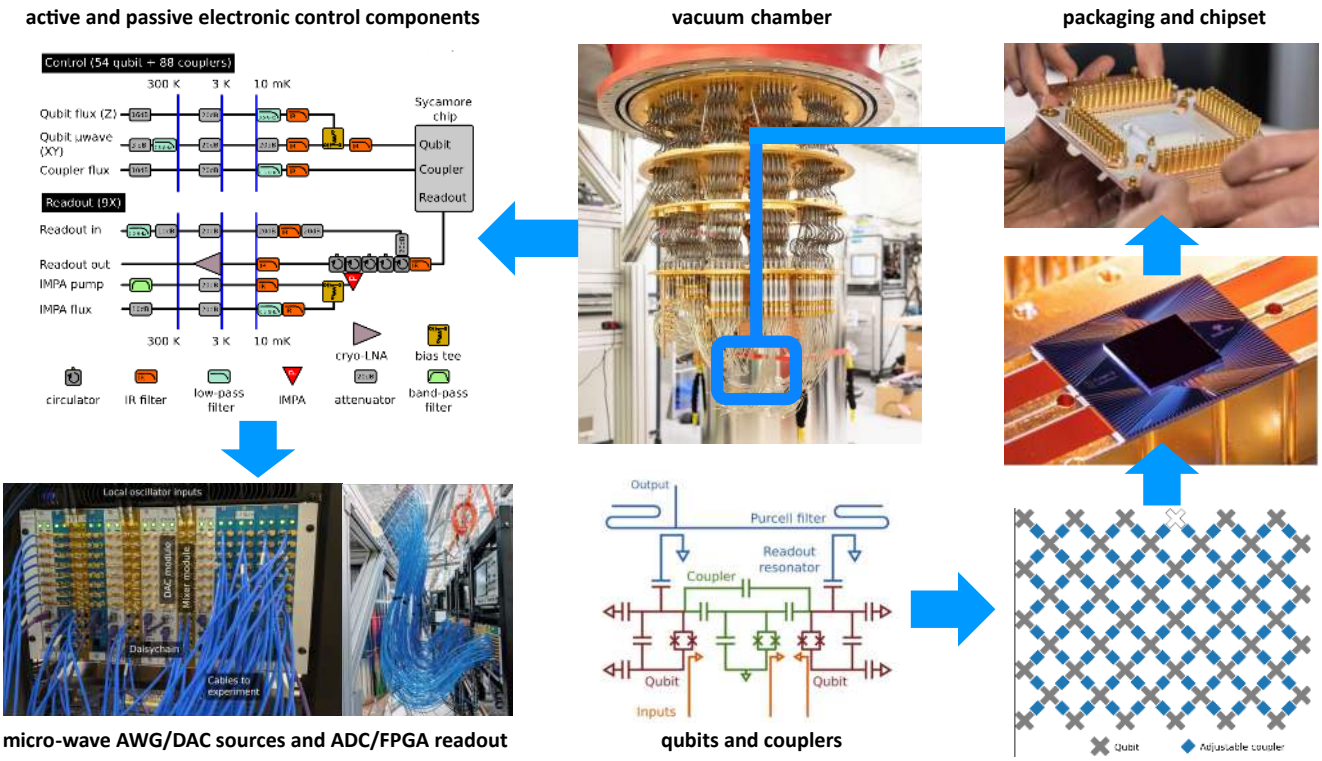

Figure 67: Russian doll description of Sycamore starting with the qubits and coupler, then with the chip layout, its size, its packaging and connectors, where it is placed in the cryostat and the surrounding control electronics. Source: Google. Compilation ⓒ Olivier Ezratty, 2020-2022 with sources from Google.

model [43]. It is not a threshold-to-physical-error ratio, and the logical error is not simply $1/\Lambda$. Reaching a 10^{-12} logical error rate with about 1,000 physical qubits per logical qubit requires $\Lambda \approx 10$ (above, right). They implemented their first surface codes with d=3 and d=5 [1026]. A surface code size depends on the target logical qubit gates fidelity.

In 2021, Google tested repetition code layouts on a 53-qubit Sycamore chip with 21 qubits in a 1D chain correcting flip or phase errors and a distance-2 surface code of 7 qubits correcting both flip and phase errors. It did show that flip and phase errors could be exponentially suppressed by adding more physical qubits [678, 1027, 1028]. They could assess the impact of a good Λ value. They also propose to use "pulse sequences" to correct unwanted crosstalk and dephasing that are disturbing surface codes [1029].

In March 2023, their July 2022 preprint published in Nature used a 72-qubit Sycamore version implementing a distance-5 surface code for a single logical qubit of 49 physical qubits. It was still insufficient to create a logical qubit with a better fidelity than the underlying physical qubits [1030]. The next step is a 105 qubits QPU to implement a distance-7 surface code logical qubit that will be the first to improve fidelities compared to its physical qubits. It was operational in 2024.

In September 2023, Google AI published a paper proposing some new optimizations in surface code implementation by replacing CNOT gates by iSWAP gates [1031].

Other QEC work cover color codes to correct transversal single-qubit logical Clifford gates in December 2024 [1032] and dynamic surface codes in June 2025 which can be implemented with iSWAP gates that are supported in one version of Willow which enables better detection of leakage errors [1033]. That paper did show that Google was considering an hexagonal qubit layout similar to the heavy-hex layout that IBM abandoned in 2025. It was confirmed in another preprint from August 2025 showing how to go around broken qubits and couplers in such circuits [1034].

Willow. In August 2024, Google created a logical qubit memory with better logical fidelities than the underlying physical qubits [43]. They did that with a distance-5 surface code on 72 qubits, integrated with a real-time decoder, and a distance-7 surface code with 101 qubits from a new 105-qubit chip, later named Willow (in December 2024), doubling fidelity vs the distance-5 chip, and obtaining a T_1 of 291±6 μs while the best physical qubit T_1 is 65 μs. They obtained a logical error rate of 0.143%.

They implemented this in a logical quantum memory, not for quantum computing, and with no logical gate at all. They used an XZZX surface code that was created by Pablo Bonilla Ataides back in 2020 [1038]. Their surface code has 4 leakage removal qubits (Figure 70). They call this data qubit leakage removal (DQLR). They don't indicate how this resource scales with the size of the surface code.

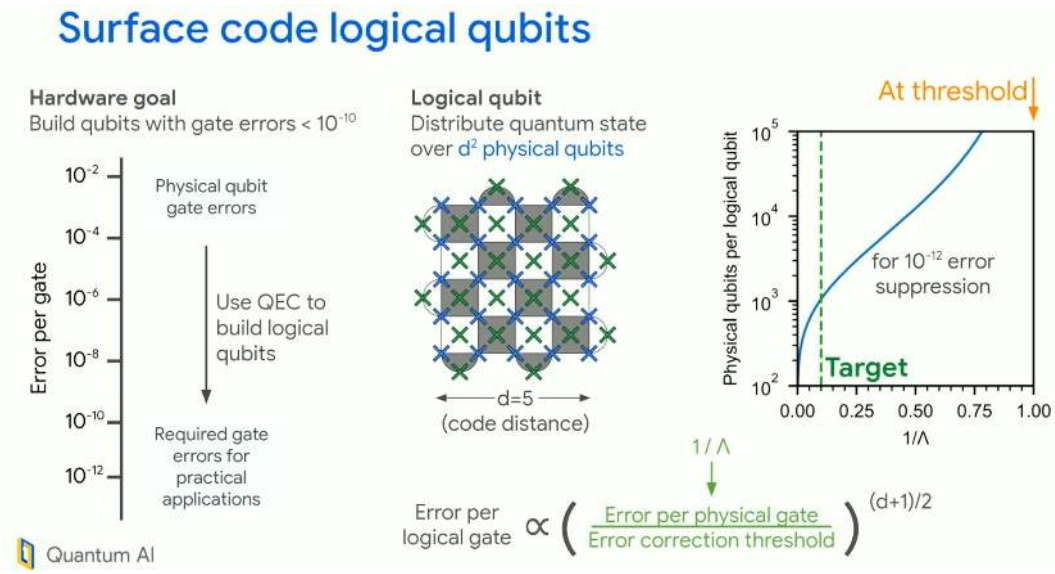

Figure 69: How Google planned in 2022 to reach an error rate of 10^{-12} with its logical qubits. Source: [1025].

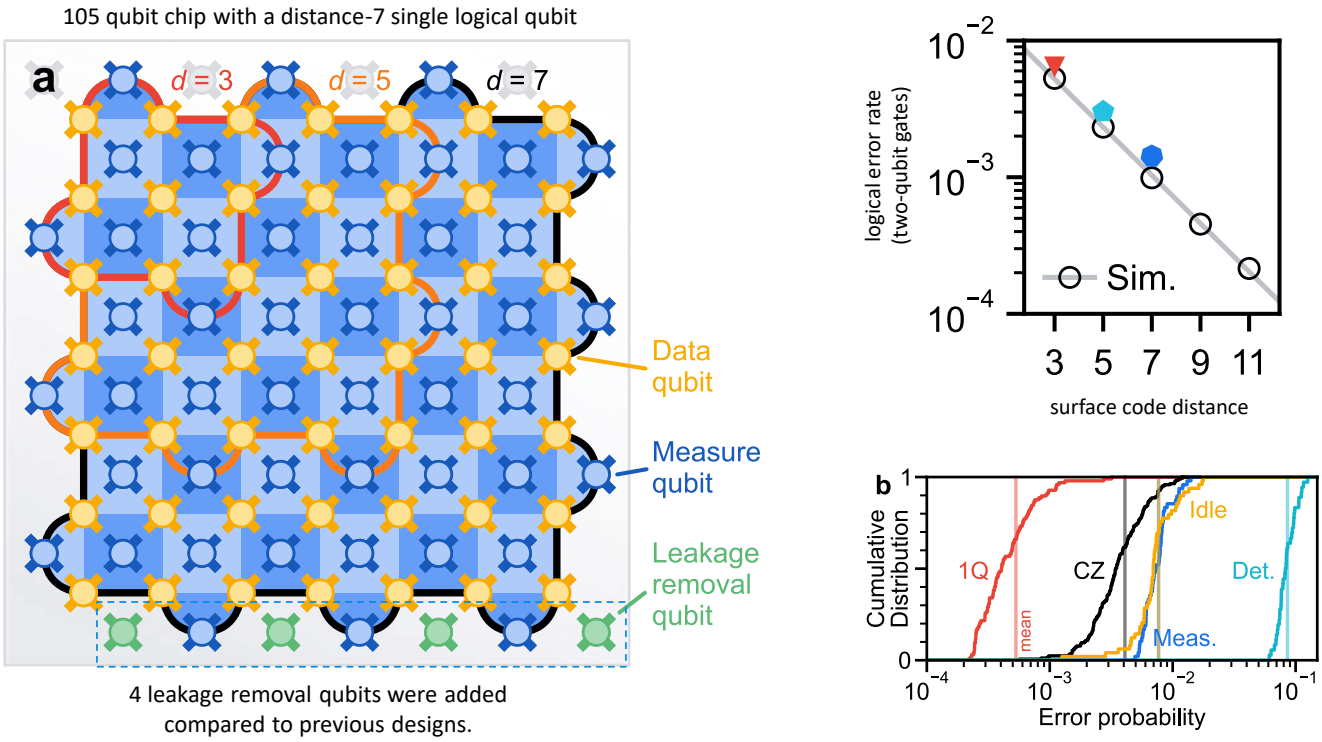

Figure 70: The distance-7 surface code logical qubit layout in Willow's 105-qubit Google chip presented in 2024, showing their 4 dedicated leakage qubits. Their logical memory exhibited fidelity improvements as the surface code distance grew from 3, 5 to 7. The chart at the bottom right exhibit the physical error rates distribution for a single-qubit gate, two-qubit CZ gate, then measurement and idle qubit. It shows that it is easier to obtain good fidelities for single qubit gates than two qubit gates. Measurement and idle qubit errors are worse. This relates to the physical qubits on the 72 qubits chip. 10^{-10} quantum memory error rates would require over 4,000 physical qubits per logical qubit. Source: [43].

They used machine learning and reinforcement learning for syndrome decoding, combining five different decoders including one using the matching synthesis technique and the Libra decoder [1039], from Google, but with a less efficient correction yielding 0.171% errors. Real-time decoding of the syndrome measurements per cycle increases quadratically with code distance. They could not implement a real-time decoder with a distance-7 surface code as a result.

Their error reduction was matching theory with a factor $\Lambda = 2.14$, which is the error reduction ratio when the code distance d increases by 2, from 5 to 7, and then, doubling the number of physical qubits, from 49 to 97, according to $(2d^2 - 1)$ and with $\Lambda = \varepsilon_d/\varepsilon_{d+2} \approx p_{thr}/p$. You gain a bit less than an order of magnitude for error

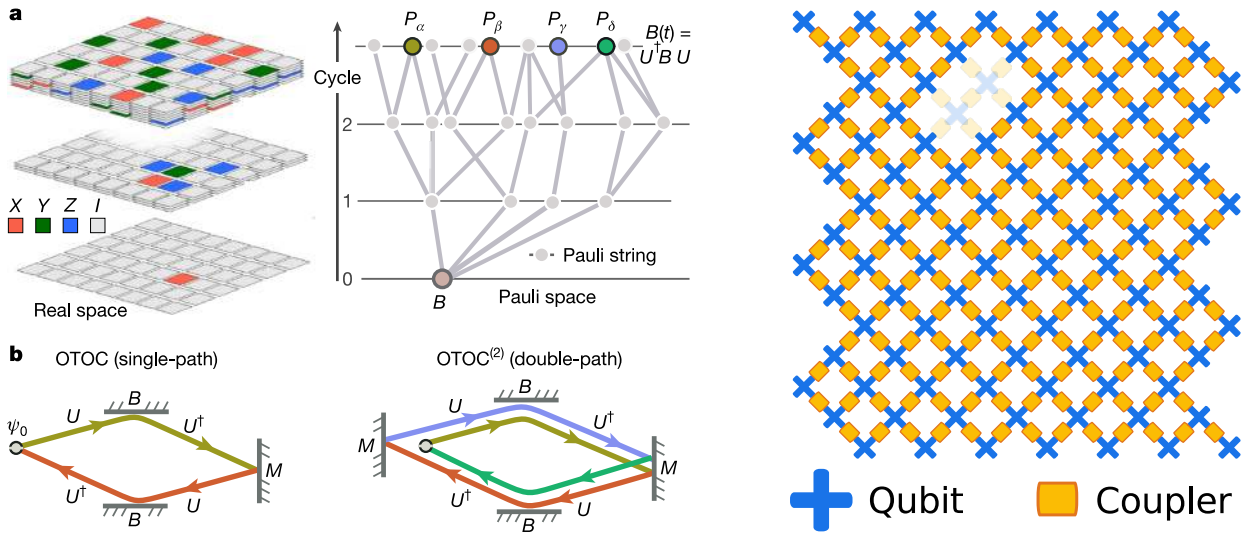

Figure 71: Google OTOC's "verifiable quantum advantage" experiment published in 2025 was using the iSWAP two-qubit gate version of Willow's processor, using 65 qubits out of the 103 functional qubits in the chip. In the 105-qubit chip, two qubits were not functional as seen on the right of this illustration. Only 65 qubits were used to accommodate for the limited available quantum volume. It was using about 1,000 two-qubit gates and quantum error mitigation. The "Quantum Echoes' experiment was simulating some quantum-chaotic system using a fixed circuits with random gates, with echo being used to detect some interferences. Google then implemented a NMR spectrography simulation reported in an arXiv paper and tested with only 9 qubits for toluene and 15 qubits for dimethylbiphenyl. It wasn't base on Google Echoes but used a variational Hamiltonian evaluation circuit built by the AlphaEvolve LLM. Sources: [122, 1035–1037].

How was Willow's chip initialized to correct its logical memory?

Willow's logical qubit experiment didn't involve the correction of single or two-qubit logical gates. But, the memory logical qubit had still to be initialized to some values to "correct" it. How did they do this?

It is relatively simple! They used the XZZX error correction code created by J. Pablo Bonilla Ataides in 2021 [1038] which corrects X and Z errors like most variants of the surface code. It uses "code stabilizers" alternating between XZXZ and ZXZX patterns across the qubit lattice. This structure enhances performance under biased noise (especially dephasing). They use logical operators X_L and Z_L which are defined as strings of Pauli operators across the code lattice for respectively a string of Z operators across one direction and of X operators across the orthogonal direction in the Bloch sphere.

They thus prepared the following eigenstates for X_L:

$$-|0_L\rangle, |1_L\rangle$$

And eigenstates for Z_L:

$$-|+_L\rangle = \frac{1}{\sqrt{2}}(|0_L\rangle + |1_L\rangle), |-_L\rangle = \frac{1}{\sqrt{2}}(|0_L\rangle - |1_L\rangle)$$

What is the meaning of L used everywhere? It corresponds to the fact that we are dealing with logical qubits where the qubit state is encoded across multiple physical qubits in the qubit chip.

rates by increasing the code distance by 4. As a result, to obtain 10^{-10} error rates, 7 orders of magnitude x 4 vs the distance-7 surface code would be required, landing in a distance d=7+32=39, which corresponds to 3,720 physical qubits.

But this is a low approximation. Google indicated in its paper that a 10^{-6} logical error rate would require a distance-27 logical qubit using 1,457 physical qubits. And this is without implementing any logical gate nor magic state distillation and T gate support. As a result, one interesting logical qubit will probably not fit in a single chip and will therefore require interconnecting several chips.

They also ran repetition codes up to distance-29 with as many qubits to correct only one type of (flip) error. They found that the logical performance was limited by rare, correlated error events occurring approximately once every hour, or 3×10^9 cycles. It creates a floor of 10^{-10} for logical qubit fidelities. This is better than the 10^{-6} contribution of correlated errors coming from cosmic rays. This progress may be linked to the implementation of gap engineering for their Josephson junctions, which was published earlier in 2024, thanks

to the work with Michel Devoret [637], and expanded in 2025 with 3D gap engineering [667].

In September 2024, Google researchers completed this work with proposing an efficient way to implement magic state "cultivation" (instead of distillation) for the creation of logical T gates [916]. It could potentially reach logical fidelities of 2×10^{-9}, and even 4×10^{-11} with halving the depolarizing qubit noise to 5×10^{-4} which remains challenging. It was experimented for the first time in 2025 [1040].

FTQC roadmap. Willow was a key milestone on the way to FTQC, but there's still a lot on Google's plate. They need to scale the number of supported physical qubits, with plans to host up to 10K qubits per chip, then to scale all control electronics accordingly, to interconnect these giant chips of 10x10 cm. And of course, to create a full-fledged FTQC architecture supporting logical gates and magic state distillation. Google's plans are to scale up to a million physical qubits (Figure 74). It now corresponds to the capability to break an RSA-2048 key according to a May 2025 paper from Craig Gidney [171].

In a July 2020 conference, Hartmut Neven announced his 10-year plan to achieve this result, showing impressive mockups of a giant quantum computer containing 100 modules, each with a single chip of about 10×10 cm hosting 10,000 physical qubits. It would be a giant installation, as shown on the impressive artist's rendering. This is still Google's roadmap as of 2026.

Since the Willow paper was first published as a preprint in August 2024, Google AI's team and particularly its rockstar Craig Gidney, published a wealth of papers related to the implementation of error correction and FTQC. The most important one may be related to magic state cultivation, an error correction scheme to create magic states very efficiently at a cost similar to a CNOT logical gate [916]. The was also one paper on a Tesseract syndrome decoder [1041], that may be better than the AlphaQubit machine learning based decoder that doesn't seem to scale well beyond distance-11 surface codes [1042]. An adaptive surface code taking into account defects in chips was also proposed [1043], as well as improved distillation factories [1044], dynamic surface codes with detect errors by alternating between different circuit constructions, providing greater flexibility in the choice of the types of gates, connectivity, and correlated error suppression [1045, 1046], and a denser planar surface code [1047].

Late 2025, the FLASQ paper described how to estimate resources to implement Google's QEC/FTQC playbook, particularly on how to manage spacetime tradeoffs [1048]. It described the relationship between physical qubit fidelities, time to solution, and the number of physical qubits, for a specific task like simulating a 11×11 2D Ising model. Other charts deal with QEC code distance and couple others show how and when NISQ combined with QEM (error mitigation) could be more efficient than FTQC (i.e. with better physical qubit fidelities, but starting with 25K physical qubits in Fig 5). The FLASQ Google paper contains a lot of assumptions: a 1 μs surface code cycle, required to execute the sequence of gates and measurements for one round of stabilizer measurements, 10 μs reaction time to implement a measurement, process the results classically, and communicate the action conditioned on the outcome of that processing to the QPU. 100 logical qubits with 630 physical qubits per logical qubit, all with 99.9% physical fidelities for all operations (gates, readout). And at last, no interconnect overhead despite the need for over 60K physical qubits.

Cryo-CMOS. To scale up micro-waves generation and put it inside the cryostat, Google published some work on a cryo-CMOS chip operating at 3K, using simple waveform generators consuming a minimum of energy to create only single qubit gates [1049, 1050]. It has however not yet been deployed. It relies on cosinusoidal shape microwaves with the interest of creating spectral "holes" corresponding to the qubits frequencies harmonics of the state $|1\rangle$ to the state $|2\rangle$ transition, that must be avoided (Figure 72). It corresponds to the wavelength known as ω_{12}.

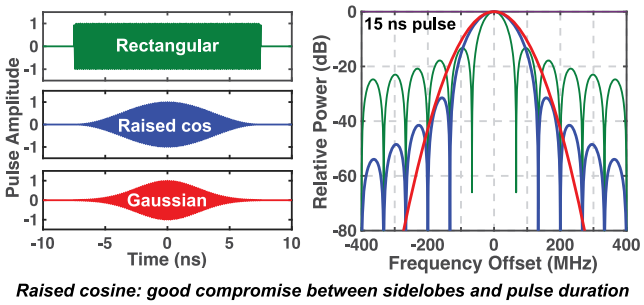

Figure 72: Qubit control signals optimization with spectral holes matching qubit frequencies harmonics. Source: [1051].

Applications. Starting in 2020, Google tried to make some good use of Sycamore, and then Willow, to test various algorithms:

- The chemical simulation of a diimide $(NH)^2$ molecule in 2020 [1053] and with three families of combinatorial problems using a QAOA algorithm [1054]. In 2021 [1055], together with researchers from Columbia University, Google's teams created a chemical simulation classical/quantum hybrid algorithm using a Monte Carlo method [1056, 1057]. It was used to compute the ground state of two carbon atoms in a diamond crystal, using 16 qubits. The method was, however, not more efficient than a full classical algorithm.

- Fundamental research activities like simulating time crystals, wormholes [1058] and even topological error codes [1059–1061]. There was no more supremacy since most of these experiments didn't use more than 20 qubits.

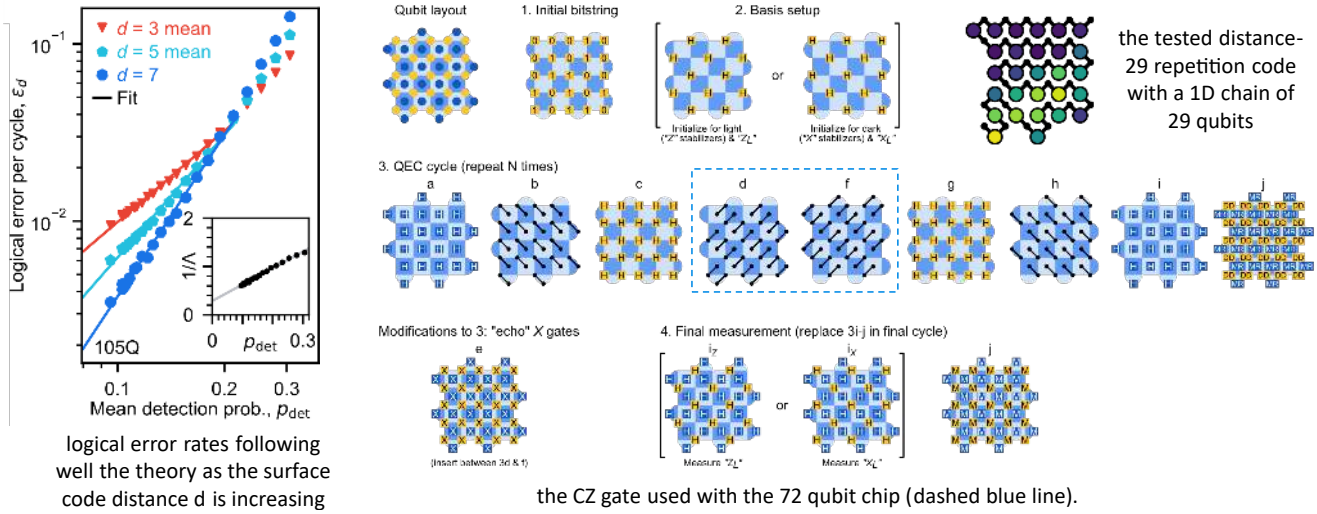

Figure 73: How the logical memory correction is implemented in the 72-qubit Google chipset from 2024. Source: [43].

Quantum error correction	–	Enabled	At scale
# Physical qubits	10 – 100	100 – 1000	10^4 – 10^6
# Logical qubits	–	1	10 – 1000+
Logical error	10^{-3}	10^{-2} – 10^{-6}	10^{-6} – 10^{-12}

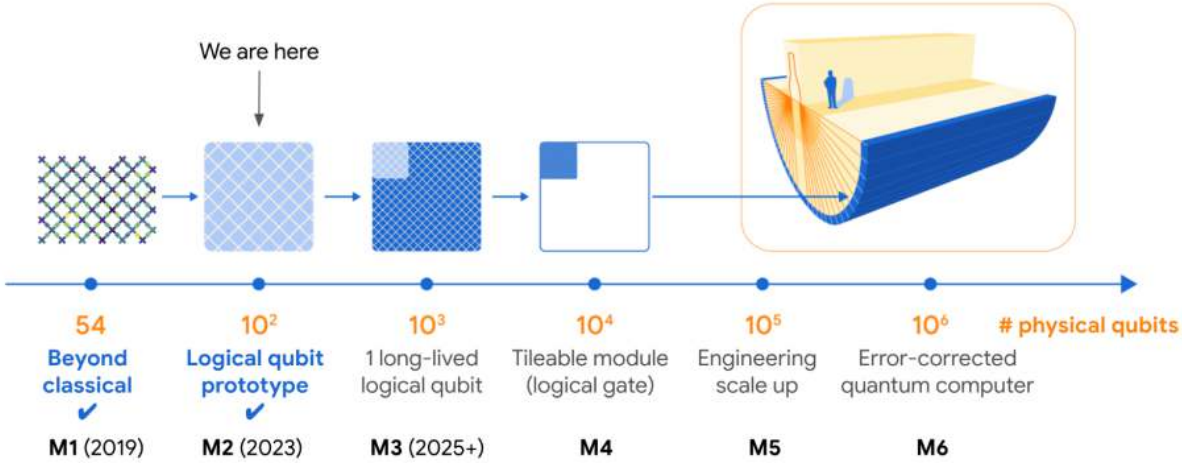

Figure 74: Google's scalability roadmap with logical qubits made of 1,000 physical qubits, as planned in 2020. And a giant system, as envisioned in 2020. One can wonder how these chips will be connected. At least, it will involve microwave connections, and at best, some longer range photonic connections. You can see that Google is late on the hardware side. It planned to reach 100 qubits by 2023 and it was done in 2024, then 1K qubits in 2025 and we've not seen it yet. Source: [1052].

- In 2021, Google teamed up with Caltech to show some quantum superiority when quantum computers directly exploit quantum data coming from quantum sensors. Fewer experiments are required than if the communication between sensors and the quantum processor was classical. The experiment was done with 40 qubits and 1,300 quantum operations, but with no quantum sensor [1062].

- In March 2022, another simulation of some molecules and materials was published, first with the iron-sulfur clusters of nitrogenase, including the FeMo-cofactor (aka FeMoCo), a component of the natural nitrogen cycle and second with the electronic structure of α-RuCl3, a candidate material for realizing spin liquid physics and Majorana fermions [1063]. The experiments were using 5 to 11 qubits, far from any quantum advantage territory.

- In November 2022, Google simulated the traversal of a wormhole with 9 qubits and 164 two-qubit gates, creating an obvious debate on its validity [1064–1071]. This can be emulated on a simple laptop and even on your smartphone.

- In June 2025, Google published a quantum advantage experiment on a quantum many-body physics

simulation to characterize ergodic dynamics using the second-order out-of-time-order correlators (OTOC). This workload that is hard to simulate classically was implemented on the iSWAP version of the Willow chip with 103 qubits (2 being non functional) using some error mitigation and with 65 operational qubits (Figure 71) [1072]. The chip has improved T_1 to about 98 μs on chip 2. The preprint became a Nature paper in October 2025 [122]. In 2026, Google teams completed their OTOC paper with another one describing why another quantum inspired technique, tensor networks with belief propagation (TNBP), couldn't simulate efficiently the OTOC experiment [1073].

- In 2024 and 2025, another fundamental physics simulation was also published, on a translationally-invariant lattice gauge theory (LGT) [1074].

- In collaboration with Abu Dhabi's TII, the University of Maryland, and Freie Universität Berlin, Google teams created a hybrid quantum digital-analog simulations using its Sycamore chip [580]. These analog simulations were implemented with sending sequences of mi-crowave and flux pulses to manipulate superconducting qubits and their couplers. The Sycamore chip allows dynamic tuning of qubit frequencies (μ) and nearest-neighbor hopping rates (J), while the qubit nonlinearity (ν) remains fixed. Each qubit is equipped with control lines for excitation and frequency tuning, and couplers have mechanisms to adjust hopping rates. During the experiment, qubit frequencies were ramped to a rendezvous point around 6500 MHz, with pre-distorted pulses compensating for filter effects. Simultaneously, couplers were ramped to set hop-ping rates, then both qubits and couplers were returned to initial states. Measurements were per-formed in the Pauli-X and Pauli-Y bases using frequency-multiplexed readout. The system was used to simulate the non-interacting part of the Bose-Hubbard Hamiltonian, modeling bosonic excitations as microwave photons. A novel classical algorithm, tensorESPRIT, applied tensor networks and super-resolution Fourier analysis to extract frequency data. Despite the sophistication of the experiment, no quantum advantage was achieved, with the experiment being limited to 14 qubits and a single initial qubit excitation.

- In 2026, Google researchers performed three analog simulations using superconducting circuits, one of superfluidity although without demonstrating some quantum advantage [1075], one of an interacting spin model in a disordered landscape to find evidence of a quantum glass phase [1076] and a third one on a 2D Ising-model to simulate some magnet [1077].

- One interesting advance was the DQI algorithm which could bring some exponential speedup for solving specific optimization problems [1078, 1079]. We discuss it in the algorithm part of this book.

- Google published a paper in March 2026 on new resource estimations to break ECC-256 keys [1080], using a zero-knowledge proof (ZKP) to demonstrate their algorithm without revealing its circuit. Such breaks using Shor's dlog algorithm would need about 10 minutes and half a million physical qubits. It drove a lot of additional fear about the quantum threat on cryptocurrencies. Google even pulled in 2029 the advice to deploy PQC. Whatever, we are still quite far from assembling 500K physical qubits with 99.9% operation fidelities (the paper assumption, as usual), whatever the qubit type.

Other research. Google AI researchers frequently publish interesting work on various topics. On an optimized way to prepare entangled states [1081], on NISQ-era many-body physics simulations using time-space symmetries [1082], on dispersion based qubit readout and qubit leakage with multiple photon number [673] and on the creation of solid state circulators using arrays of Josephson junctions [85]. Michel Devoret is also working on the planaron, a variation of the transmon qubit which could operate at higher temperature (above 1 K) [1083].

Software. Several Google teams are working on quantum software, including those working on Cirq, on TensorFlow Quantum and another Google X team working on applications, under the leadership of Jack Hidary, which later spun-off some of this effort in SandboxAQ [1084]. Google also released a **Fermionic Quantum Simulator** for quantum chemistry applications in collaboration with **QSimulate** (2018, USA, $4M) *aka* qsim. It can simulate noisy quantum circuits with Nvidia GPUs on Google Cloud. Since 2022, it seems branded as the Quantum Virtual Machine. Google also published **stim**, an open-source tool providing a 10,000x speedup when simulating error correction circuits.

In March 2024, Google and the GESDA NGO (Switzerland) launched the 3-year and $5M **XPRIZE Quantum Applications** global competition. It will award developing quantum computing algorithms that can solve real-world challenges as defined by the United Nations Sustainable Development Goals (SDGs), either on NISQ QPUs or in the future in FTQC systems [1085, 1086]. A first batch of up to 20 teams will share a $1M prize. Then, $3M will be shared among up to 3 grand prize winners, with $1M being split among runners-ups.

Quantum cloud. Google cloud offering includes a quantum algorithm emulator. It also hosts an IonQ trapped ion system and, surprisingly, none of its Sycamore systems which are only accessible to a handful of academic partners, an outreach strategy that is very different from the broadscale one IBM adopted. Google and IBM have very different commercial approaches with quantum computing. For Google, it is a research playing ground while for IBM, it is a way to lock-in large account customers as early as possible.

Rigetti

US, 2013, $942M

Rigetti was launched by Chad Rigetti, who got a PhD and did a post-doc at Yale University on microwave driven two-superconducting qubit gates in 2009 [1087]. He was a researcher at IBM between 2010 and 2013.

Company. Rigetti is a weird beast in the quantum computing landscape. It's the second oldest company after D-Wave but its technology and business achievements are really bad. Rigetti acquired QxBranch in July 2019 to complete its software offering. It was established in the USA, UK and especially in Australia. After having raised about $200M through classical VCs, they went into the stock market after being acquired by a SPAC company in March 2022, Supernova Partners Acquisition Company II. It brought in $345M for a valuation of $1.152B. As of December 2021, the company had 140 people in the United States, UK and Australia. Its quarterly results then drove its stock below $1, exposing the company to a Nasdaq delisting by July 2023. It then announced the layoff of 28% of its workforce and the departure of its CEO and founder, Chad Rigetti. In June 2023, Chad Rigetti left his own company and joined the Dutch investment fund QDNL Participations (Ground State Ventures since April 2026) as a venture partner. In 2025, he created Sygaldry, an AI+quantum company with fuzzy goals. Late 2024, Google Willow's announcement drove a market rebound which saved Rigetti from delisting. In November 2024, the company raised $100M through an at-the-market (ATM) stock offering. In June 2025, it did that again for $350M bringing them enough cash to last again a few years. In-between, in April 2025, they got a $35M investment from Quanta Computer (Taiwan), underlying their willingness to use Quanta (which has nothing quantum) for manufacturing some components of its computers. At their SPAC time, they were forecasting a revenue of $594M by 2026, based on the release of their 1,000-qubit system expected in 2024 (Figure 75). The 2026 expected revenue is $23M, with 2025 landing at $7.1M with a $216.2M net loss.

Technology. While Rigetti's qubit quality is not stellar at all, their technology developments are focused on chip design and assembly, and control electronics. They worked on multi-chip and inter-module connectivity, which could enable scaling their qubit numbers. They also work on 3D qubit control signal delivery, a technique also seen with other vendors like IBM.

- **Modular chips**. Rigetti is splitting qubits in multiple semiconductors dies connected with each other with indium-based flip-chip bonded on a single larger carrier die as shown in Figure 78.

- **Qubit count**. In about 12 years, their QPUs went from 3 to 108 qubits (Table 4). They prematurely announced a 128 qubits test version in August 2018 that never saw the light. They started to deploy their system on Amazon Braket with the 31-qubit Aspen-9 processor in 2020. Their Aspen-M 80 qubits chip announced in December 2021 was commercially available in February 2022 on Rigetti Quantum Cloud Services and Amazon Braket, and subsequently on Azure Quantum, Strangeworks QC and Zapata Computing's Orquestra platform [1088]. As of 2025, their flagship system was the Ankaa 84-qubit QPU. Early 2026, they released after some delay the 108-qubit Cepheus-1 system which is made of 12 9-qubit chips assembled on a chiplet (Figure 76).

- **Qubits couplers**. Their qubits were initially entangled using fixed configurable couplers. They then adopted tunable couplers in their Ankaa-1 and Ankaa-2 84 qubits chips, bringing more flexibility for managing two qubit gates (Figure 77) [1089]. These are adjustable transmon qubits using asymmetric SQUIDs (magnetometers). The Ankaa-2 chipset was delivered in January 2024, with 2-qubit gate fidelities of 98%. They are also studying dynamical decoupling between qubits to reduce crosstalk [1090] and ways to improve transmon frequency tuning [1091, 1092]. This strategy is very similar to what Google did back in 2019 with its first Sycamore chip and with IBM's technology starting with Heron in December 2023.

- **Qubit drive**. Rigetti made efforts to optimize the physical and electrical components of its QPUs by integrating the control and measurement wiring of the qubits in patented compact sheets [1093]. They developed their own qubit control electronics. They also found a way to limit crosstalk between qubits [1094]. They work on merging microwave and DC flux lines into the same wires used for respectively XY and Z single qubit gates, between the 10 mK cold plate and the qubit chip [1095]. This turned into CLOPS (circuit layer operations per second) improvements for their 40-qubit Aspen-11 and 80-qubit Aspen-M systems, from 844 to 892 CLOPS which pales in comparison to the 3.8 K to 5 K CLOPs of IBM QPUs as of August 2024. Their Ankaa generation were supposed to have two-qubit gates three times faster than with Aspen-M-3. [1096]. This reduces qubits crosstalk between modules, at the expense of a smaller fidelity. They first tried this with 4 chips containing each 4 aluminum- and niobium-based SQUIDs qubits and 4 static couplers, with fidelities of 99.1±0.5% and 98.3±0.3% for iSWAP and CZ gates [1097]. They then expanded this to two 40-qubit dies in their Aspen M1 chip released in December 2021. Other improvements include vertical signaling feeds, enabling higher qubit density, and using tunable couplers [1098]. This multi-die QPU approach is the main driving technology for them to scale their QPUs. The short term roadmap contains the 84-qubit Ankaa for 2023 and the 336-qubit Lyra for late 2023 (not delivered yet as of August 2026). They have however not yet explained how they will interconnect these multi-die chips [1099]. They are

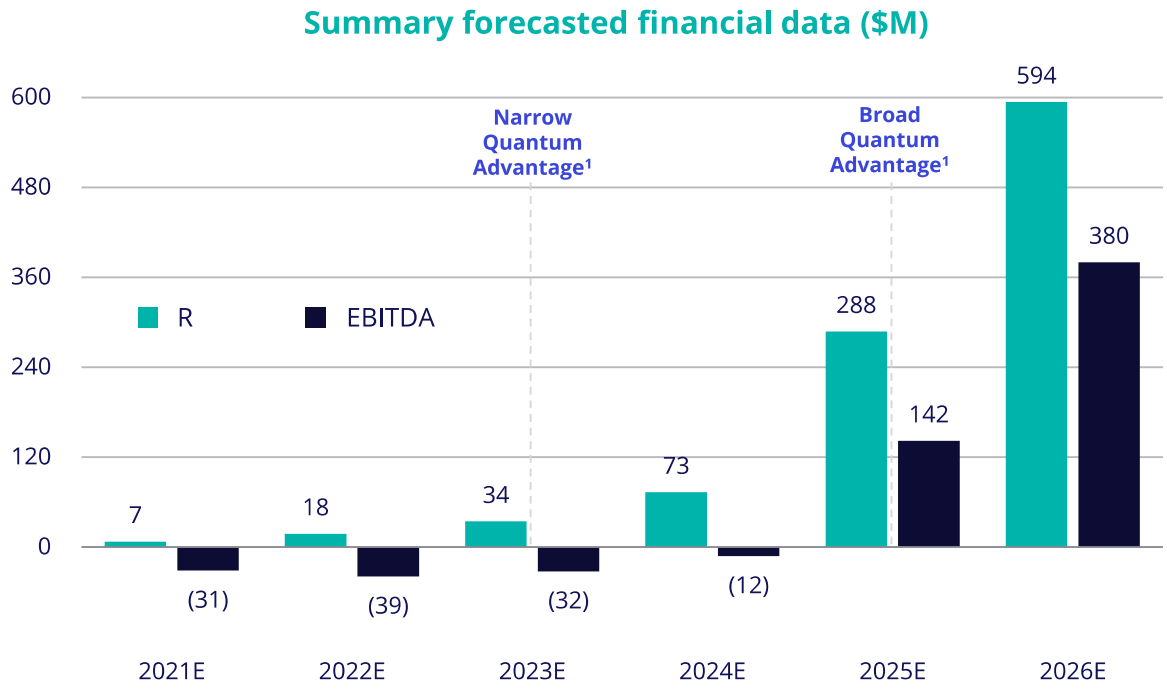

Figure 75: Rigetti's revenue and EBITDA forecasts until 2026 as shown in their Q1 2022 quarterly report. Their actual revenue was $8.2M in 2021, $9.1M in 2022, $10.1M in 2023, $11M in 2024 and $7M in 2025. They are far from $288M as well as from any broad quantum advantage. Comments updated in August 2026.

also developing an alternative bias annealing process for the precise tuning of their qubit frequency.

Manufacturing. Rigetti has its own research fab, named Fab-1, in Fremont, California (Figure 79). They invested between $10M to $20M, which is reasonable, even for a startup [1100, 1101]! Still, it is a challenge to use such fabs at full capacity. It may explain their five-year contract with the Air Force Research Lab announced in September 2023. It will cover various needs like quantum circuits, quantum-limited amplifiers, cryogenic microwave components. It was extended in 2025 with a $5.48M to cover the development of their ABAA chip fabrication technology (Alternating-Bias Assisted Annealing). In May 2026, Rigetti got $100M in funding from the US Department of Commerce for extending its manufacturing capability as part of the CHIPS Act, in exchange for some equity.

Qubit fidelities are not as good as with IBM but are continuously improving. In 2022, they demonstrated improved two-qubit gates fidelities of 99.5% but with a 9 qubits prototype while commercial QPUs are in the 95%-98% zone, which is not sufficient to run any useful NISQ algorithm [1102] (Table 4, Figure 77). The 84-qubit Ankaa-2 QPU has a 98% median 2-qubit fidelity. They were supposed to reach 99.5% two-qubit gate fidelities with 108 qubits in 2025. The system didn't perform well in an independent 2026 benchmark comparing them with other systems including IQM processors [1103]. In April 2026, Rigetti experimentally realized a 24 ns adiabatic CZ gate with fidelity exceeding 99.9%, and average fidelity of 99.874% [1104] (Figure 80).

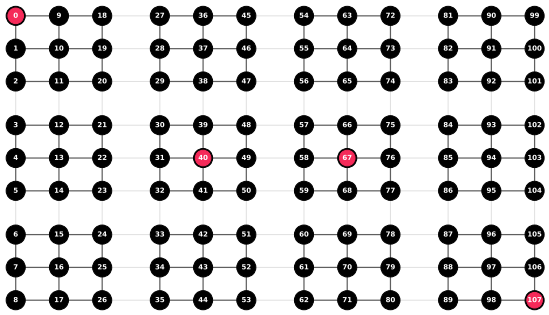

Figure 76: Rigetti's Cepheus 108-qubit processor made of 12 interconnected 9-qubit chips using microwave couplers. Source: [1105].

In December 2023, Rigetti launched Novera, a 9-qubit QPU at $900K. It is using a square lattice of qubits and tunable couplers [1107]. It has a 2-qubit gate fidelity of 98.5% with an iSWAP gate, which must be used multiple times to build a CNOT gate. This price only covers the processor and its control signals chain, but not the remainder of the quantum computer which is integrated by their customers, particularly the cryostat. Rigetti develops its own control electronics, named Tsunami.

In July 2025, Rigetti announced a "*twofold improvement in gate error rate vs the Ankaa-3 QPU*" with a 36-qubit QPU made with a 4-chip chiplet, each chip containing 9-qubits, and exhibiting a 99.5% two-qubit gate fidelity [1108]. You may wonder what "twofold" means given their December 2024 announcement said its Ankaa-3 84-qubit QPU already obtained a 99.5% median two-qubit gate fidelity [1109]. You have then

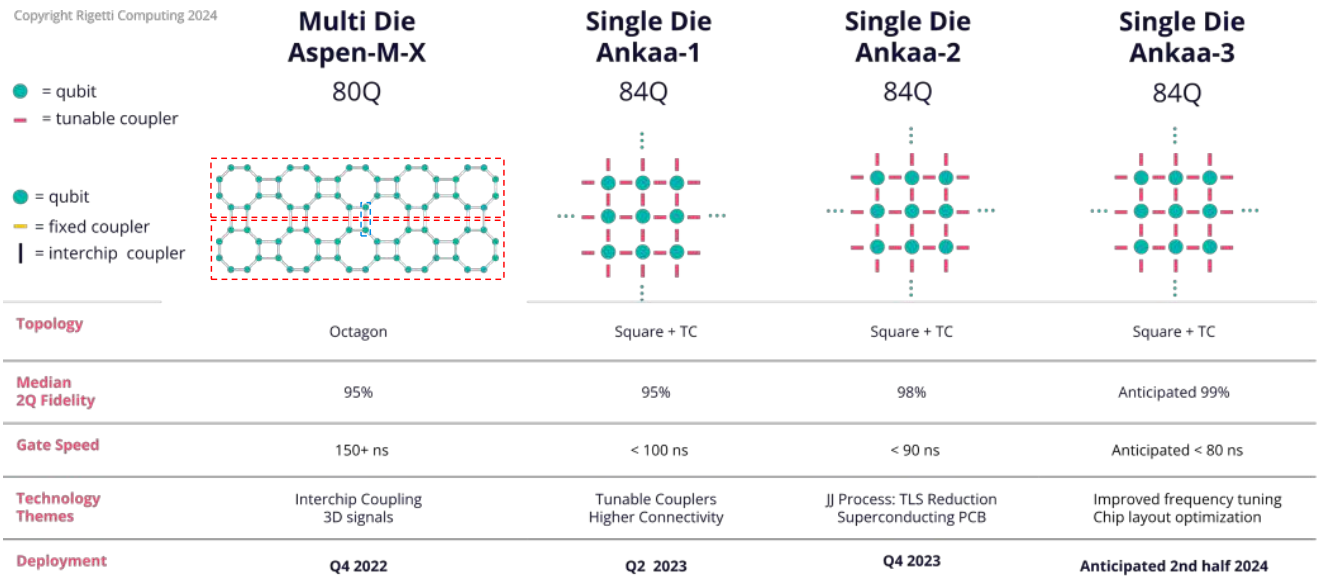

Figure 77: Rigetti's roadmap until the end of 2024. Their goal to reach 99% two-qubit fidelities is not in line with what is needed for both NISQ and FTQC, which require 99.9% fidelities. In red, the tunable couplers. Source: [1106].

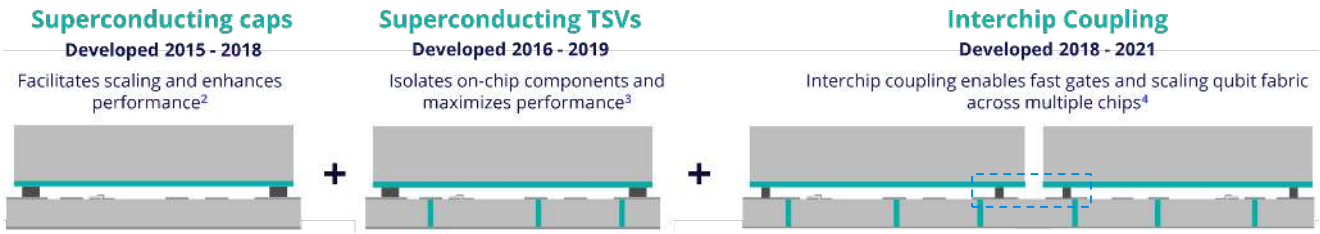

Figure 78: Interchip coupling implemented with their Aspen-M-1 80-qubit processor, assembling two dies of 40 qubits. Source: Rigetti.

Figure 79: Rigetti's superconducting cleanroom fab line in Fremont, California. Source: Rigetti.

99.5% fidelities with 84 qubits, and then the same fidelities with 36 qubits, which is a "twofold" improvement, by the way corresponding to the fidelities they had in 2022 with 9 qubits. The explanation is the following: Ankaa-3's fidelities where of 99% with iSWAP gates and it demonstrated 99.5% median fidelity with a parameterized NISQ gate fSim(θ, ϕ) which applies a partial SWAP between qubits (controlled by angle θ) and a conditional phase shift (controlled by angle ϕ). So we can presume that the 99.5% fidelity obtained in July 2025 was with an iSWAP gate, not a fSim gate.

Rigetti is also experimenting the usage of qutrits with three level anharmonic oscillators in their superconducting loops. It was tested in 2021 on a 5-transmon chip with two qutrits entanglement [1110, 1111].

Software tools. Their full stack offering includes pyQuil for scripting, Quil for quantum gate management and their Quantum Cloud Service. The first two are both open-source and published on GitHub. Quil allows tasks to be synchronized between quantum and classical computing [1112]. In 2018, they demonstrated the use of their quantum computer for a machine learn-

Metric	Aspen-9	Aspen-11	Aspen-M1	Ankaa-2	Ankaa-3	9x4 Chiplet
Physical Qubits	31	40	80	84	84	36
Median T1	27 μs	25.7 μs	30.7 μs	12 μs	–	–
Median T2	19 μs	14.9 μs	23.0 μs	13 μs	–	–
Median Simultaneous 1Q Fidelity	99.80%	99.50%	99.70%	99.42%	–	–
Median 2Q Fidelity	95.80% CZ 95.40% XY	90.20% CZ 93.70% XY	93.10% CZ 95.30% XY	96.56% CZ	99% iSWAP 99.5% fSim(θ, ϕ)	99.5% iSWAP
Median RO Fidelity	97.10%	98.20%	94.90%	–	–	–
Median Active Reset Fidelity	99.20%	99.80%	–	–	–	–

Table 4: Comparison of Rigetti quantum processors across key performance metrics. There are nuances on the supported two-qubit gate types. Having good two-qubit gate fidelities seems much easier with iSWAP gates than regular CZ gates. Different native entangling gates incur architecture- and compilation-dependent overhead when synthesizing a target gate such as CNOT or CZ, so raw fidelities measured on different native gates are not directly comparable. Sources: Rigetti press releases.

ing algorithm that does not require a hybrid algorithm [1113].

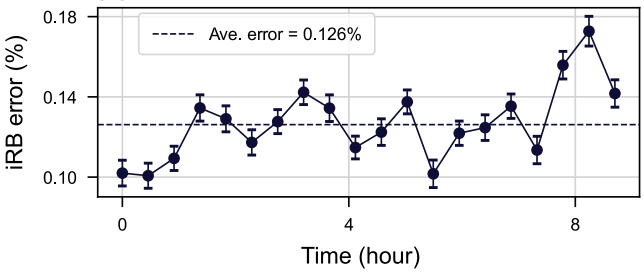

Figure 80: Rigetti's CZ experiment in 2026 showing a best case of a randomized benchmarked 99.9% fidelity, but an average fidelity of 99.874%. Source: [1104].

Roadmap. Rigetti's successive roadmaps have been revised repeatedly. In May 2022, the company announced a one-year delay on their roadmap [1114]. It updated its roadmap with basically removing long term goals with 1,000 and 4,000 qubits and focusing on 84 and 336 qubits NISQ platforms (Figure 81). In their new 2026 roadmap (Figure 82), their most ambitious goal is to deliver 1,000 physical qubits with 99.9% median fidelities and gate times below 50 ns. This should enable "logical gates". The roadmap does not yet state a code, a logical error target per operation or a physical-to-logical qubit ratio, which are the milestones needed to assess an FTQC path.

They need to find a way to improve their two-qubit gate fidelities and reach the 99.6% to 99.9% zone to compete with other vendors, and particularly with IBM as well as with all trapped ions QPU vendors. 2023 was supposed to be the year of a "narrow quantum advantage". We are not there yet. Focusing like this on short-term NISQ opportunities may be very shortsighted, if not a dead-end strategy.

Cloud. Rigetti offers access to its quantum computers via the cloud, like IBM and D-Wave do with their Quantum Cloud Services. It started running in beta in January 2019. Since early 2020, they are also distributed in the cloud by Amazon in its Braket service.

Partnerships. In September 2020, their UK-based subsidiary announced the launch of a collaborative project to accelerate the commercialization of quantum computers, funded with £10M private/public money. On top of **AWS**, **Microsoft**, **Zapata AI** and **Strangeworks** for cloud deployments, they announced in 2022 a new partnership with **Ampere Computing** (USA) to create hybrid quantum-classical computers designed to run machine learning applications, with **Keysight** for control electronics and **Bluefors** for cryogeny. Ampere is a fabless company designing 128-core arm chips for servers [1116]. With **Zapata**, they were building hybrid quantum-classical compilation tools with the support of the 80Q Aspen-M QPU and Rigetti cloud services. In May 2025, Rigetti signed a MOU with the quantum service company **Norma Partners** to launch an 84-qubit quantum cloud service in South Korea.

Rigetti also has various business and academic partnerships running in the UK. One led to the deployment in the UK at Oxford Instruments' Tubney Woods facility of a 32-qubit Aspen system in April 2024 [1117]. In February 2024, it got a Small Business Research Initiative (SBRI) grant from Innovate UK and funded by the National Quantum Computing Centre (NQCC) for a 24-qubit QPU to be deployed at the NQCC Harwell Campus [1118]. It got an Innovate UK funding for the development of some QML financial service [1119]. They also announced a partnership with **Riverlane**

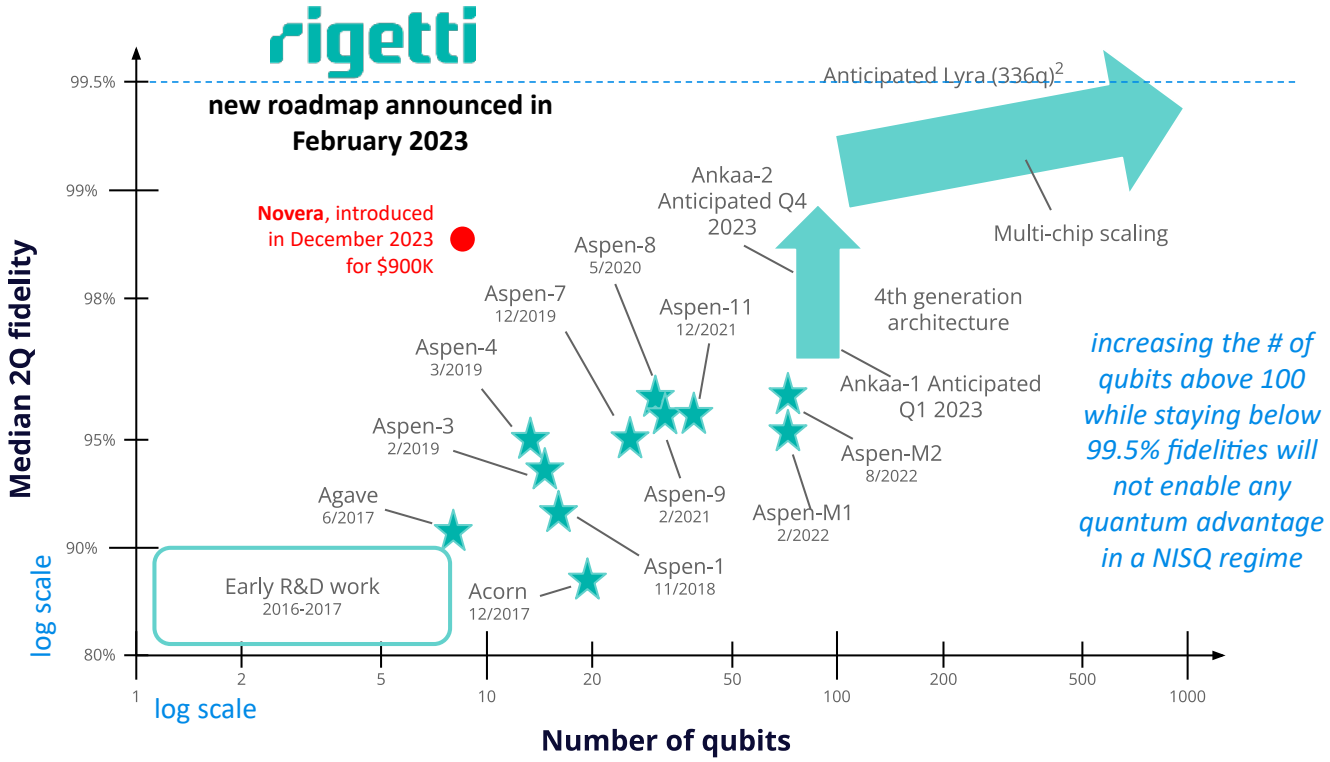

Figure 81: Rigetti's scalability roadmap update from 2023. They removed the 1,000 and 4,000 qubits QPUs that were announced in 2022, to focus on "shorter term" revenue opportunities. They expected to release a 336-qubit QPU in 2023, which is not done as of September 2026. Given their target fidelities, these chips will not enable any quantum advantage in the NISQ regime. Source: [1106].

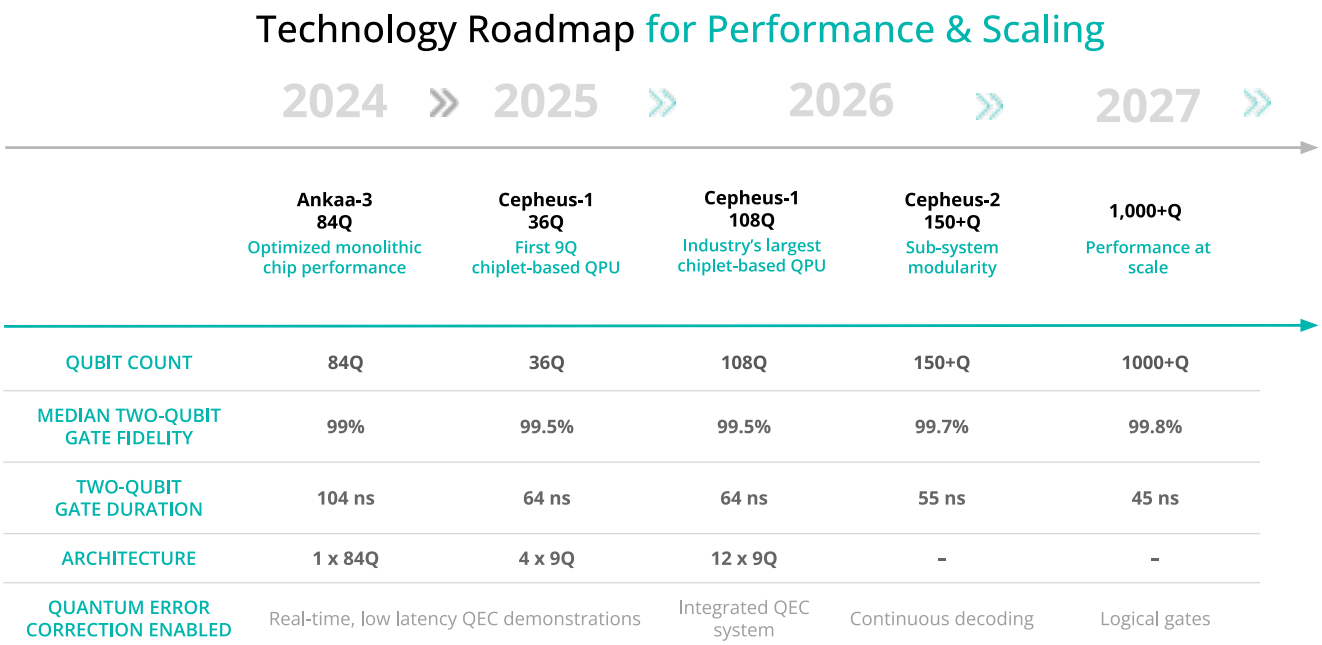

Figure 82: Rigetti's updated roadmap in 2026. Source: [1115].

(UK) in June 2022 to work on error correction [1120]. Then, in April 2025, Rigetti was selected to lead a £3.5M Innovate UK's Quantum Missions project to advance QEC on its superconducting quantum computer at the NQCC, with a 36-qubit QPU, Riverlane's error syndrome decoding stack. In September 2025, they announced a Memorandum of Understanding (MOU) with the Centre for Development of Advanced Computing (C-DAC) in India, an R&D organization from the Ministry of Electronics and Information Technology, for the development of hybrid quantum computing systems. In the UK, they are also partnering with QphoX, with a UK grant, to demonstrate an optical readout chain in Rigetti's Novera platform [733].

In the USA, Rigetti is working with **DARPA**, having been selected to provide hardware, software, and benchmarks for phase two of the DARPA ONISQ program (Optimization with Noisy Intermediate-Scale Quantum). The aim is to create quantum computers able to solve complex optimization problems. This work is jointly done with Universities Space Research Association (USRA) and NASA's Quantum Artificial Intelligence Laboratory (QuAIL). Rigetti has also a strong R&D partnership with the DoE **Fermilab**, which conducts testing and material designs in its Superconducting Quantum Materials and Systems Center (SQMS) led by Anna Grassellino [811]. They are working on using Nb/Si combinations and specific surface treatments, generating 450 μs T_1. They are also working with **NASA** on variational algorithms optimization techniques [1121]. In April 2025, they were one of the 16 companies selected by DARPA for their Quantum Benchmark Initiative program which is about funding prototypes leading to quantum utility FTQC systems in the future. One can wonder what roadmap Rigetti presented to DARPA!

Customers wise, they have a couple early adopters, like **Nasdaq** which plans to use their systems to detect fraud, optimize order matching and handle risk management. Rigetti sold the $900K Novera processor to Horizon Quantum Computing (Singapore) and delivered in April 2024 [1122], to Fermilab and AFRL in the USA, and to two undisclosed customers including some Asian technology manufacturing company (for about $5.7M). In September 2025, Rigetti was awarded a 3-year contract of $5.8M by AFRL to work superconducting quantum networking interconnect along with QphoX (the Netherlands). In January 2026, it announced the sale of their Cepheus-1 108-qubit system to India's Centre for Development of Advanced Computing. Rigetti also plans to invest up to $100M in the UK to deploy their upcoming 1,000+ qubit quantum computer. We would instead have preferred some revenue!

IQM

Finland, 2018, €525M

IQM is a spin-off from the Quantum Computing and Devices group of the Aalto University and from the VTT research center. Jan Goetz is their CEO.

Company. Its funding is a mix of dilutive capital investment and debt financing through the European Investment Bank with €33M in convertible options. In April 2025, the company announced it was planning to raise over €128M and it finally raised €275M in September 2025. They are by far the best funded quantum startup in Europe. IQM had about 400 people as of June 2026. They opened a research lab in Munich (with more than 80 people as of 2025), Germany in March 2020, one office in Spain in 2021, one in Paris and Singapore in 2022, one in Poland in 2024, including a partnership with Gdańsk University of Technology, one in South Korea in 2025, and one in the USA in Maryland in 2026. In 2026, they announced a SPAC and IPO which was achieved in July with a valuation of $2.7B as of July 7th. They became the first European Union listed quantum company, just before Pasqal. With a $36.2M revenue, they fare well above all other traded quantum computing companies, besides IonQ ($130M, but not only on quantum computing).

Technology. IQM develops superconducting qubits QPUs based on a variation of transmons, with tunable qubits, and tunable couplers for qubits entanglement.

- **Qubit topology**. Their topology is a nearest neighbor one, like the one in Google Sycamore. They had initially created an on-chip cooling technology for superconducting and silicon chips based on electron transfer using an electron tunnel-effect [1123]. It has a fast clock enabling about 2,800 CLOPS thanks to 6 ns single qubit gates, 30 ns two qubit gates and 300 ns readout time. On 20 qubits, their median two-qubit (CZ) gate fidelity is 99.51% across 30 qubit pairs, with a CZ two-qubit time of 48 ns [146]. They are also publishing interesting research work describing the various sources of noise in their qubits [1124]. They published in 2022-2023 a paper explaining how they plan to implement long-distance reliable two-qubit CZ gates, based on a custom ETH Zurich transmon design [1125]. It can reach fidelities of 99.8%. It will enable qLDPC codes for quantum error correction. It proposed a different approach in 2025 which is based on a resonator shared by multiple qubits as part of their Star topology [1126] (Figure 83). IQM is partnering with UC Berkeley and Irfan Siddiqi's team to design 3D-integrated versions of their qubit chips with high quantum coherence and low crosstalk [1127].

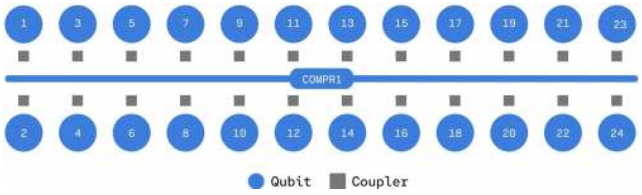

Figure 83: The IQM star topology with a share resonator between 20 qubits. Source: [1128].

- **Qubit fidelities**. In August 2025, IQM published a preprint reporting single-qubit gate, two-qubit gate and readout fidelities each at or above 99.9% [1130]. These are three distinct metrics, obtained on a laboratory two-qubit prototype, and they do not establish processor-scale performance or a modality-wide record. The paper showcases a graph consolidating error sources Figure 88. The chip was optimized with a digital simulation and to handle trade-offs between two-qubit gate speed and single-qubit gate fidelities. Readout is using separate resonators and Purcell filters for each qubit which is commonplace

Figure 84: IQM Spark 5-qubit CPU. Source: IQM.

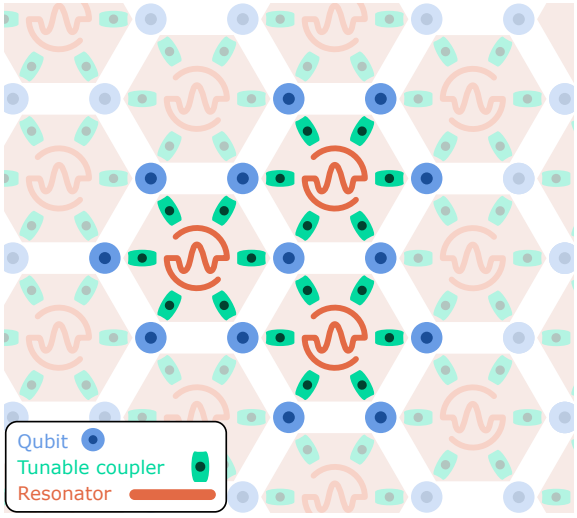

Figure 85: IQM 2D Constellation layout extending the Star architecture. Source: IQM in [1129].

with commercial vendors. Resonators and Purcell filters mutualization between qubits was only tested in academic labs, by RIKEN, the University of Tokyo and ETH Zürich [726].

- **Qubit drive**. IQM creates most of its qubit control electronics in-house, particularly to optimize pulse shaping methods [1131]. It participates in a research consortium including Aalto University and VTT which proposed in 2021 a qubit on-chip circuit to create microwaves pulses that could be used to drive superconducting qubits and working at 10 mK [1132, 1133]. Its size is one mm and would remove the need to use cables to feed the processor with microwave pulses. So far, it only creates a sinus wave at 1 GHz, still far from what is needed to drive a superconducting qubit, i.e., a short duration pulse with a precise waveform added to some carrier frequency at around 5 GHz. It is closer to a local oscillator source. IQM also uses a TWPA from VTT in the first stage amplification of qubit readout microwaves [1134]. They are also experimenting qubit readout mechanism using a bolometer, which so far has a low fidelity of 61.8% due to the readout duration of 13.9 μs that is constrained by a T_1 of 28 μs [1135]. This fast graphene-based bolometer can detect a single microwave photon. Its benefits are some power saving compared to parametric amplifiers.

Manufacturing. After relying on VTT Micronova 2,600 m^2 clean-room fab, they inaugurated their own Espoo 560 m^2 and a 200 mm wafer €20M fab in November 2021 to manufacture their chips, a self-sufficiency strategy also seen with Rigetti. This cleanroom enabled them to produce a test chip with 99.9% two-qubit gate fidelities and 1 ms coherence times. These gate fidelities were measured on multiple pairs of qubits with an unspecified number of qubits [1136]. In May 2024, IQM announced it would invest €100M in France to put in place superconducting chips industrial capabilities manufacturing, first with a pilot line at CEA-Leti in Grenoble [1137].

Products. Its QPU generations are Pyrite (5 qubits, available), Deneb (6 qubits, available [1138]), Garnet (20 qubits, available and thoroughly benchmarked [1139]), Kade (54 qubits, for 2024, which became Radiance, and was delivered in 2026) and Selenite (150 qubits, planned for delivery in 2025). In August 2023, the company announced its commercial launch of its Spark system with 5 qubits aimed at the academic and enabling technology vendors market, priced at around €1M [1140]. As of September 2024, it had manufactured 30 QPUs. IQM also offers customized hybrid analog/digital "Co-Design QC" QPUs [1141, 1142]. They work on this with partners like Infineon at the LRZ supercomputing center in Garching, near Munich in Germany [1143, 1144]. In November 2021, IQM was officially selected to provide its quantum computer to LRZ (Leibniz Supercomputing Centre) in association with an HPC to set-up a hybrid computing system as part of the Q-Exa project. It's part of a €45.3M consortium project funded by BMBF (German Federal Ministry of Education and Research) with €40.1M. The system was deployed officially in June 2024 with 20 qubits. I saw it in LRZ (Munich) in October 2024.

Their co-design offering is based on **KQCcircuits**, an open-source software tool based on KLayout for qubit design, using the OASIS format for masks that is lighter. It enables graphic-based creation of circuits elements and contains a library with SQUIDs, complex waveguides, coplanar capacitors, qubits, flip-chip bonding connectors, indium bumps and other templates.

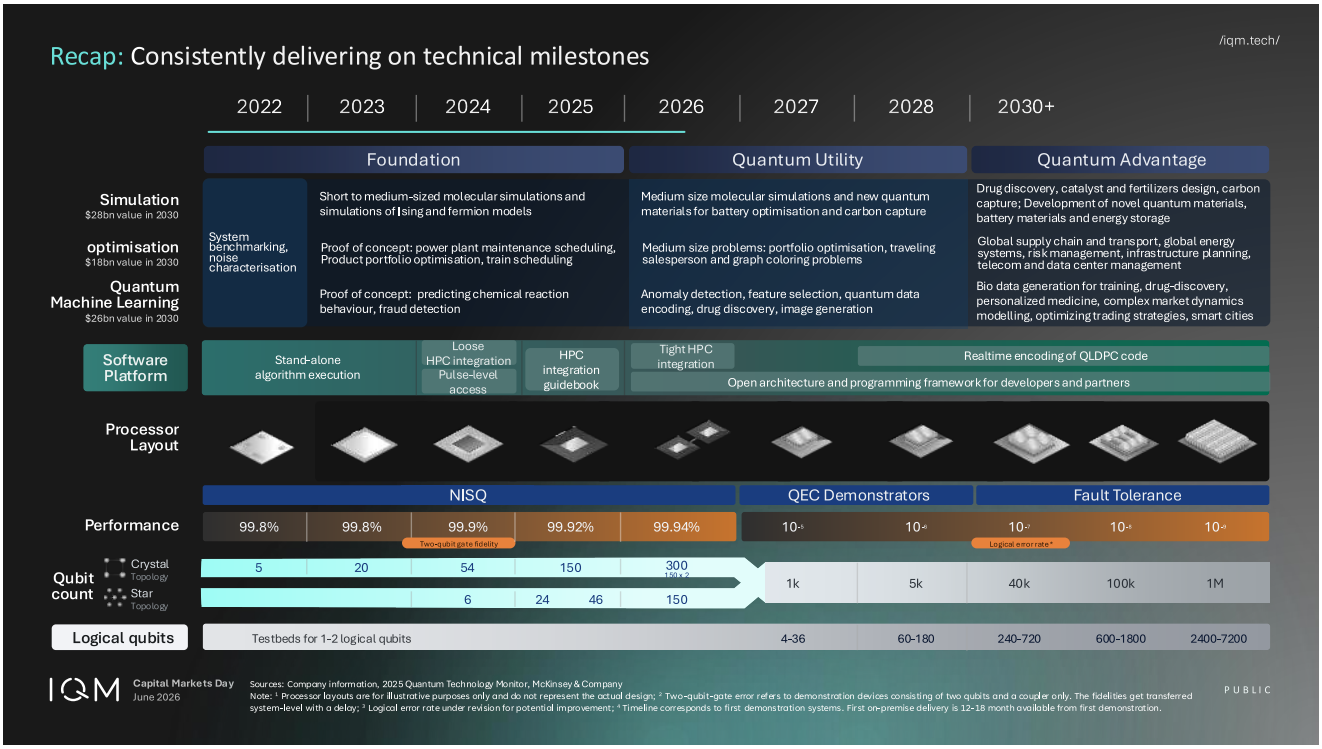

Figure 86: IQM's updated roadmap as of June 2026. It has not changed since 2025. Source: [1145].

In March 2024, IQM launched its QPU cloud offering Resonance providing access to their Garnet 20-qubit QPU with a friendly user interface [1147].

FTQC roadmap. The company updated its roadmap in November 2024. It targeted two-qubit gate fidelities of 99.94% by 2026, first logical qubits around 2027, and later thousands of logical qubits from much larger physical-qubit systems. The source roadmap is a vendor projection rather than an experimental result. At the qubit level, they plan to merge their crystal and star topologies by 2027 to enable qLDPC quantum error correction, in their planar star lattice Constellation layout [1129]. They are working with **Riverlane** for quantum error correction syndrome detection. IQM is also collaborating with the Taiwan Semiconductor Research Institute (TSRI) on cryo-CMOS control electronics for future scalable designs [1148]. It acquired a Spark in 2024. They updated their roadmap around their IPO in June 2026, with not much change besides the impact of their Barbell qLDPC code Figure 86.

In 2026, IQM developed their Barbell codes, a variant of qLDPC codes which uses what they call near local couplers with a fixed connectivity, a bit similar to the additional couplers in IBM's Loon architecture. These couplers will be created with using bump bonds, through-silicon vias (TSV) and a special single interconnect layer thanks to using parallel connections [1149] (Figure 89). The related chip hadn't seemingly been experimented yet as of mid-2026 but the technique is documented by the MIT in [1146] (Figure 87). At the physical level, they also presented a qubit frequency optimization using pulse shaping to reduce crosstalk in single-qubit gates [1150] as well as a reduction of TLS losses (two-level system) using tantalum coplanar waveguide resonators fabricated on high-resistivity silicon substrates through the use of an ultrathin titanium sacrificial layer [1151].

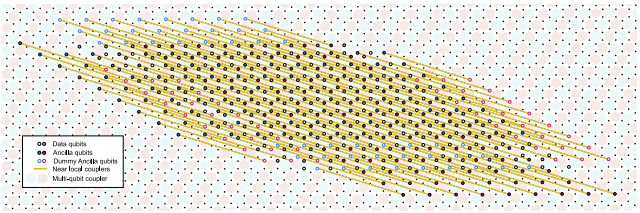

Figure 89: IQM's Barbell's qLDPC codes leverage a one layer additional near local couplers connectivity (in yellow). Source: [1149].

Partners. IQM is partnering since August 2022 with **Multiverse Computing** on various fraud detection, quantum reinforcement learning and quantum reservoir computing use cases, and since July 2024 with **Quantistry** for the chemical and material industry. They are part of the German project QLindA on quantum reinforcement learning along with **Siemens**, **Ostbayerische Technische Hochschule Regensburg**, and **Friedrich-Alexander-University Erlangen-Nuremberg**. They work on various case studies on fermionic simulation of battery oxidation, on carbon capture, on dynamic mean field theory, using quantum error mitigation. They also have one case study of NMR physics simulation, implemented in Spain [1152]. They work with **Eviden**/Atos together with the Finnish supercomputing center **CSC** which bought a classical

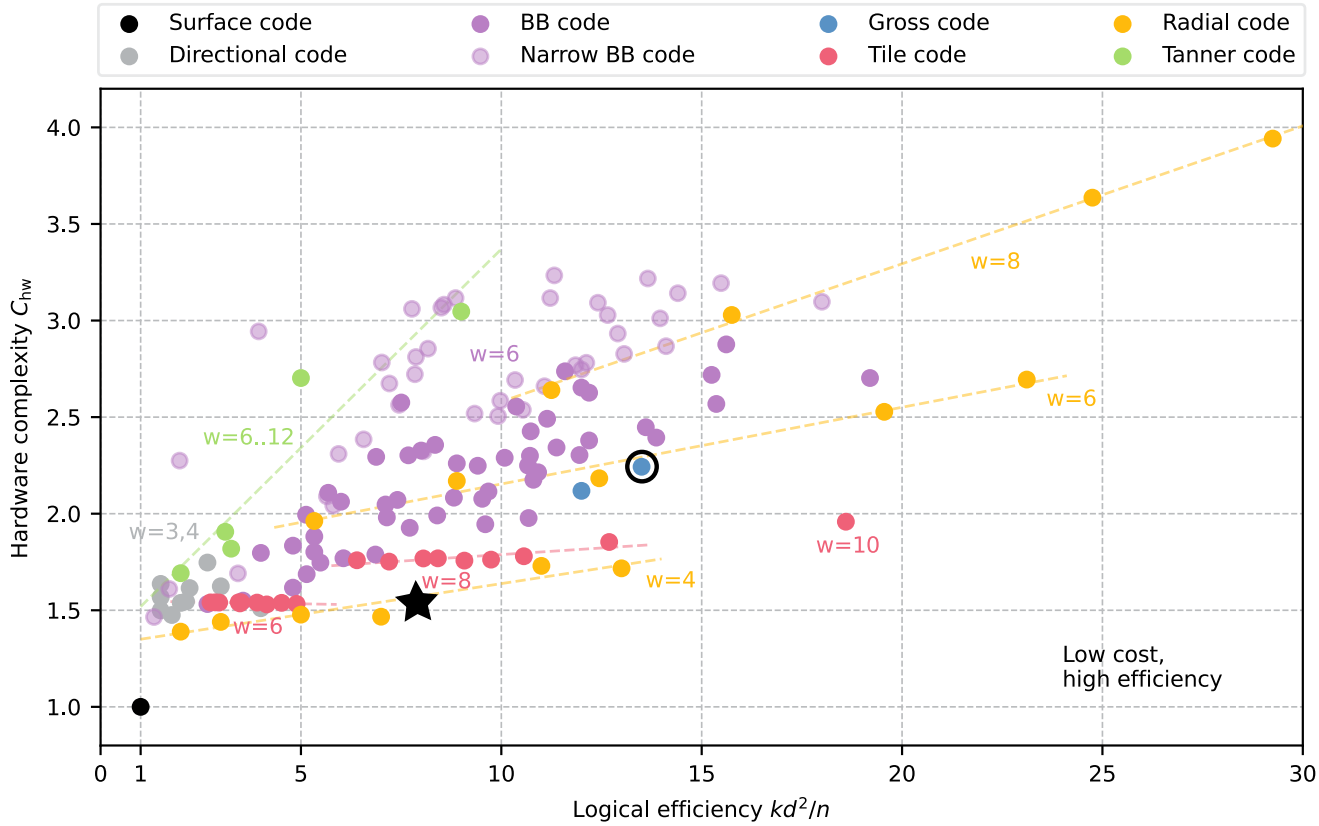

Figure 87: Chart showing surface code and qLDPC efficiencies. The X-axis shows the logical Efficiency (kd^2/n), which measures how effectively a quantum code stores information compared to the standard surface code which is the dot at 1 (X) and 1 (Y). A higher number means the code performs better and uses physical resources more efficiently. The Y-axis shows hardware Complexity (C_{hw}) and evaluates how difficult the chip will be to physically manufacture. A score of 1 represents a simple, single-layer design with nearest neighbor connectivity. With higher score, the physical chip is more complicated to manufacture with additional extra routing layers, longer wire connections, and more transitions between layers. Since you want a chip that is easier to build, being down is better. The black star positions IQM's Barbell code implementation. The black circle shows IBM's qLDPC implementation. Recreated using Fig 3. from [1146] and IQM's additional data from slide 32 in [1145].

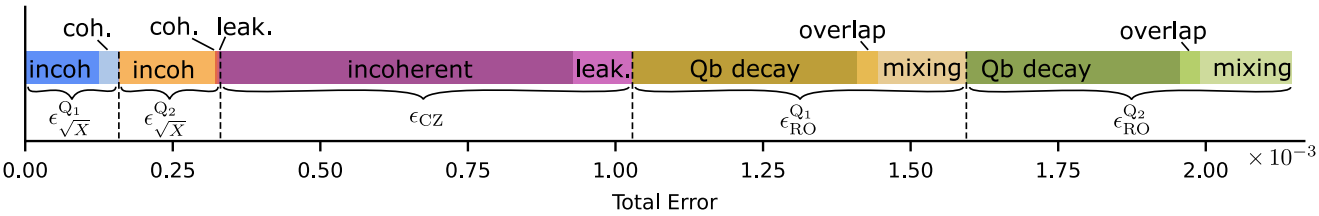

Figure 88: This chart decomposes error sources in the two-qubit 2025 IQM chip with single gate qubit errors, two-qubit gate errors (CZ) and the two related qubit readout errors. The total error is 2.1×10^{-3}. The two main error sources are the two qubit gates and readout errors. Source: [1130]

QLM emulator for their services. This machine is used both to simulate the operation of IQM's quantum accelerator qubits and to drive it [1153]. In December 2022, IQM announced a partnership with **Tech Mahindra** (India) covering quantum computing, cryptography, and communication technologies for the development of customer software solutions. IQM launched a partnership with HPE on the integration of QPUs and supercomputers and a 20-qubit Garnet QPU was made available on **AWS** braket in May 2024. IQM is also working with **HQS** (Germany) on quantum chemistry simulations [1154]. IQM is also partnering with Volkswagen. In 2024, they introduced the CS-AFQMC hybrid method, to improve chemical simulations accuracy using fewer qubits in applications like battery de-composition and nitrogen dimer modelling [1155].

Customers. In 2020, the Finnish government granted VTT with a €20.7M funding to acquire an IQM system. It was supposed to reach 54-qubit by 2024 and 150 by 2025. A 50-qubit QPU was finally delivered to VTT in March 2025. The delivery of the 150-qubit QPU was postponed to 2026, with an addition of a 300

qubit QPU planned for 2027, and using two 150-qubit chips. Beforehand, they had 5 qubits as of November 2021 and 20 as of October 2023. 5-qubit and 20-qubit were delivered to VTT as well as to LRZ in Germany, plus a 54-qubit QPUs named Euro-Q-Exa also to LRZ (in 2026), and a Spark to the Jülich Supercomputing Center as well as to Polytechnico Milano. IQM also signed an MOU with the quantum security specialist Norma in South Korea to enter this market [1156]. IQM also won a contract to deliver a 24-qubit QPU to the IT4Innovations National Supercomputing Center in Ostrava in Czechia, as part of the EuroHPC JU. It will be connected to the EuroHPC petascale supercomputer Karolina that is operating since 2021. In April 2025, IQM sold a Spark to the Wrocław University of Science and Technology and in 2026 a Radiance 54-qubit system to GALAXY Systemy Informatyczne in Poland. It also installed a Spark at Chungbuk National University in South Korea. In December 2024, IQM signed a scientific partnership MOU with AIST in Japan dealing with quantum hardware development, algorithm optimization, error mitigation, and machine learning. In Japan, they also initiated in 2025 a sales distribution agreement with Toyo Corporation and sold them a Radiance system. At last, in August 2025, IQM installed a 20-qubit QPU at the Oak Ridge National Laboratory in the USA, a premiere for a European company. In June 2026, a Radiance 54-qubit system named "NOX" was installed at CINECA in Bologna, Italy.

OQC

UK, 2017, $496M

Oxford Quantum Circuits was launched by Peter Leek from Clarendon Laboratory Oxford and Ilana Wisby who was their CEO until May 2024

Company. The current company leadership is Gerald Mullally (CEO), Simon Phillips (CTO) and Peter Leek (CSO). It had a team of over 150 people as of mid-2026. It is now the best funded quantum startup in the UK, thanks to a funding round of $350M closed in June 2026. Beforehand, in November 2023, the company had announced a funding round of $100M, led by SBI Investment from Japan [1157]. But, surprisingly, Chevron joined this funding round in March 2024, which may mean that the $100M November 2023 funding round was not completed back then [1158].

Technology. OQC's technology was initially based on their "coaxmon" superconducting qubits architecture that were composed of highly coherent planar qubits [1159] and using a 3D structure connecting the qubit chip with an interposer and using a layer for controlling the qubits on top of the chip and another one below for qubit readouts. The 3D layering and TSV structure was inspired by a project funded by IARPA [1160]. It was based on research from MIT and the University of Oxford, on an idea from Peter Leek [415, 1161, 1162]. In 2024, they disclosed an electron-beam annealing technique that improves the quality of their qubits which it seems was implemented for a long time by IBM [1163], a technique to implement TSVs (through-sapphire-vias instead of the typical through-silicon-vias) to implement vertical connectivity in their superconducting chips [1164] and a solution to multiplex readout signals using a "3D re-entrant cavity filter", demonstrated with only 4 qubits with an average readout fidelity of 98.6%.

Then, in 2025 came many other scientific advances. A 25 ns CZ with 99.8% fidelity [1165], based on using a dual-rail qubit design was tested in Peter Leek's lab [530], reduced crosstalk on a matrix of 4x4 qubits [1166], a model to improve the cryogenic capacity of their platform for I/O scaling [39] and finally, some work on their chip characterization to improve their manufacturing process [1167]. Other work published in 2025 related to reducing crosstalk [1168] and in 2026 to the improvement of Purcell filters [1169].

The coaxmon is OQC's three-dimensional packaging architecture, while the dimon is a multimode superconducting circuit used to realize a dual-rail encoded qubit (Figure 90). Calling the inner dual-rail encoding a "logical qubit" is defensible at the code-encoding level, but it is not a fully fault-tolerant logical qubit. The architecture is designed to convert dominant loss events into detectable erasures, while residual Pauli errors, including dephasing, still require an outer QEC code [529].

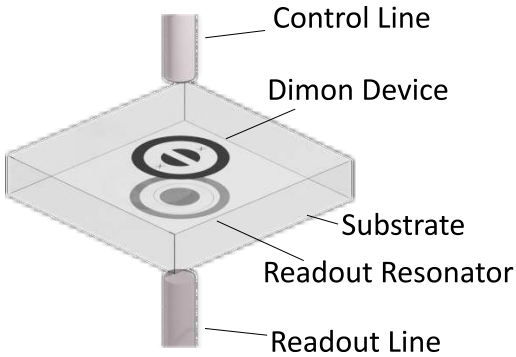

Figure 90: The dimon qubit sits inside the coaxmon architecture for the implementation of a dual-rail mode which enables erasure detection and simplified quantum error correction processes. Source: [530].

Cloud. In July 2021, OQC announced that they were making their first system available only as a QCaaS solution, in private beta (quantum cloud as a service) without even saying how many qubits were deployed. They then announced in December 2021 that an 8-qubit version of their processor nicknamed Lucy would be made available on Amazon Braket and revealed that their July 2021 system had a mere 4 qubits. The OQC system became live on AWS Braket in February 2022.

Qubit Fidelities. Late 2022 during the Q2B and thanks to various third party benchmarks, it became possible to access OQC's qubit fidelities data. The fidelity of the OQC Lucy 8 qubit QPU goes from 89.9%

to 96.8% depending on the qubit couplers in the chip. The single gate fidelities are above 99.72% with a record 99.8% obtained in lab for a CZ two-qubit gate. T1 is between 22 μs and 58.1 μs [1170]. In March 2023, OQC and Equinix also announced that their QPU will be deployed by Equinix to provide cloud access to worldwide customers [1171]. Their 32-qubit Toshiko QPU was delivered to Equinix in Japan, in November 2023, touting "colocation" capabilities in HPC datacenters. OQC presents this as enabling "*enterprise ready* $x^{2}2x^{2}$*lutions*" which is clearly overstated given 32 noisy qubits can easily be emulated on a single PC. The qubit median figures of merit were disclosed later: T_1 of $78\mu s$, a T_2 of $104\mu s$, single-qubit fidelity of 99.9% and two-qubit fidelity of 96% (not stellar, presumably a CNOT gate).

Roadmap. In June 2025, OQC published an FTQC roadmap targeting 16 logical qubits for Genesis, 200 for Titan in 2028 and 50,000 for Atlas in 2034, with Atlas specified at a 10^{-12} logical error rate on a 300 mm wafer [9] (Figure 91).

Software Tools. They are partnering with Cambridge Quantum Computing (CQC) which is developing a quantum compiler dedicated to their qubits. They also work with Classiq since December 2023. In April 2020, OQC obtained collaborative project funding from the British government of £7M. As part of this project, they are associated with SEEQC UK, Oxford Instruments, Kelvin Nanotechnology, the University of Glasgow and the Royal Holloway University of London.

Customers. In April 2023, OQC announced the sale of their future 32 qubit QPU to CESGA in Spain and the creation of a knowledge center in Galicia in September 2023. This will be complemented by Fujitsu's 34 qubit quantum computer simulator running on the FX 700, the FUJITSU Server PRIMERGY HPC. In September 2025, OQC announced it sold a 16 logical qubit QPU to the cloud hyperscaler Digital Realty in New York. It was installed with the GENESIS system in New York City, and supposedly operate hybrid AI/quantum workloads.

Case study. In April 2024, OQC released a case study of chaotic systems simulation for weather forecast, using a hybrid quantum reservoir-computing method on their 8-qubit Lucy QPU, way from any quantum advantage or utility regime [1173, 1174].

Intel

USA, 1968

Intel is another player in the superconducting qubits field. With no commercial solution so far as it is only a research field at this stage, completed by to the more natural avenue of electron spin silicon qubits they are also pursuing. At CES 2018, Intel's CEO proudly showcased a 49-qubit superconducting chip during his keynote, stuck between a passenger drone demonstration and a broad talk on artificial intelligence.

Named Tangle Lake, the chip was tested at **QuTech** in the Netherlands. They were at 7 qubits at the end of 2016, 17 qubits at the end of 2017 and 49 (uncharacterized) qubits in January 2017. Since then, no news. It seems that Intel is now entirely focused on electron spin qubits, along with their partner QuTech in The Netherlands, where they invested $50M back in 2015.

Anyon Systems

Canada, 2014, $17M

Anyon Systems was created by Alireza Najafi-Yazdi. Their physics team is managed by Gabriel Éthier-Majcher and the startup had about 20 employees as of mid-2023.

The CEO and cofounder adopted a full stack approach, creating custom control electronics, dilution cryogenics and nearly custom anything.

They started by creating their Quantum Device Simulator (QDS), a software tool used in quantum computer design and simulation that can run on supercomputers. It was used by John Martinis's Google team in 2017 for the design of their superconducting 6 and 20-qubit processors [1175]. Their software was mainly used to predict the level of adjacent qubits crosstalk. It is part of Snowflake, an open-source library for creating quantum circuits running both on quantum emulators and quantum computers. Their main goal then became to create superconducting qubits quantum computers.

Their first 6-qubit system was deployed internally in 2021. They published related qubit fidelities data in March 2022 with 99.7% for single qubit gates and 95.6% for two qubit gates [1176]. Their T_1 is 10 μs and T_2 is 8 μs, which is quite low, but is compensated by fast gates of about 20 ns.

Their chip is manufactured at the Quantum-Nano Fabrication and Characterization Facility (QNFCF) from the University of Waterloo in Canada (Figure 92, *left*).

They planned to deploy a 12-qubit system named Monarq in 2023 for Calcul Québec, a regional hybrid HPC-quantum computing research facility whose HPC hosts 1,500 Nvidia GPU. It became a 25-qubit system, deployed in May 2024. Their plan is to improve the quality of their physical qubits to deliver utility quantum computing, without relying on quantum error correction.

Software wise, they plan to support Cirq and Qiskit frameworks. Another system was delivered in 2024, for the École de Technologie Supérieure of Montreal, Québec.

I had the opportunity to visit their headquarters and integration laboratory in May 2023 in Montréal, Québec. The machines are real! Their Monarq system has a rather large cryostat with very large low-level cold plates of about 60 cm wide (Figure 93). It is supposed to accommodate up to 56 qubits, which may mean that their dilution yield is rather low given the size of the cryostat.

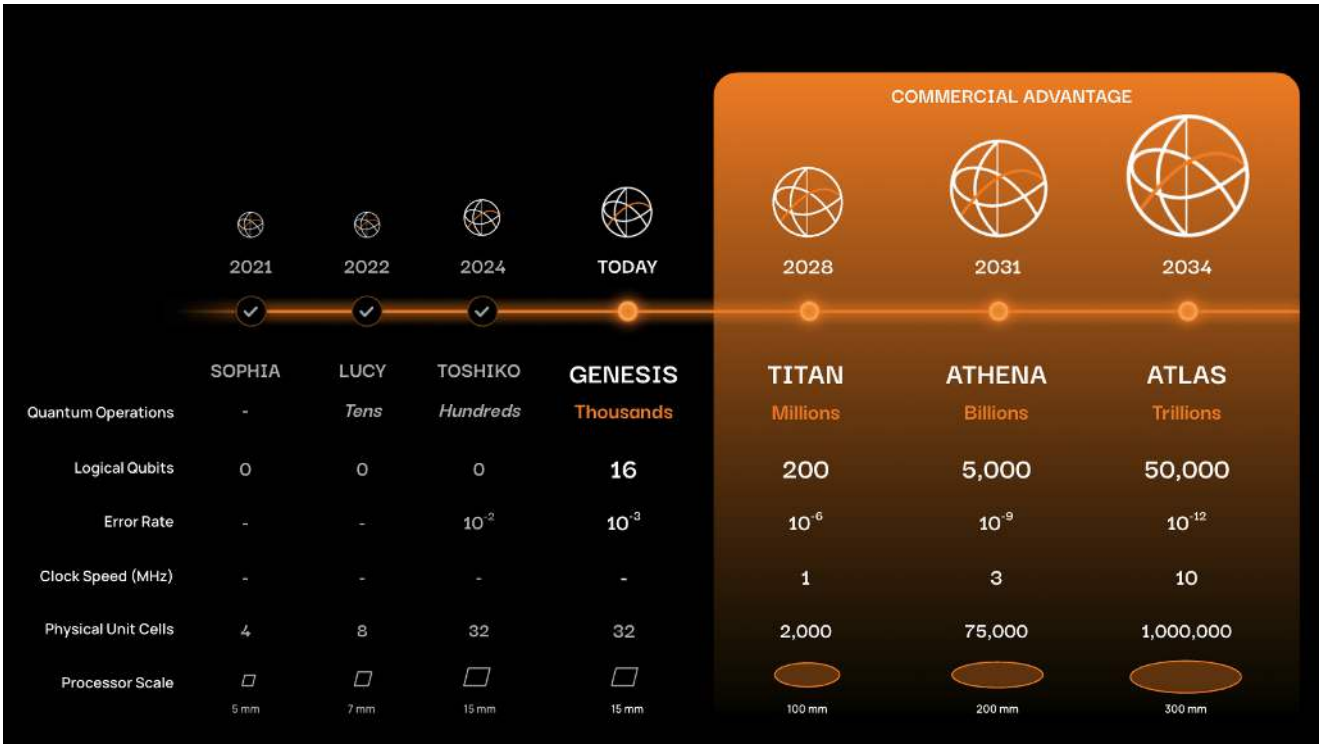

Figure 91: OQC roadmap published in 2025. Their GENESIS 16 encoded qubits correspond to the 4×4 system that they tested in 2025 in [1168]. These are dual-rail encoded qubits with erasure detection, not demonstrated fault-tolerant logical qubits. As of early 2026, OQC had tested a 76 mm (3 inch) wafer with about 100 physical qubits [1172] but not the 152 mm (6 inch) wafer as planned. Their next key milestone is TITAN in 2028, with 200 logical qubits using 2,000 physical coaxmon/dimon sites on a 100 mm wafer, supporting a megaquop. Their plan to support 50K logical qubits and a teraquop on a single 300 mm wafer in 2034 in their ATLAS system is quite ambitious to say the least. Source: OQC roadmap, June 2025. Source: [9].

Figure 92: Anyon Systems superconducting chip as of 2023.

Figure 93: Anyon Systems superconducting setup for its 12 qubit Monarq QPU that was delivered to Calcul Québec. Source: [1177].

You can't easily beat Bluefors and the like in your own garage.

As of mid-2026, their plan was to deploy soon a 72-qubit system and then another, which would scale beyond 100 physical qubits.

QpiAI

India, 2019, $38.5M

QpiAI is developing a family of superconducting qubit quantum computers on top of their efforts with silicon spin computing. They announced in 2025 the creation of a 25-qubit superconducting QPU, the Gen-1. Their roadmap contains 64 qubits (Kaveri, 2025, 99% error

rate), 128 qubits (Ganges, 2026, which moved to 2027 in 2026, with a physical error rate of 10^{-3}) and 1,000 qubits (Everest, 2027, moved to 2028 in 2026, also with 10^{-3} error rates). They planned to support at least 100 logical qubits by 2030 with the Unnati system, including qLDPC and a megaquop support.

The Gen-1 is built with a Bluefors XLD cryostat (Figure 94). Their two-qubit gate fidelities are at about 96% which is way below any QEC code threshold. They plan to support non-local quantum error correction codes, but we can have doubts on their ability to design the related chips given the sheer effort that is done there at IBM, Google and others. Their first chips were provided by QuantWare. In March 2026, they prototyped some QEC real-time decoder running with their supposedly home made 64-qubit Kaveri chip, which is "wafer-scale", and uses a flip-chip architecture with low-loss interconnects for the separation of qubits and interconnect layers.

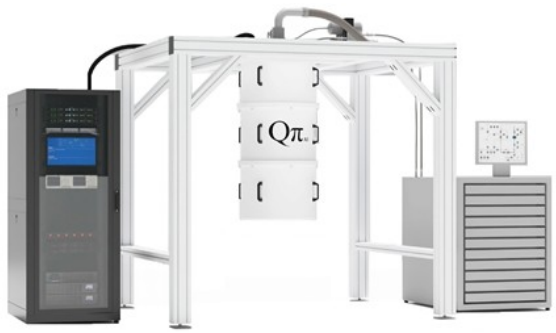

Figure 94: QPi Gen-1 25-qubit QPU built with a Bluefors XLD.

As of mid-2026, the company had not yet published any scientific paper on its chips, particularly on characterization and randomized benchmarking.

QuantWare

The Netherlands, 2021, €215M

QuantWare is a designer and manufacturer of transmon superconducting qubits processors created by Matthijs Rijlaarsdam and Alessandro Bruno [1178].

Company. In September 2022, the company got a subsidy funding of €1.1M from Quantum Delta NL, the foundation running the Dutch quantum national plan, to develop superconducting qubits based on undefined novel materials. Among their scientific advisors are Charlie Marcus, formerly running the Microsoft Quantum Lab in Copenhagen, Denmark. He left Microsoft in November 2021. In May 2026, they got a record funding of $178M. Among their investors are Intel as well as InQTel, CIA's venture fund.

Technology. The chips have airbridges and a proprietary TSV configuration (through-silicon via). They propose custom processors and a product design-to-delivery cycle of 30 days, leveraging the Van Leeuwenhoek Lab cleanroom at TU Delft. They offer a customizable connectivity with vertical interconnect that can help prototype specific quantum error corrections codes.

Their first 5-qubit Soprano QPU had a modest T_1 of 10 μs and a single-qubit gate fidelity of 99.99%. Contralto's 25-qubit processor (shown in Figure 95) could reach a T_1 of 60 μs. As of 2024, their new Soprano-D (5 qubits) and Contralto-D (25 qubits) had single qubit gate fidelities of 99.9%, 99.7% two-qubit gate fidelities, and readout fidelities of 97.5% using their Crescendo-S J-TWPA [1179]. They plan to double the number of qubits in their QPUs every year. In 2023, they announced a 64-qubit version, Tenor-64 which was launched in 2024 [1180] and the Tenor-D which is customizable. In February 2025, QuantWare launched Contralto-A, a 17-qubit chip with flux-tunable qubits created for the development and testing of quantum error-correction codes. It supports distance-3 surface codes.

Who could use these QPUs? Seemingly, various research labs [1181] and enabling technologies vendors, like their colleagues from Qblox and Delft Circuits and also SEEQC which used it to build a full-fledged 5-qubit QPU in 2023 in Italy using some of their SFQ superconducting control electronics. QuantWare also partners with QuantrolOx (UK) and QphoX (The Netherlands).

At the APS March meeting 2024 in Minneapolis, they demonstrated on the show floor a full-stack QPU built in two days with Qblox and Maybell [1182].

In May 2024, QuantWare along with Qblox, and QuantrolOx, announced the development of a new superconducting qubit technology nicknamed ferrotransmons, which reduces hardware requirements at the cabling level. In January 2025, the three companies implemented a fully automated QPU characterization and 2-qubit CZ gate characterization and tuning in under 25 mn.

In May 2025, QuantWare announced a partnership with Q-CTRL on the integration of Q-CTRL's autonomous calibration Boulder Opal software in its QPUs. This was developed at the University of Napoli and the Niels Bohr Institute.

In June 2024, QuantWare announced the inauguration of the Israeli Quantum Computing Centre (IQCC) superconducting QPU in Tel Aviv University powered by a QuantWare Contralto chip, installed in collaboration with Quantum Machines (Israel) and ParTec AG (Germany).

In September 2024, the company launched its 3D VIO technology to foundry services, to enable the creation of large scale QPUs. The VIO-176 supports up to 176 signal lines, enabling the support of up to 100 qubits.

In December 2O25, QuantWare announced VIO-40K, a future quantum processor supporting 10K physical qubits (and therefore, 4 control and readout lines per physical qubits in average), to be delivered in 2028. It will use a stacked chip architecture (VIO 3D), the system being connected to qubit control systems by multiple high-density flexible cables, to be connected to

the NVIDIA NVQLink low-latency control architecture. This chip will be manufactured in the Kilofab, a dedicated superconducting processor fab to open in 2026 in Delft. Intermediate versions are Baritone-D450 with 450 qubits and a VIO-1K chip, in 2027. The Bass-D18K system using VIO-40K will host 18K physical qubits in 2028. We'll check that in time. Late 2025, QuantWare introduced with Qblox and Q-CTRL the Quantum Utility Block (QUB), quantum system with a superconducting qubit chip of 5, 19 or 41 physical qubits, Qblox control electronics and Q-CTRL's autonomous calibration and error-suppression tools. They also partner with Maybell Quantum on scalable cryogenics.

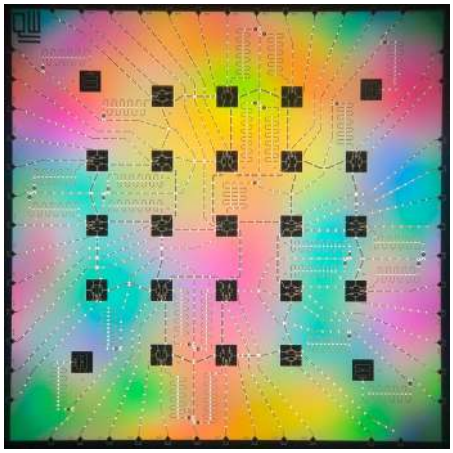

Figure 95: QuantWare's 25 qubit processor. Source: Quantware.

In May 2026, QuantWare presented the design and experiment of a $\cos(2\phi)$ transmon qubit which embeds some protection against relaxation (flip error) [1183].

Atlantic Quantum

USA, 2022-2025, €9M

Company. Atlantic Quantum was a startup cofounded by Jonas Bylander from Chalmers University in Sweden, along with Bharath Kannan (CEO), Simon Gustavsson, Youngkyu Sung, William D. Oliver, Shereen Shermak and Tim Menke, from the MIT [421]. In October 2025, the company was acquired by Google. A first of a kind.

Technology. The startup developed fluxonium superconducting qubits-based quantum computers with experts covering all aspects of the quantum computing stack, from chip design and device fabrication to gate calibration and quantum algorithms (Figure 96). The cofounder's research group develops superconducting quantum electronic devices for quantum computing and simulation. Jonas Bylander published a paper on an efficient qubit readout solution using two microwave pulses and getting rid of the parametric amplifier [1184]. I visited the company's site at Cambridge (USA) in April 2025 and could see their test bed with a Bluefors LD cryostat. They were testing a chip with about 4 qubits. The company was also partnering with Riverlane for the integration of QEC syndrome decoding on their future QPUs [1185].

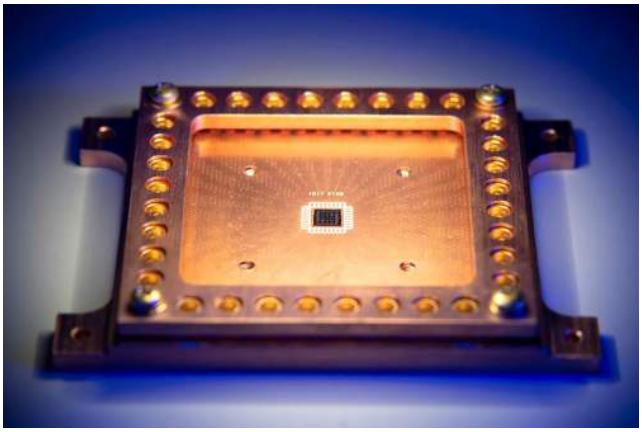

Figure 96: Atlantic Quantum fluxonium superconducting chip. Which is insufficient to have an idea of its qubit fidelities, that is not yet published. Source: Atlantic Quantum.

DoD. In September 2023, Atlantic Quantum was awarded a $1.25M contract by the Air Force Research Lab to develop its prototype fluxonium based quantum processor. It was completed in November 2024 by a new $1.8M grant to pursue the same goal. Atlantic Quantum was also selected in April 2025 by DARPA in the first exploratory phase of the Quantum Benchmark Initiative challenge to build a FTQC system.

Origin Quantum

China, 2017, $163.4M

Origin Quantum *aka* "Yuanyuan Quantum" is a startup created in Hefei by Guang-Can Guo and Guo-Ping Guo out of the CAS quantum lab in Hefei, with Zhang Hui being their CEO. It closed a record $148M Series B funding round in July 2022 for a China quantum startup, making it a unicorn.

Emulation. Initially, it worked mainly on developing quantum algorithms and a quantum emulator. They were behind one of the records for 64-qubit quantum algorithm emulation on a supercomputer [1186]. They also created cloud-based emulation appliances supporting 32 and 64 qubits. In 2025, they published a paper on SparQSim an emulator written in C++ implementing the rarely seen Feynman method which compressed the vector state with storing only the non zero values. It is supposed to be more efficient than state vector based emulators, implementing the Schrödinger model [1187].

Technology. The company started to create its own quantum chips, including superconducting qubits chips with 6 qubits (KF C6-130) and 100 qubits (XW B2-100), using tunable couplers. They expected to reach 1,024 qubits by 2025 with intermediate steps of 64 qubits in 2021 and 144 qubits in 2022 (not achieved yet as of mid-2026). In January 2024, their 72-qubit Wukong QPU using 126 tunable couplers was made available on the cloud. In May 2024, they published some figures

of merit for this QPU, which are substantially below the comparison set of Table 2 at the same date, and for which no independent reproduction or uncertainty data were identified: a T_1 of 14.51 μs, T_2 of 1.84 μs, single-qubit gate 99.65% and CZ gate 96.86% fidelities [1188, 1189]. Along with Guo-Ping Guo's Hefei lab, they have however demonstrated good GHZ (3 entangled qubits) and W states with fidelities of 96.77% and 95.72% [1190]. In May 2026, they launched the 180-qubit Wukong system. The company web site exhibits fidelities of 99.9% for all operations (single qubit gates, two-qubit gates, readout). These are not published in a scientific paper nor credible as it may correspond to peak and not median fidelities (Figure 97). However, in 2026, they improved experimentally their CZ gate fidelity to 99.88% while maintaining short duration to below 60 ns [1191]. Origin Quantum is also working on QEC and FTQC. In 2026, they proposed their "routing codes", a variant of qLDPC codes which reduce the need for long range connectivity [1192].

Parameter	Value
Computational Qubits	180
Coupling Qubits	251
Average T1 Coherence Time	40 μs
Average T2 Echo Coherence Time	20 μs
Average Single-Qubit Gate Fidelity	99.90%
Average Two-Qubit Gate Fidelity	99.90%
Average Readout Fidelity	99.90%

Figure 97: Origin Quantum's Wukong 180-qubit processor was released in May 2026. Its figures of merit are not credible at all. Source: Origin Quantum website as of July 2026.

Enabling technologies. Origin Quantum is developing its own room temperature control electronics with HiMA [1193], its own cryogenic equipment, and NDPT-100, a non-destructive probe electrical measurement platform in December 2022, and the MLLAS-100 laser annealer that is useful for improving quantum chips quality in January 2023 [1194].

Software. The company software include an operating system (Origin Pilot), a programming framework (QPanda), the EmuWare virtual machine, a quantum machine learning framework (VQNet), a quantum programming language (QRunes), an integrated development environment (Qurator), the development of quantum error correction codes [1195], some applications frameworks for quantum chemistry (ChemiQ), fluid dynamics (OriginQ QCFD) and for the financial sector, for portfolio optimization [1196] and with Ping An Insurance for the detection of financial fraud, and in quantum machine learning [1197].

Customers. The company is growing fast thanks to selling their QPUs to China's universities investing in quantum computing education. Interestingly, a bit like IBM, they are also doing research in silicon quantum dot qubits [1198].

SpinQ

China, $97M

SpinQ is known for its NMR educational computers. It is working on a "Shoawei" 20-qubit superconducting qubits with an EDA software named Tianyi [1199] and delivered 2 qubits in 2023 to some unnamed Middle East customer [1200]. The Ursa Major family now supports from 2 to 20 qubits. The company produces its chips in its own cleanroom in the Shenzhen-Hong Kong Innovation and Technology Cooperation Zone [1201].

Alibaba

China, 2019-2023

Alibaba is using the resources of its datacenters to emulate quantum algorithms exceeding 50 qubits. China's leading e-commerce company was partnering with the University of Science and Technology of China (USTC) of the Chinese Academy of Sciences (CAS) to create superconducting qubit QPUs.

Their quantum research effort was embedded in its DAMO Academy, established in 2017. They started with providing cloud access to 11 qubits as of early 2018, on a technology platform developed with USTC. They announced in 2018 that they were creating a subsidiary, **Ping-Tou-Ge**, which develops NPUs (neuromorphic processors for AI) and, eventually, superconducting quantum chips [1202]. They worked on fluxonium superconducting qubits, announcing qubit lifetimes T_1 and T_2 over 100 μs and a 99.5% iSWAP gate fidelity. In August 2023, they implemented a CZ two-qubit gate with a similar fidelity, of 99.53% and fast gate time of 20 ns [1203]. In November 2023, Alibaba dismantled its whole quantum lab. It laid off its 30 employees and donated its equipment to Zhejiang University in Hangzhou, near Shanghai. The former Alibaba quantum created the TraverseQuantum company which design FTQC/QEC architecture.

Baidu

China, ≈2020-2024

Baidu announced in August 2022 its Qian Shi QPU with 10 superconducting qubits, to be later expanded to 36 qubits using couplers to run two-qubit gates, reusing a concept first pioneered by Google in 2019.

These qubits numbers where: $T_1 = 31$ μs, $T_2 = 8.7$ μs, single qubit gate at 99.8% and two-qubit gates at 96.4% (CX) and 96.8% (CZ). It was less than stellar. In January 2024, Baidu announced it was killing its quantum

computing investments and donating its equipment to BAQIS in Beijing.

NEC

Japan, -2026

NEC partnered with RIKEN to build a superconducting qubit CPU to be delivered by 2025 to Osaka University. No detailed specifications are available here. The company decided to stop its quantum computing efforts in September 2026.

Fujitsu

Japan

In April 2021, **RIKEN** and **Fujitsu** created the 20 researchers RIKEN RQC-Fujitsu Collaboration Center in Wako City, Japan, to do joint research and create a transmon based superconducting qubit computer, with a goal of reaching 1,000 physical qubits by 2026 and to develop an associated software platform (not yet achieved as of mid-2026).

It leverages RIKEN's existing work on superconducting qubits from Yasunobu Nakamura's team and Fujitsu's computing know-how. The research plan is quite classical: improving qubit manufacturing, reducing the size and noise of driving electronics components, and wiring and improving error correcting codes. Some roadmaps were uncovered in August 2022. The company also works on microwave quantum interconnect between QPUs [1204].

Fujitsu planned to release a first 64 qubits QPU by spring 2023 and delivered it in October 2023, although with no public qubit fidelities [536, 1206, 1207], combining it with Fujitsu's classical 40-qubit emulator and NTT qubit control software.

Fujitsu delivered #Qmio, a 32 qubits QPU to CESGA in Spain the same month. In April 2025, they announced the integration of a 256-qubit QPU made of an assembly of four 64-qubit chips and integrated electronics. They didn't provide any data on the system because characterization wasn't done yet. Still, they explained that the system optimized the heat dissipation within the cryostat and the chip was manufactured to reduce variability. Keysight is also providing the control electronics of the QPU. As of late 2025, they were working on the next QPU with 1,000 physical qubits and the ability to test error correction codes of distance 11 [1205].

In 2025/2026, the company published a roadmap (Figure 100). They plan to support 10K physical qubits and 200+ logical qubits by 2039 using the STAR architecture, or "partial fault tolerant" with the support of QEC/FTQC for Clifford group gates but not for magic states (we described it in the QEC section of this book in quantum computing engineering). In parallel, they are investing in classical HPC. Fujitsu is the manufacturer of the Fugaku HPC that is run by RIKEN.

Toshiba

Japan

Toshiba (Japan) has been conducting fundamental research in quantum computing since at least 2008, in quantum photonics and with superconducting qubits in its Frontier Research Laboratory.

Here, Hayato Goto is a prolific scientist working in many disciplines. In 2022, he created a double-transmon coupler that turns on/off coupling between two superconducting qubits in an efficient manner, enabling fast computing and two-qubit gate fidelities of 99.99% and time of 24 ns [1209, 1210]. Now, this is not yet commercial-grade fidelities, and it must scale to a decent number of physical qubits.

Now, on to cat-qubit and other bosonic qubits vendors...

Alice & Bob

France, 2020, €130M

Alice & Bob develops cat-qubits FTQC systems, their technology's main benefit being its capability to implement a complete universal FTQC with a much lower ratio of physical per logical qubits than traditional transmon based superconducting qubits.

Company. The startup was cofounded by Théau Peronnin (ENS Lyon) and Raphaël Lescanne (ENS Paris). The startup which is based in Paris, France, also has an office in Boston, USA. Nvidia became an investor in the company in 2026. As of mid-2026, the company had more than 250 employees.

Technology. Alice & Bob's technology is based on the PhD thesis of the startup's founders and the associated work of **Mazyar Mirrahimi**'s Quantic team at Inria [497]. Raphaël Lescanne was a doctoral student in this team, with **Zaki Leghtas** and **Jérémie Guillaud** also being past or current members [1211]. The work additionally involves contributions from CNRS, ENS Lyon, ENS Paris, and Pierre Rouchon from Mines Paristech. Cat-qubits encode the state of a qubit with superposing opposite quantum states in microwave photon cavities, precisely, in the two-dimensional Hilbert space spanned by two coherent states of microwaves of same amplitude and opposite phase [498, 501]. These cat qubits exhibit an exponentially suppressed **bit-flip rate** as the average photon number increases [499]. The reported 10 s, 22 s and later tens-of-minutes figures refer to bit-flip lifetimes or stability of the encoded cat states, not to the ordinary energy-relaxation time T_1 of a two-level transmon [157, 500, 1212]. Phase-flip errors increase with photon number, which is why an outer code is still required.

The remaining phase-flip error increases linearly as the bit-flip error is suppressed exponentially. It can be corrected with repetition error codes or qLDPC codes having a rather low overhead. Based on numerical simulation, a fault-tolerant cat-qubits computer with a

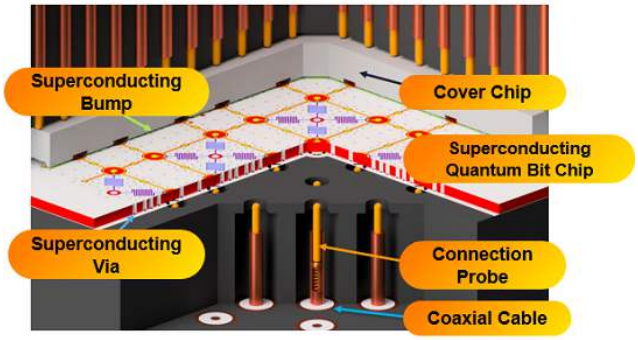

Figure 98: Fujitsu vertical cabling to control its QPU chip. Source: [1205].

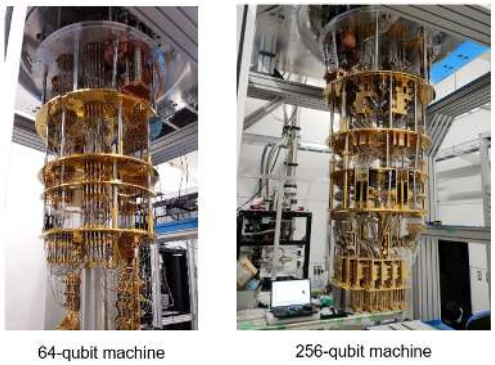

Figure 99: Comparison between the Fujitsuś 64 and 256 qubits QPUs and the related control electronics. It is not tightly integrated at this stage, at least compared with what IBM did in 2022 and 2023 with its experimental Osprey and Condor QPUs. Source: [1205].

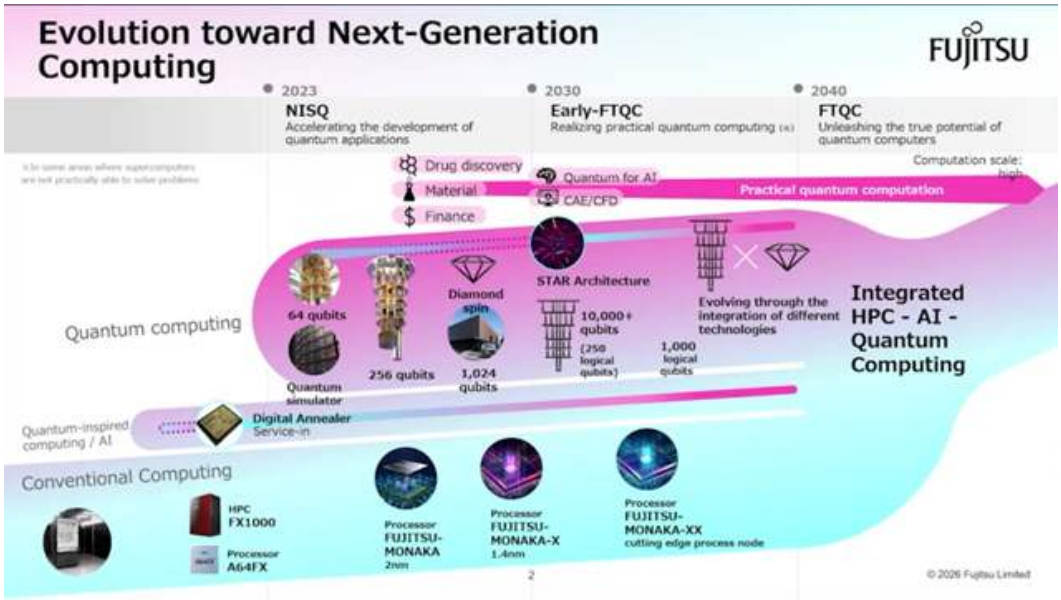

Figure 100: Fujitsu roadmap. Source: Fujitsu in [1208].

logical error probability of 10^{-10} could be realized using 140 physical cat-qubits for Clifford gates and an average number of 15 photons per mode. A Toffoli gate could be implemented with only 180 physical cat-qubits including all required ancilla qubits [502, 503]. In a 2025 paper, they proposed the unfolded distillation, a protocol to create a T gate with between 53 and 175 physical qubits depending on the noise bias [526].

Cat-qubits drive needs some more connections than regular transmon qubits. A continuous pulse tone drives the cat-qubit photons buffer. The qubit autonomous error correction is using an ATS (Asymmetrically Threaded SQUID), a nonlinear element that is flux biased with an AC current in the 4-8 GHz range. In 2024, they published a paper on the way to remove the need for an ATS, but it was not used [1213]. The cat-qubit cavity is just a simple coplanar resonator as shown in Figure 101. All waveguides are made with tantalum. A single qubit gate requires two pulses (cat drive and dissipation phase). A cat-qubit readout uses two pulses on the coupling transmon and a readout pulse. Qubit readout uses 3 inbound pulses and one reflected pulse. And in total, cat-qubits require about 6 control lines but this may decrease in the future thanks to various improvements [505].

Cat-qubits can support a native implementation of 3-qubit Toffoli gates which, combined with X and Z gates [1214] and preparation of $|+\rangle$, can complete a universal gate set. But finally, Alice & Bob decided to go towards the T-factory route.

In 2026, Alice & Bob researchers introduced the Elevator codes, a resource-efficient QEC architecture designed for biased-noise qubits like cat qubits. It concatenates two classical codes to minimize physical qubit overhead. The first layer utilizes simple high threshold 1D repetition codes to continuously correct phase-flip errors. The

residual bit-flip errors are handled with a high-rate outer code that is applied at the logical level [1215]. They also designed in 2026 a QND multi-qubit Pauli-Z measurement enabling QEC that can re-place CNOT gates and simulated it digitally. It can reduce the physical overhead of their QEC schemes [1216].

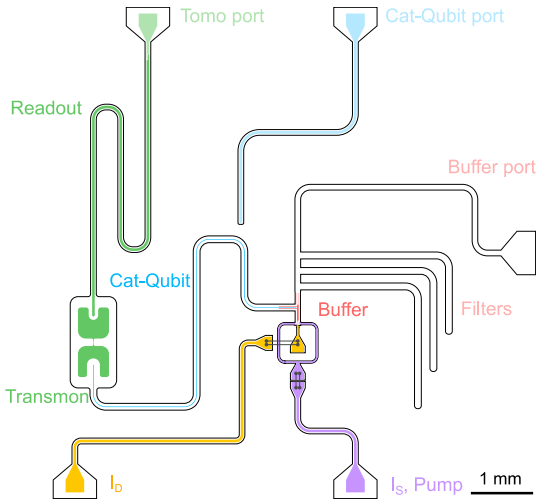

Figure 101: Alice & Bob experimental cat-qubit chip as of mid-2023, with the original logical layout.

In July 2026, they published a complete overview of their FTQC plans and metrics [1217]. The paper introduces bias-preserving CX gates and high-fidelity multi-qubit QND Pauli-Z readouts, enabling high-encoding-rate QEC including their Elevator codes and magic state distillation.

Manufacturing. Alice & Bob chips are currently manufactured at the C2N in Palaiseau and CEA SPEC cleanroom in Saclay, France. They use sapphire wafers. In December 2023, Alice & Bob announced having manufactured its Helium 1 chip with 16 physical cat-qubits, which is milestone on the way to the creation of a logical qubit targeting a raw error rate of 10^{-6} [1220]. In May 2025, the startup announced the creation of a $50M fab line in the Paris region. It will consolidate many production steps that were distributed across the above mentioned sites and help them accelerate the test-and-learn cycle with their chips and improve their quality. As of 2026, the cleanroom was being installed.

Roadmap. Alice & Bob's estimate of about 2,000 physical cat qubits for 100 logical qubits at a 10^{-6} logical-gate error rate is a resource estimate and roadmap target, not a demonstrated 100-logical-qubit processor. The proposed single-chip 8×3.5 cm layout (Figure 103) likewise remains an architectural projection. Their 2025 magic-state work provided resource estimates for a logical magic-state primitive, which is an important FTQC component.

Services. Sideways, Alice&Bob launched in July 2023 "The Box" a consulting unit, to help customers with building applications (in the future). They also opened a branch in Boston in October 2023.

Software. In November 2024, Alice & Bob released Dynamiqs, its open-source Python quantum simulation library exploiting Nvidia GPUs, for fast simulations of large, complex quantum systems such as QPUs and their components like resonators. It simulates the physics of qubits themselves [1221].

Applications. Alice & Bob is working with the Los Alamos National Laboratory and a General Electric spinoff, GE Vernova, on the design of more efficient magnets to be used in electric motors, turbines and future energy and industrial technologies. This collaboration was funded by DoE's ARPA-E with $3.9M.

Partners. Alice & Bob announced a partnership with Equinix in November 2023 to serve large account customers using Equinix hosting facilities. It also announced a partnership with Nvidia in March 2024, in line with their existing partnership with Quantum Machines which itself announced a partnership with Nvidia in September 2023. Alice & Bob is to use Nvidia DGX Quantum, a server appliance combining GH200 Grace Hopper chips and Quantum Machines' OPX+ qubit drive control system. DGX Quantum also runs the classical part of hybrid algorithms, quantum error correction codes, qubit calibration, and qubit control drive [1222]. Their Boson-4 qubit chip has been available online for a while on Google's cloud starting in June 2024. Alice & Bob also partners with Horizon Quantum (Singapore) to support their emulator with Horizon Quantum's Triple Alpha platform that handles compilation, resource analysis, and error-correction for FTQC application development. At last, Alice & Bob will rely on Nvidia GPUs for handling QEC error syndrome detection, as announced in March 2026.

DARPA QBI. In April 2024, Alice & Bob was selected by DARPA for the first phase of its Quantum Benchmark Initiative challenge for the development of a FTQC QPU. It was selected among a total of 16 vendors. It was the only vendor from the European Union who participated to the challenge until being selected. They were however not selected in phase two in April 2025.

Customers. Alice & Bob presold Helium, a 18 physical qubit system to GENCI / TGCC as announced in May 2026 to be installed in 2027. Meanwhile, their test system is available for researchers collaborating with the company. The acquisition was funded by the France HQI program launched in 2022.

Amazon

USA, 2020

Amazon started first to announce late 2019 its Amazon Braket cloud offering, based on using third-party quantum computers from D-Wave, Rigetti and IonQ, covered in the cloud section of this book.

Blueprint. In December 2020, the company published a detailed blueprint to build its own quantum computer, using cat-qubits, in a 118 pages paper [1223]. This work

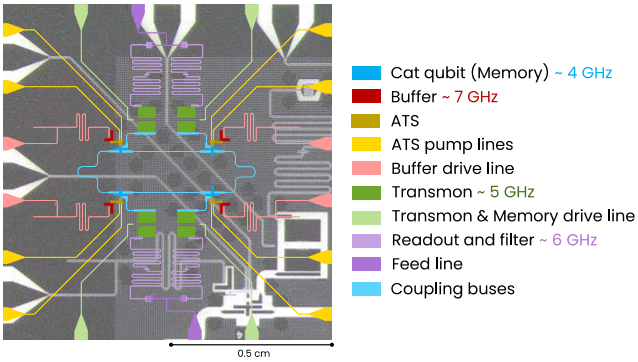

Figure 102: Alice & Bob experimental cat-qubit chip as of mid-2023, with its current physical layout. Sources: [498] and Antoine Gras in [1218].

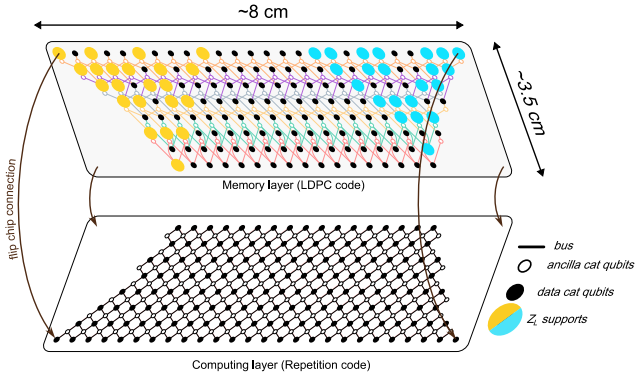

Figure 103: A single Alice&Bob chip with about 2,000 physical cat-qubits could support 100 logical qubits. Source: [1219].

got the help from Caltech, including John Preskill, in connection with Yale University where some Caltech students did their PhDs in the teams of Rob Schoelkopf and Michel Devoret. The Amazon effort was then led by Simone Severini (Director of Quantum Computing at AWS [1224], who left the company to join Google in June 2025), Oskar Painter (Head of Quantum Hardware at AWS), Fernando G.S.L. Brandão (Head of Quantum Algorithms at AWS and also researcher at Caltech) and Richard Moulds (GM Amazon Braket).

Cat-qubits. Amazon initially proposed an architecture largely inspired by what the French teams at Inria have investigated since 2013 with Mazyar Mirrahimi et al., including the founders of Alice & Bob. They wanted to create a FTQC QPU. On top of France's founding work on cat-qubits, Amazon is also relying on many US Universities research like Caltech, Stanford, Chicago University and Yale University.

In 2020, Amazon planned to use an electro-acoustic resonator to host the cat qubits while the circuit element, the Asymmetrically Threaded SQUID (ATS) invented by Raphaël Lescanne and Zaki Leghtas, used by Alice & Bob to stabilize the cat-qubit is superconducting. While Alice & Bob QEC is based on dissipating excess qubit energy to maintain it in low-energy states with encoding it in a linear oscillator driven by 10 GHz microwaves, Amazon chose a variant that uses linear harmonic oscillators-based cat-qubits using very compact piezoelectric nanostructures and phonons. Like with Alice & Bob, these cat-qubits self-corrects flip errors at the hardware level while phase errors are being handled by some QEC requiring, supposedly about 20 physical qubits.

Cat-qubits encode information with microwaves put in coherent states with opposite phases, $|+\rangle$ and $|-\rangle$. The qubit computational basis states are defined as even and odds coherent states cats, meaning using positive and negative sign superpositions for these two cat-states. Like Alice & Bob, they will implement a universal gate set comprising X, Z, CNOT and Toffoli gates. They use two new ideas for implementing fault-tolerant Toffoli gates: an extremely small chip layout ("bottom-up Toffoli") and a technique to lower the bit-flip error rate ("top-down Toffoli"). They also avoid crosstalk between cat-qubits using four cat-qubits connected to a single dissipating reservoir. This compact layout is compatible with a scalable architecture but may generate significant crosstalk errors, which could be mitigated with a well-chosen filter design cutting the frequencies to remove crosstalk errors.

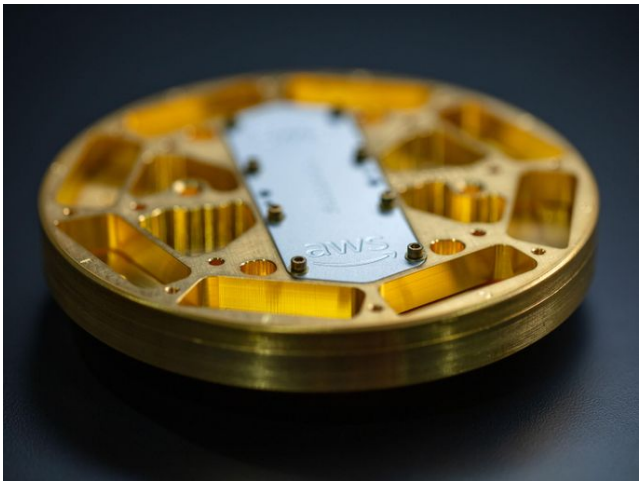

Figure 104: The first prototype Amazon cat-qubit chip was shown as early as 2021 but its details were disclosed only in 2024.

They first planned to implement a 9-qubit QEC to obtain a logical error rate of 2.7×10^{-8}. As a result, they expect to use 2,000 superconducting qubits to create a 100 logical qubits system supporting 10^6 operations, exactly like Alice & Bob. If this works, it will generate a significant difference with IBM and Google who plan to obtain the same number of logical qubits with way more physical qubits, about 150K for Google when using data published in 2024 about Willow, and even considering the non-local gross codes and better qubit connectivity for IBM. The scalability constraints are much different in

both cases, whether it deals with cryogenics, microwave generations and readouts, or cabling.

AWS is also working on some interconnect technologies involving piezoelectric based conversion of qubit state from the microwave to the optical domain, to enable long range interconnect between QPUs [1225].

Error correction. In April 2021, University of Sydney science undergraduate Pablo Bonilla Ataides published in Nature Communications a paper on its ZXXZ surface code that would reduce the number of required physical qubits to create a logical qubit thanks to a lower error threshold. It brought the attention of Amazon researchers [1226]. This surface code could be used by Amazon who made a choice to use a relatively low number of photons per cat qubit (8 to 10, compared to about 15 for Alice & Bob, but the optimum number of photons is still to be determined experimentally), with intrinsic cat stabilization suppressing bit flips while the outer code detects and corrects the dominant residual phase flips. That is where an XZZX surface code could come into play. XZZX QEC codes are indeed mentioned as an option QEC technique in Amazon's technical paper from December 2020. Finally, in their Ocelot 5 cat-qubit chip, they used a different and simpler code, a repetition code that corrects only phase flip errors, using 4 ancilla transmon qubits (Figure 106).

Dual-rail, GKP qubits and 0-n Fock qubits. AWS is not just investigating cat-qubits. Its research team also works on GKP bosonic qubits [515, 1227], with dual-rail qubits [521, 1228], regular transmons [1229] and with a 0-n Fock state qubit proposal published in August 2026 [1230]. They are hedging their bets considering that they find that cat-qubits are difficult to engineer. The AWS research team is also exploring other qubit avenues including photon qubits.

Figure 105: Amazon's quantum lab in Caltech opened in October 2021. Source: AWS.

Research Center. The bulk of Amazon's quantum team is based in the new 21,000-square-foot AWS Center for Quantum Computing building next to Caltech in Pasadena, North of Los Angeles. It was inaugurated in October 2021 [1231]. They even then showcased a picture of a prototype quantum processor, maybe the one with 9 qubits (Figure 105).

First QEC experiments. AWS's Ocelot result uses five cat-qubit data modes and four transmon ancillas in a repetition-code experiment [506, 524]. The distance-5 result reports a logical error per cycle of about 1.65%. It is a meaningful demonstration of hardware-efficient concatenated bosonic QEC, but it is not yet a general fault-tolerant logical qubit: the repetition code primarily addresses the dominant phase-error channel and does not by itself implement a universal fault-tolerant gate set. Comparing its logical error per QEC cycle directly with an isolated transmon gate error is also not an apples-to-apples metric.

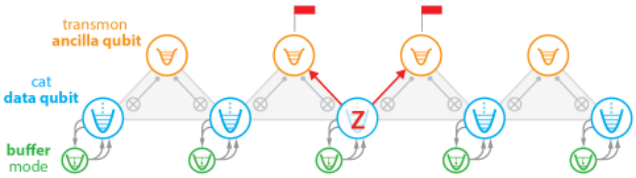

Figure 106: The first publicized cat-qubit chip from AWS. Ocelot uses five bosonic cat-qubit data modes and four transmon ancillas forming a single distance-5 repetition code. Intrinsic cat stabilization suppresses bit flips, while repeated syndrome measurements correct residual phase flips. Source: [506].

This work was extended in October 2024 with an architecture enabling the correction of residual flip errors using a 2D QEC code also using ancilla transmon qubits [1232]. In August 2026, they implemented a bias-preserving cat-cat CNOT gate. The result supports a projected distance-7 repetition-code architecture built from 13 cat qubits [527].

Nord Quantique

Canada, 2019, $55.5M

Company. Nord Quantique was created out of the Institut Quantique from Sherbrooke University by Julien Camirand Lemyre and Philippe St-Jean with the scientific support from Alexandre Blais. Their main investors are BDC Capital (USA), Quantonation (France) and Real Ventures (Canada). The company had a team of over 65 as of mid-2026.

Technology. Nord Quantique is developing a superconducting quantum computer using qubits with autonomous error correction and GKP codes, a variant of bosonic codes, and 3D cavities created at Yale. They have tested one qubit so far (Figure 107). Their chips were manufactured in Sherbrooke University's nanofab and will be manufactured in Bromont at the MiQro Innovation Collaborative Centre (C2MI) with some components also manufactured by RIKEN Center for Quantum Computing, and cryo-CMOS at the 300 nm NanoFab from NY CREATES in Albany, New York state.

In 2024, Nord Quantique demonstrated autonomous QEC of a single-mode GKP-encoded qubit and reported a roughly 14% lifetime improvement to about 208 μs [509, 1233]. It is legitimate to call the oscillator degree

of freedom a bosonically encoded logical qubit. The important caveat is that this is not yet a complete fault-tolerant logical qubit with arbitrarily suppressible logical error under a universal gate set.

In July 2026, they demonstrated high-fidelity SPAM (state preparation and measurement) for a single-mode GKP qubit, combining postselected stabilization for repeat-until-success (RUS) state preparation, reaching total SPAM error below $7(7)\times10^{-4}$ for cardinal states and $8(5)\times10^{-3}$ for magic states, a two-orders-of-magnitude improvement. Conditional on successful postselection, the reported SPAM error is comparable to selected transmon results, but the 9% overall acceptance probability prevents a direct operational comparison [528].

FTQC. In September 2024, the company published a blueprint for their FTQC architecture laying out a lot of details on their plans [1234]. Their approach combines GKP bosonic qubits with autonomous, reservoir-engineered error correction, which corrects small displacement and loss errors through engineered dissipation rather than through a generic self-correcting memory. The qubit information is encoded in a microwave oscillator in a 3D cavity (Figure 108) which could potentially be turned into a 2D cavity which would be easier to manufacture. The qubit is coupled to an auxiliary nonlinear element used to drive it. Then, a lossy resonator performs qubit readout and resets of the auxiliary. Nord Quantique estimates that its QPU supporting 1,000+ logical qubits would have a reasonable footprint of 20 m2 and low energy footprint. They expect to support 100 logical qubits by 2028 and 1,000 by 2031.

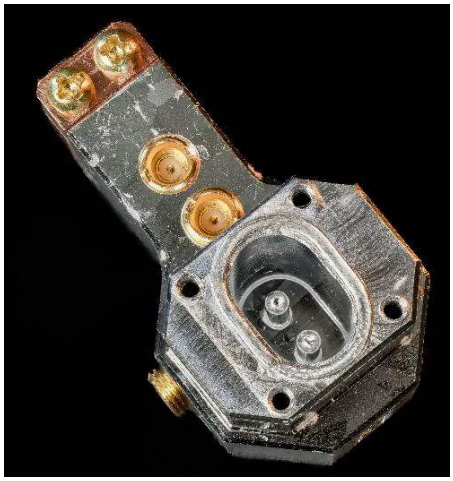

Figure 107: One Nord Quantique qubit. Source: Nord Quantique.

Their GKP oscillator is already an encoded logical qubit at the bosonic-code level, so describing it simply as a physical qubit is also misleading. What remains necessary is additional fault-tolerant error correction and protected logical operations at the architecture level. They plan to concatenate bosonic encoding with additional codes, including binomial and tesseract-code concepts. The blueprint describes the reservoir engineering-based small-**B**ig-small (sBs) protocol and how they implement single (X, Z, H) and a parametrized two-qubit exponential SWAP gate ($e^{i\theta S}$) using the echoed conditional displacement technique (ECD). In July 2025, they described how they would implement magic state preparation for a non-Clifford $\sqrt{H}_L$ gate that could be used to create a logical universal gate set [512].

Partnerships. In June 2024, Nord Quantique announced a partnership with OTI Lumionics to test quantum applications for material sciences, a typical move for most quantum computing hardware startups, but with doubtful meaning given they won't have a functional and useful QPU before a couple years [1235].

Qolab

USA, 2024, $73.7M

Qolab is a startup created by Alan Ho (CEO), John Martinis (CTO), and Robert McDermott (Head of Hardware).

Along with academic and industry partners, they published a blueprint in November 2024 that they updated several times, in January 2025 and March 2026, which describes their plans in a thorough manner [41]. They plan to create very large 20K superconducting qubits chips of 14 cm × 14 cm hooked to another wafer containing the wiring from 15 mK to 3.5K going to cryo-CMOS controls. Qubit readout will use Josephson photomultipliers, removing the need for TWPAs and circulators. They aim to tile 10 of these chips in a single cryostat, therefore supporting 200K physical qubits. The target figures of merit are 3×10^{-4} two-qubit gate errors, 35 ns gate times and 200 μs coherence times.

HPE provides insights on HPC-QPU connectivity and QPU/HPC integration [1236], using circuit knitting. They provide resource estimates for running a QPE on benzene and FeMoCo. The company wants to build a horizontally integrated QPU ecosystem with various specializations. Thus, the participation of Applied Materials (cleanroom and fab), HPE (HPC-QPU integration), Synopsys (EDA), 1Qubit (resource estimation), FZ Jülich (error correction modelling [1237]), etc.

They also explicitly stated that they don't believe that quantum computers could provide some quantum advantage for solving combinatorial decision problems. The consortium is investing, mostly through HPE, in alternative unconventional classical computing paradigms among which photonic coherent Ising models and probabilistic computing [1238–1240]. In that later case, their tests cover Gibbs sampling, a Markov Chain Monte Carlo (MCMC) algorithm used to sample from complex, high-dimensional probability distributions when direct sampling is challenging. Their first tests use FPGA, before manufacturing dedicated CMOS chips and it provides already significant speedups vs existing classical solutions for solving SAT optimization problems.

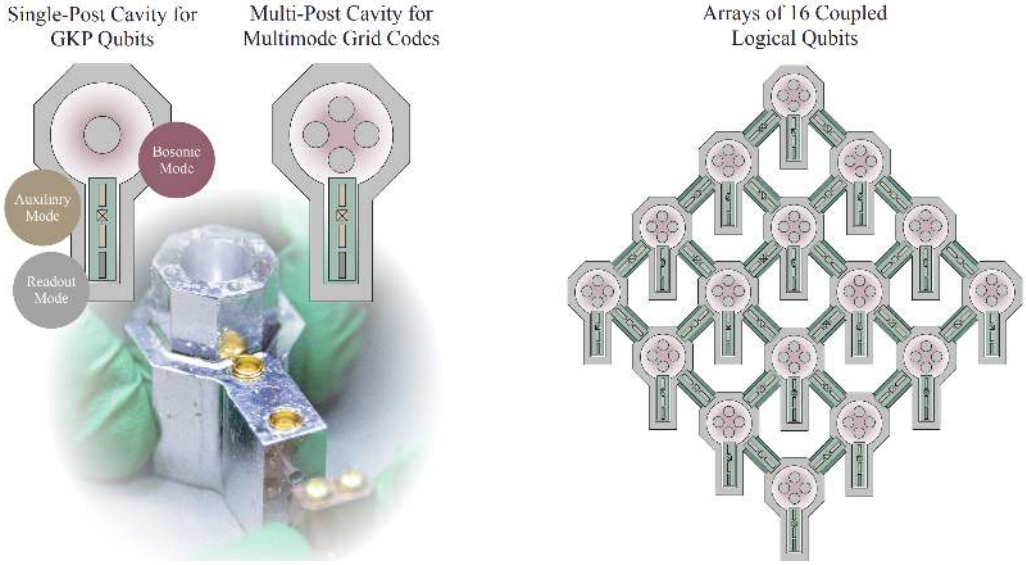

Figure 108: The 3D prototype GKP qubit presented by Nord Quantique in their September 2024 preprint. They still plan to later adopt a 2D structure which would be easier to manufacture. Source: [1234].

In March and May 2025, they published two preprints describing how they would improve their chip manufacturing using a lift off-free qubit fabrication that employs a silicon oxide (SiO_2) scaffold to define an etched window with a well-controlled size to form a Josephson junction. The lift off phase is usually implemented after the evaporation based deposition of materials for the creation of the Josephson junction and is the source of various contaminations of the Josephson junction [642, 1241]. In March 2026, they proposed a blueprint for the implementation of pFT, partial fault-tolerance, along the lines of the Fujitsu STAR model where non-Clifford states are generated in a non FTQC manner [1242]. It could support a megaquop operation with a smaller hardware footprint than full QEC/FTQC architectures. The projected gain is about two orders of magnitude in physical qubit numbers to support a megaquop.

In November 2025, the Quantum Scaling Alliance was launched by Qolab, HPE, and many enabling technology vendors along the same lines than Qolab's blueprint paper (1QBit for FTQC/QEC, compilation, and resource estimations, Applied Materials for engineering and fabrication, Quantum Machines for control electronics, Synopsys for EDAs and the University of Wisconsin for algorithms and benchmarking and with the addition of Riverlane for error correction). It formally ties these players along the plan to create scalable quantum computers. The alliance is led by Masoud Mohseni from HPE Labs and John Martinis from Qolab.

Peak Quantum

Germany, 2024, €5M

Peak Quantum is developing a superconducting qubit quantum chip, using a business model similar to QuantWare. The company based in Garching near Munich was created by Stefan Filipp, who is also a professor at TUM and director of the Quantum Computing and Information Processing team at the Walther-Meißner-Institute for Low Temperature Research (WMI).

Based on work from WMI by Stefan Filipp, it seems that they are working in different directions:

- Fixed-frequency transmons plus a tunable coupler, to implement CZ gates which can reach 99.9% fidelity, but not with such an average or median fidelity, and a duration of 64 ns [1243].
- The fluxonium-transmon hybrid lattice at the theoretical level, using fluxonium's much longer coherence and larger anharmonicity while solving fluxonium's control and loading problems by interleaving transmons, using transmon couplers, and with better scaling prospects [1244]. So far, they tested 5 qubits, but with average 98.8% two-qubit gate fidelities but 5-GHZ states with a very good fidelity of 90% [1245].
- The P-mon two-qubit gate, a multimode superconducting qubit hosting a protected, fixed-frequency computational mode alongside a flux-tunable mediator mode, with a third high-frequency mode engineered to decouple. It has intrinsic protection against decoherence from the readout environment. This yielded a 180 ns CZ gate with 99.62% fidelity [1246].
- Using optimized pulses, building single-qubit gates resilient to drift in qubit frequency, drive amplitude, and coherence [1247].

They also work on the manufacturing of High-Q (one million) superconducting resonators with Infineon on 200 wafers [1248] and using design automation (EDAs) with an analytical model to create scalable and adaptable resonator design [390].

QuamCore

Israel, 2022, $35M

QuamCore is a startup that plans to create a scalable superconducting qubits platform, with using superconducting control electronics. In a sense, they are the first competitor to SEEQC, with the apparent goal of becoming a fully-stack QPU vendor. The company targets one million superconducting qubits in a single cryogenic system. The public information reviewed here is insufficient to identify the cryostat architecture. The company was created by Alan Cohen (CEO), Shay Hacohen-Gourgy (CTO, coming from Technion), Serge Rosenblum (CSO, coming from the Weizmann Institute) and Edy Friedman. It is quite difficult to obtain more information on their architecture based on their past scientific publications [665, 1249]. They may be using some form of autonomous error correction in superconducting qubits using transmon ancilla [1250].

Planckian

Italy, 2023, €2.7M

Planckian spun out of the University of Pisa and Scuola Normale Superiore and is run by Michele Dallari (CEO), Marco Polini (Chief Scientist), and Vittorio Giovannetti (Executive Scientific Advisor) Planckian was the world's first startup willing to create a macroscopic solid state quantum battery also named a Dicke quantum battery "*powered by entanglement*" [1251, 1252].

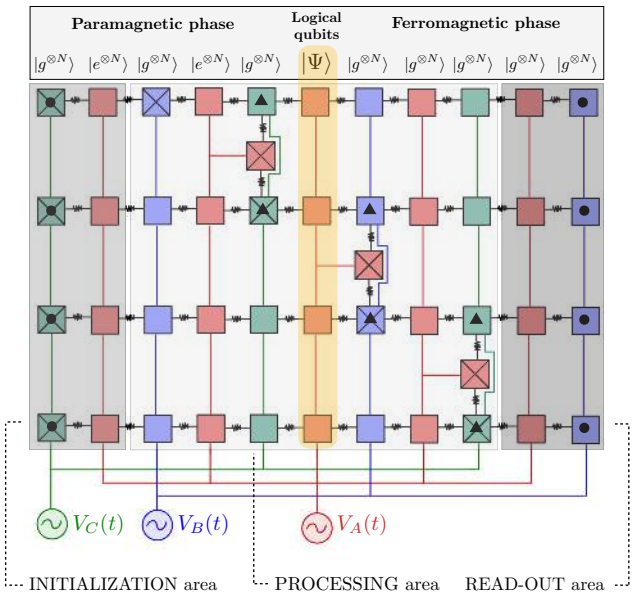

Figure 109: Planckian architecture using only three lines to control a set of qubits in a chip. Source: [1253].

They pivoted in 2024 to create a superconducting qubit technology that simplifies wiring [1254]. They position themselves as being upstream of QuantWare and Peak Quantum who also design superconducting chips. They use global pulses to collectively control a collection of one third of the register qubits, reducing the total number of wires necessary to run the computation [1253, 1255, 1256].

In October 2025, they described how their architecture could resist to fabrication-induced inhomogeneities in qubit resonant frequencies and coupling strengths [1257]. In January 2026, they did show how they could implement ZZ interactions between qubit, with a potential application in analog simulations [1258] and in August 2026, how their global control approach could enable quantum error correction, using what they call "cyclic" stabilizer codes based on global iSWAP and single-qubit gates [1259].

Qarakal Quantum

Israel, 2024

Qarakal Quantum develops QPUs using superconducting qubits using "novel quantum gates and circuits". Among its founders are Sheir Yarkoni (quantum algorithms) and Samuel Goldstein (hardware), who are coming from the Hebrew University of Jerusalem.

In August 2026, they published a preprint presenting Pangaea, an FTQC architecture using a quantum bus that mediates logical operations between remote patches of two-dimensional topological codes [1260]. It reduces the cost of lattice surgery to connect logical qubits with planar error correction codes. The bus also enables the support of heterogeneous codes for implementing magic states distillation with color-codes used as noisy magic resource states, used in generation, cultivation, and post-selection, and inserting a surface-code logical qubit in the protocol through the bus to distill the logical magic state. They didn't describe any hardware architecture, providing hints that their offering will maybe sit at the architecture level rather than at the hardware level, a bit like Iceberg Quantum (Australia) and QC Design (Germany).

Anyon Technologies

Singapore, 2023

Anyon Technologies sells superconducting qubits QPU including quantum processors, cryogenics and quantum control electronics. They integrate it with Nvidia GPUs. They don't provide much more information on what they exactly do and sell let alone any number of qubits or fidelity numbers. They partner with small service companies like SDT Inc (South Korea) and YQuantum (Switzerland).

DelQuanTech

Canada, 2023

DelQuanTech is developing high-temperature superconducting qubits that generate entangled photons [1261]. It's a startup with a TRL 1 technology.

Qolumbus

France, 2025, $3.5M

Qolumbus was created by Michael Stern (CSO) and Frédéric Attia (CEO). It grew out of the QNANO launch project supported by the Systematic Paris-Region cluster and from academic work on superconducting flux qubits and donor spins. The company designs hybrid quantum chips com-bining superconducting qubits with bismuth donor semiconductor spins. It plans to licence its tech-nology to other industry vendors. Stern had a PhD from the Weizmann Institute in semiconductor physics and a postdoc at CEA Saclay in the Quantronics group on superconducting circuits.

Their architecture uses bismuth-209 donors implanted in silicon, whose nuclear spin of 9/2 makes each donor a natural qudit and whose spin coherence reaches very long lifetimes in the order of ∼1,500. These are used as data qubits. The mediator and readout element is a compact superconducting flux qubit of roughly 3×3 μm, operating as a two-level system with its third level pushed to ∼50 GHz, which enables fast single-qubit gates of about 1 ns and strong anharmonicity [1262]. The flux qubit acts as a tunable coupler and a mini-antenna on a shared 1D resonator at ∼3 GHz and ∼5-10 cm long, with frequency multiplexing letting about 8 qubits share a resonator and 20-50 bismuth spins to couple per flux qubit [454, 1263, 1264] . Bismuth atoms are randomly placed on the chip and then addressed individually by frequency. The plan is to implement some all-to-all-connected sub-processors of about 50 qubits, joined into larger 1D bars and multiple bars through dynamic, adiabatic, and longitudinal coupling and SWAP operations between flux and spin qubits [1265]. It would enable non-local connectivity that enables qLDPC QEC [1266].

Quint Computing

Germany, 2026

Quint Computing aims to build a FTQC superconducting qubit quantum computer. The company was created by Christopher Eichler, Michael J. Hartmann and Jona Stinner. Florian Marquardt, Reinhard Ploss and Markus Hoffmann are part of their advisor board.

Based on the academic profile of their cofounders, we can infer that Quint Computing is probably building a superconducting FTQC processor hybrid architecture based on fluxonium data qubits and transmon ancilla qubits (Figure 110), targeting surface code error correction with lower physical qubit overhead than with transmon qubits. They bring expertise in QEC (Christopher Eichler with his work on distance-3 surface code in [1267]), crosstalk-free coupler design (Michael J. Hartmann in [1244, 1268]), AI-native decoding and control (Florian Marquardt), semiconductor manufacturing scaling experience (Reinhard Ploss is a former Infineon CEO), and industrial ecosystem access (Markus Hoffmann has a Google Quantum AI background).

Quantum Circuits Inc

USA, 2015-2026, $118M

Quantum Circuits Inc (QCi) is a spin-off from Yale University co-founded by Rob Schoelkopf, Luigi Frunzio and Michel Devoret. Michel Devoret left the company in 2019, preferring to be a full-time researcher at Yale University. As of April 2025, they had a headcount of 67. In January 2026, the company was acquired by D-Wave for $550M.

Technology. They used dual-rail cavity qubits, based on Rob Schoelkopf's team research at Yale, which convert dominant photon-loss events into detectable erasures. Residual Pauli, leakage, measurement and correlated errors still require additional fault-tolerant protection. They announced in 2019 that their system should be available someday on Microsoft Azure Quantum cloud. Technically, their planned qubits are stabilized by discrete parity measurement using a transmon and a so-called dual-rail model [522, 1270] and their two-qubit gates are implemented using SNAP gates (Selective Number-dependent Arbitrary Phase (SNAP) using the same transmon [1271].

They also planned to use micromachined 3D cavities with a good Q factor [1272, 1273] and to obtain a linear gain in qubit lifetime with the number of physical qubits. It will still require an outer code, such as a surface code, addressing both bit-flip and phase-flip error types in a single error model. In November 2024, they released their 8-qubit Aqumen Seeker QPU. In May 2025, QCI published a paper laying out their overall architecture for the implementation of the first entangling gate for superconducting erasure qubits [1269] (Figure 111).

Software. Quantum Circuits' software work centers on operating and error-managing its dual-rail cavity-qubit hardware. The company also collaborates with Algorithmiq.

D-Wave

Canada, 1999, $1.4B

In their 2021 Clarity roadmap, D-Wave announced the future release of a gate-based QPU that was to be implemented in a separate (fluxonium-based) multi-layer superconducting processor architecture, starting with 60 and then 1,000 qubits to implement error correction. They planned to use surface code QECs and to use some combination of RSFQ and other cryo-electronics to control these qubits. They could be highly differentiated for that respect and only challenged by other superconducting qubit vendors partnering with SEEQC. As of mid-2023, they had tested 1- and 2-qubit fluxonium qubit circuits validated a new scalable readout method for gate model architecture. They reduced by a factor of 4 the noise of these qubits. D-Wave published a white

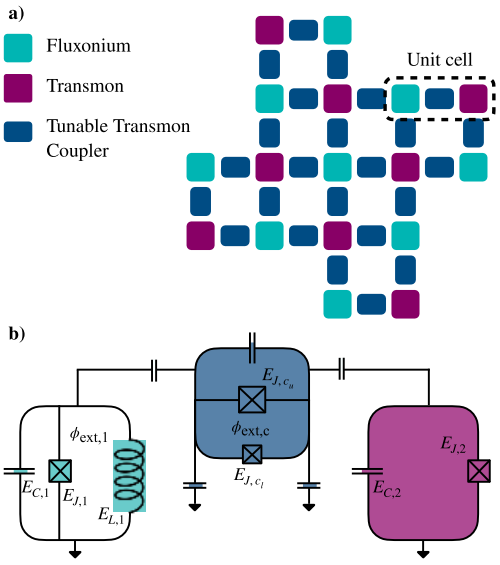

Figure 110: Quint Computing probable hybrid transmon-fluxonium architecture. Source: [1244].

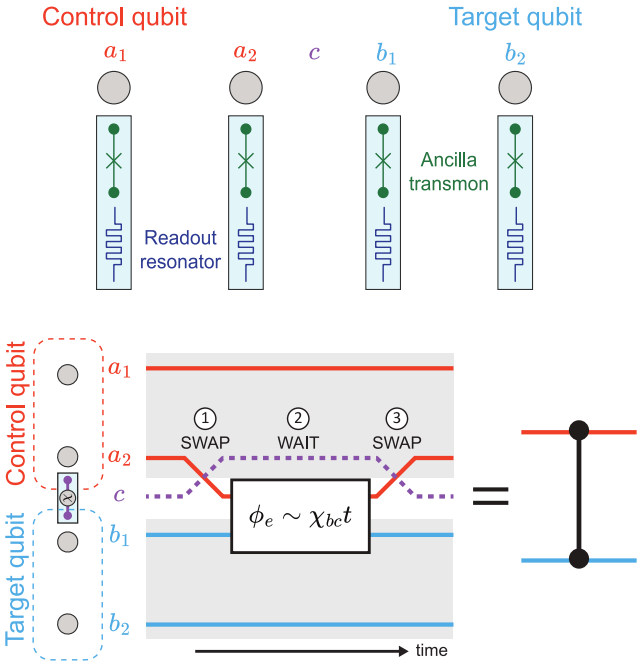

Figure 111: How QCI plans to implement two-qubit CZ gates using two pairs of physical qubits. Source: [1269].

paper on its fluxonium qubit development progress in September 2023, with a T_1 of 120 μs [1274]. They also added a gate model simulator in the Ocean software suite. Since then, their gate-based roadmap seemed to be somewhat stalled.

In January 2026, D-Wave acquired Quantum Circuits Inc. (USA), making dual-rail cavity erasure qubits the most visible element of its gate-model strategy. This is strong evidence of a strategic shift. The gate-model dual-rail roadmap targets 175 physical qubits by 2028, 1,000 by 2030 and 100 logical qubits by 2032, without any precision on the related number of physical qubits or supported circuit size. As a reminder, QCi took 10 years to move from 0 to 8 physical qubits (2015-2025). D-Wave plans to use its own cryo-CMOS control electronics to reduce the cable clutter entering the cryostat. For example, they plan to support 100,000 physical qubits with about 500 control lines [1275].

Through their Quantum Circuits acquisition, D-Wave got a $100M funding by the US Department of Commerce in 2026 as part of NORDTECH's Microelectronics Commons program. The SQFab project is about superconducting technologies materials, packaging, testing and scalable manufacturing. NORDTECH is the Northeast Regional Defense Technology Hub, which is one of eight regional hubs of the U.S. Microelectronics Commons (MEC), a DoD program executed through the Naval Surface Warfare Center Crane Division and managed by NSTXL, the National Security Technology Accelerator. The cleanroom is at the NY CREATES Albany NanoTech Complex. In June, the QCi team for a $4M grant from NSF, as part of the ERASE project, in collaboration with Yale University, where QCi comes from.

In August 2026, the former Quantum Circuits team at D-Wave published in *Nature* an entangling gate for two dual-rail cavity erasure qubits [523]. The experiment reports a roughly 500 ns entangling gate, Bell-state fidelity around 99.60% and a strongly biased error channel in which erasures dominate residual Pauli errors. This is an important two-qubit primitive, but it was demonstrated on a two-encoded-qubit device and by itself does not establish processor-scale QEC performance.

Qbit Force Quantum

India, 2025

Qbit Force Quantum was created by Venkata Subramaniam (CEO, an IBM alumnus) and Ojaswin Singh and is located in the Amaravati Quantum Valley. They sell a modular, made-to-order superconducting qubit quantum computer with its dilution refrigerator. Its use-case is for hardware testing of enabling technologies. They started in 2026 with 3 qubits, with plans to support 30 to 40 qubits. Their cryogenics use a Sumitomo compressor and pulse tube and a home-made dilution. The chips come from Tata Institute of Fundamental Research and the Indian Institute of Science in Bengaluru.

Srsti Quantum Technologies

India, 2025

Srsti Quantum is a superconducting quantum hardware manufacturing startup created by Venkata Sub-

ramaniam (CEO), who is also the CEO of Qbit Force, Subhash Kalidindi (Director of Nanofabrication), Nagalakshmaiah Kalva and Prasanta Kumbhakar (CSO). It is positioned as a component and services supplier, a bit like Quantware and Peak Quantum. They propose superconducting qubit quantum processors and microwave resonators, combining nanofabrication, precision thin-film processing, device characterization, and semiconductor manufacturing, all this with a relatively low TRL and no published scientific paper trail. They seem to be the chip manufacturing arm of Qbit Force.

Logical Qubit Technology

China, 2022, est. $85M

Logical Qubit Technology was created by Zhen Wang (CEO) and Wang Yonghuan (COO). Wang comes from Zhejiang University and worked with Haohua Wang, himself a former student of John Martinis. They were incubated out of the Zhejiang University superconducting quantum computing laboratory. The company scientists participated to various work at Zhejiang University and USTC (Jian Wei-Pan's Hefei team) including the creation of a 10, 18 and 60-qubit GHZ states and 20-qubit cat states [1277–1279].

They have four offerings: the AGate-series frequency-tunable transmon-based superconducting processors, a quantum measurement and control system, an RF signal chain, and, since July 2026, a public quantum cloud. The AGate 30 and AGate 100 chips have a 99.93% median single-qubit gate fidelity and 99.5% median CZ fidelity with a 30 ns gate time, and readout and reset both under 500 ns. Their latest 2026 chip, the AGate-165 chip, also has a median 99.5% two-qubit gate fidelity at 40 ns, which is not best-in-class compared to Google and IBM. They tested distance-9 repetition code and distance-3 surface code circuits. They expect to support tens of thousands of physical qubits with dozens of logical qubits with a logical error rate of 10^{-8} in 2029.

The company team co-authored the demonstration of two low-overhead qLDPC codes, a distance-4 bivariate bicycle code and a distance-3 qLDPC code, on the 32-qubit long-range-coupled Kunlun test processor built at Zhejiang University [1280]. In 2025, the academic team behind the company also demonstrated ZNE QEM applied to repetition and surface code circuits [1281].

SDT Quantum

South Korea, 2023, $7.5M

SDT Quantum is an electronics enabling technology vendor who also created the first South Korean quantum computer, in collaboration with KIST, KISTI (Korea Institute of Science and Technology Information) and Seoul National University. It is a 20-qubit superconducting qubit QPU released in 2026, the KREO SC-20, using a processor from Anyon Technologies (Singapore) and some custom made dilution.

Key superconducting quantum computing reviews

Here is a selection of superconducting qubits scientific reviews to dig into the concepts presented in this section:

A Quantum Engineer's Guide to Superconducting Qubits by Krantz *et al.*, June 2019 (67 pages): the standard engineering entry point covering qubit design, noise sources, control and readout, bridging cQED theory and gate-model practice [584].

Superconducting Qubits: Current State of Play, March 2020 (27 pages): on coherence times, gate fidelities, architectures and error correction prospects [827].

Moving beyond the Transmon: Noise-Protected Superconducting Quantum Circuits, September 2021 (14 pages): on qubits beyond the transmon, with fluxonium, 0-π, multimode and hybrid circuits, and hardware-level noise protection [546].

Advancements in superconducting quantum computing, August 2025 (22 pages): on chip fabrication, gate implementations, entangled state and random circuit sampling records, surface code demonstrations, plus bosonic qubits, fluxonium and qudits [1276].

Enabling Technologies for Scalable Superconducting Quantum Computing, December 2025 (23 pages): what sits around the chip, control electronics, wiring, packaging, cryogenics and the scaling bottlenecks they create [86].

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This **Superconducting qubits** subsection contains 934 bibliographical references and notes containing at least 16,155 pages.

1.4 Quantum dot spin qubits

Electron spin qubits are a promising family of qubit technologies with many variations (Figure 113), with active related research starting later than superconducting-qubit research. Their potential benefits include high miniaturization, comparatively high operating temperatures in some implementations, and compatibility with semiconductor manufacturing. Several variants can leverage processes derived from standard CMOS semiconductor fabrication.

1.4.1 History

The quantum state of a semiconductor spin qubit is generally encoded in the spin of a confined electron or in the effective spin degree of freedom of a confined hole. A hole is not a physical "inverse electron". It is a quasi-particle describing an unoccupied state in an otherwise filled valence band and can carry charge, momentum and an effective angular momentum that can be used as a qubit.

It is usually considered that Daniel Loss with David DiVincenzo and Bruce Kane are the first to have devised ideas to use electron spins to create a quantum computer, a couple of years after Peter Shor created his famous integer factoring eponymous algorithm.

Daniel Loss (University of Basel) and **David DiVincenzo** (then at IBM Research) proposed in 1997 the use of gate-defined quantum dots to encode qubits in confined electron spins [1282]. Their design used electrically controlled exchange coupling between neighboring quantum dots to implement SWAP-type two-qubit operations and also included single-qubit rotations. Later architectures added nearby charge sensors or ancillary dots for spin-to-charge conversion and electrical readout, frequently using radio-frequency reflectometry. These readout circuits are capacitively coupled to the quantum-dot device and are conceptually analogous to dispersive readout chains used with superconducting qubits.

A landmark 2005 experiment demonstrated coherent manipulation of coupled electron spins in a GaAs/AlGaAs double quantum dot, not GaAs on a silicon substrate [1283]. GaAs has an important limitation for spin coherence because the naturally occurring Ga and As isotopes carry nuclear spin, producing a fluctuating hyperfine field. Silicon and germanium offer isotopic-engineering routes to much quieter nuclear-spin environments. In particular, ^{28}Si and ^{72}Ge have zero nuclear spin, although natural Si and Ge contain other isotopes, notably ^{29}Si and ^{73}Ge, that must be reduced when very low hyperfine noise is required. Isotopically enriched heterostructures add manufacturing and materials-supply constraints.

The first demonstration of a silicon spin qubit was made in 2012 by UNSW teams. In 2016, silicon qubits were demonstrated using industry-grade manufacturing processes by a French team from CEA-Leti and IRIG in Grenoble [1284]. This belongs to the Si-MOS category, one of the most CMOS-compatible approaches. Quantum dots can be defined in planar MOS or FD-SOI devices and in FinFET-like geometries inspired by advanced CMOS manufacturing technologies.

The electrostatically active dimensions of these spin-qubit devices are typically of order tens to about 100 nm, which gives them a strong density advantage in principle [49, 115]. This geometric density does not by itself imply that control wiring, readout, calibration and error correction can scale to the same density.

Bruce Kane (UNSW) presented in 1998 another spin-based quantum computer concept based on individual phosphorus donors (^{31}P) in isotopically purified silicon [1285]. This approach is usually labeled "donor spin". The donor provides both a nuclear spin and a bound electron spin, which can be used separately or jointly as quantum degrees of freedom. The qubits are controlled by electrical and magnetic fields [1286] (Figure 112). Nuclear-spin coherence can reach seconds or much longer in optimized isotopically purified silicon devices [1287].

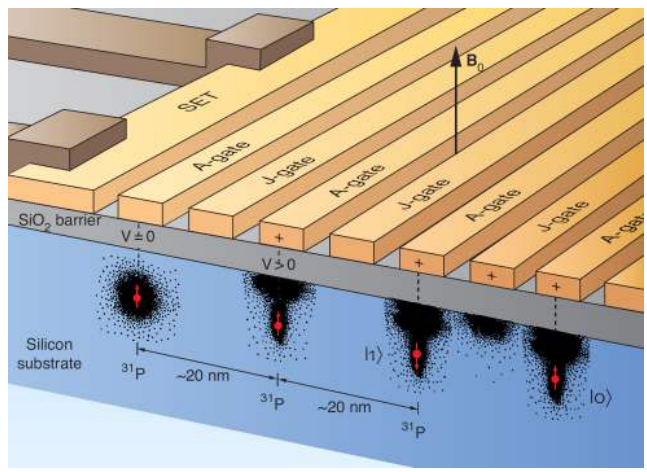

Figure 112: The donor spin architecture with a phosphorus atom implanted in a silicon substrate under a SiO_2 isolation layer. The substitutional phosphorus donor contributes a weakly bound electron whose spin couples hyperfine to the phosphorus-31 nuclear spin, four of its five valence electrons being engaged in covalent bonds with the surrounding silicon atoms. Source: [1288].

The Bruce Kane concept uses a linear array of phosphorus donors buried in an isotopically purified ^{28}Si silicon wafer, operated in a static magnetic field and at cryogenic temperature. The ^{31}P nuclear-spin states provide a computational basis. Metal gates are located above an insulating SiO_2 barrier. A-gates above the donors tune the electron-nuclear hyperfine interaction for single-qubit addressing, while J-gates between donors tune the overlap and exchange interaction of neighboring donor electrons to mediate two-qubit operations. Readout proposals include spin-dependent tunneling to a single-electron transistor (SET). Magnetic-resonance force mi-

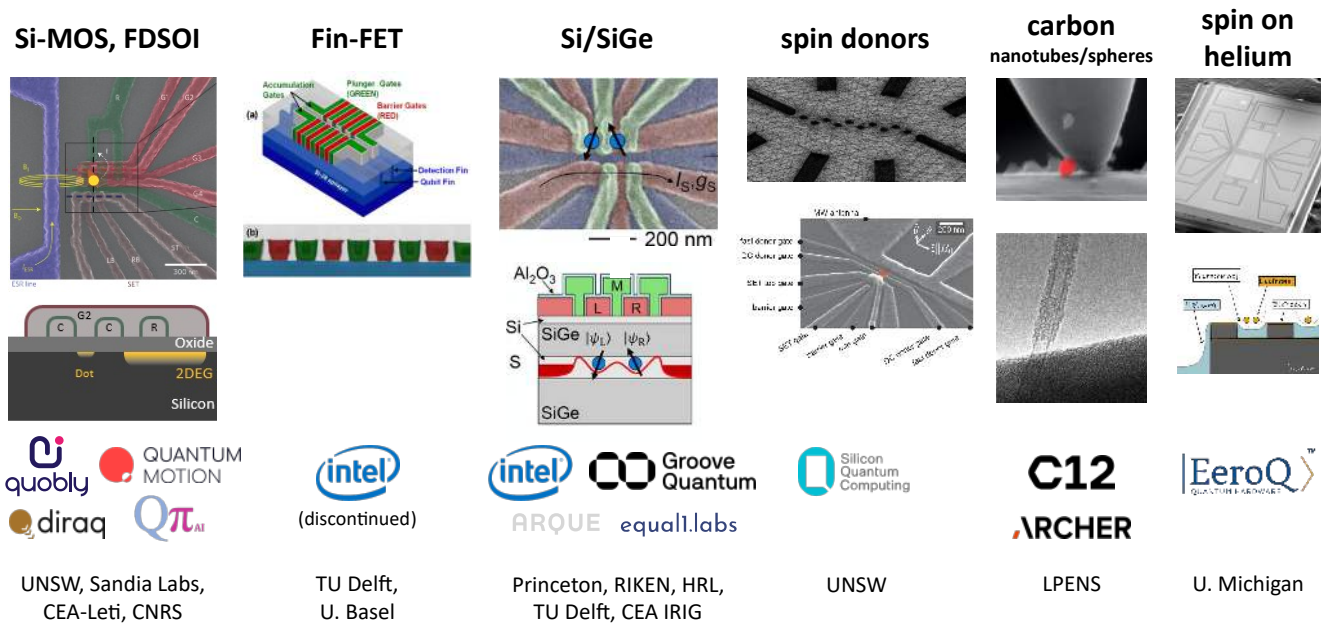

Figure 113: Representative semiconductor spin-qubit and trapped-electron platforms and their vendors, in their order of appearance in the vendors subsection. Si-MOS and Si/SiGe electron-spin platforms can leverage silicon manufacturing. Ge/SiGe hole-spin qubits form a distinct branch that benefits from strong spin-orbit coupling and does not suffer from the same conduction-band valley-degeneracy problem as silicon electron qubits. Donor spins use implanted or atomically placed dopants in silicon. GaAs spin qubits (not shown here) were historically important but are strongly affected by nuclear-spin noise. Other avenues include electrons in carbon nanotubes and electrons above liquid helium or solid neon. These platforms have very different maturity levels and not all of them can even be described as supporting silicon spin qubits. The qubit encodings are summarized in Figure 116. 🅭 Olivier Ezratty, 2022-September 2026.

croscopy was also discussed historically, although electrical spin-to-charge readout has become the more relevant scalable route.

The challenges lie with the way to precisely position the phosphorus atoms in the silicon lattice [1289] and how to control qubit entanglement and readout [1290]. This is the path chosen by Michelle Simmons at UNSW and in her startup SQC. The individual atoms are positioned in the silicon structure with lithography using a scanning tunneling microscope (STM).

The first processor fully implementing this architecture was announced by SQC in 2022 (we cover it later). Similar options are pursued like the use of antimony nuclei embedded in silicon lattice structures and controlled by microwaves by Andrea Morello from UNSW [1291, 1292]. However, Morello et al. also work on phosphorus-based donor spins, and even along Andrew Dzurak, although his company Diraq is using SiMOS and not donor spins for their qubits [1293].

Later, Andrea Morello and Patrice Bertet designed another hybrid approach, coupling transmon superconducting qubits (for computing) and phosphorus in silicon nuclear spins with a donor electron (for creating a quantum memory) [1294].

On top of the above two mainstream paths (Si-MOS/CMOS and spin donors), several other avenues are investigated in the quantum dots based spin qubit realm:

- **Si/SiGe electron-spin and Ge/SiGe hole-spin heterostructures**. In Si/SiGe electron devices, electrons are confined in a silicon quantum well between SiGe barriers. In Ge/SiGe hole-spin devices, holes are confined in a germanium quantum well and benefit from strong spin-orbit coupling, enabling efficient all-electrical control [91, 1295]. Valley degeneracy is primarily an issue for silicon conduction-band electron qubits. TU Delft demonstrated fast two-qubit logic with Ge hole spins in 2020 [148], followed by a four-qubit Ge processor and a four-qubit GHZ state in 2021 [1296]. Heavy-hole and light-hole labels refer to the $J = 3/2$ valence-band manifolds, conventionally associated with $m_J = \pm 3/2$ and $m_J = \pm 1/2$ projections. The logical qubit itself is an effective two-level pseudospin, not a spin-3/2 or spin-1/2 particle in the elementary-particle sense [1297, 1298].

- **Gallium-arsenide** (GaAs), first tested in 2005, but with very short coherence times due to hyperfine noise from the nuclear spins of naturally occurring gallium and arsenic isotopes.

- **Electron spins in carbon nanotubes** are investigated by C12 Quantum Electronics and academic groups [1299]. Carbon materials can offer a low nuclear-spin environment when isotopically purified and can couple to microwave resonators. However, reproducible nanotube placement, disorder, contact quality and device-to-device variability remain important manufacturing challenges. Carbon nanospheres

are investigated by Archer Materials, but that program had not publicly demonstrated any operational qubit as of September 2026. Claims that all such qubits can be made intrinsically identical or frequency matched at scale are therefore premature [1300–1303].

- **Electrons trapped on solid neon or superfluid helium** form a separate trapped-electron family. The 2022 solid-neon experiment encoded the qubit in the motional states of a single electron and demonstrated $T_1 = 15$ μs and $T_2 > 200$ ns, so it was a charge/motional qubit rather than an electron-spin qubit [1304]. More recent solid-neon work also reports charge coherence [1305]. Spin-based qubits for electrons above superfluid helium have long theoretical coherence-time estimates and are pursued experimentally, but the complete spin-qubit gate stack remains much less mature than silicon quantum-dot spin qubits [1306, 1307]. UNSW is also investigating electron-on-neon device structures [1308] (Figure 114).

These qubits' small dimensions and the possibility to integrate control electronics in or around the qubit chip make it an interesting candidate for large-scale quantum computing [115]. There are however many challenges to overcome, particularly with materials design [1335, 1336] (Table 5).

While in most cases, silicon qubits are planned to be used in the gate-based paradigm, it can also implement quantum simulations in analog mode [1337, 1338].

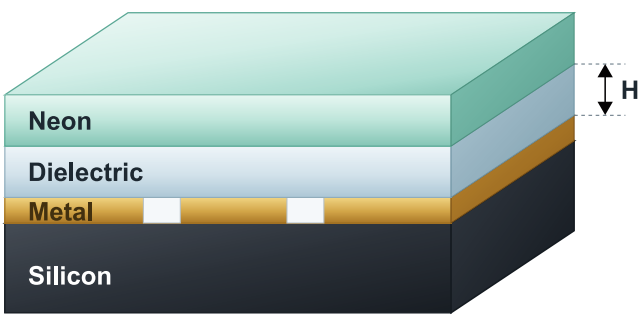

Figure 114: UNSW electron-on-neon supporting chip with neon deposited on a dielectric layer above a metal layer and silicon wafer substrate. The confinement frequency depends on the dielectric geometry, including the height H, which is optimized around 10 nm in the cited design. The cited device demonstrates confinement engineering but not yet the full initialization, coherent-control, two-qubit-gate and readout stack required for a processor. Source: [1308].

1.4.2 Science

Spin qubits have one of the smallest physical footprints among leading gate-model qubit technologies, with gate pitches of order tens to hundreds of nanometers. This creates a path toward very high on-chip qubit density, potentially reaching millions of physical qubits per large die or multi-die module in future architectures. Claims of billions of operational qubits on a single chip are roadmap extrapolations, not demonstrated engineering results, and spin qubits are not the only technology with a path to large-scale integration. Coherence and gate-error performance can be competitive with superconducting qubits in small devices, but maintaining those figures of merit while scaling control, readout, calibration and yield remains an open challenge [1339].

A subset of semiconductor spin-qubit architectures uses circuit QED by coupling quantum dots to superconducting microwave resonators. This is not the default architecture for all silicon spin qubits. In such devices, the charge or spin state changes the resonator susceptibility and can be measured dispersively from the phase and amplitude of a reflected or transmitted probe tone, often using homodyne or heterodyne detection. Electron spin resonance (ESR) and electric-dipole spin resonance (EDSR) are principally spin-control and spectroscopy techniques. They are not, by themselves, readout techniques, although resonators can participate in both control and readout chains [1345, 1346].

There are multiple ways to encode a qubit in gate-defined quantum dots, using one, two or three confined spins per logical or physical qubit (Figure 116).

Silicon spin qubits can in some devices operate near or above 1 K because the relevant orbital, charging and Zeeman energy splittings can remain large compared with the thermal energy k_BT, not because the control microwaves themselves have more energy. At 1 K, $k_BT \approx 86$ μeV. For an electron with $g \approx 2$ in a 1 T field, the Zeeman splitting is about 116 μeV, corresponding to an ESR frequency near 28 GHz. Higher magnetic fields therefore improve thermal spin polarization, while readout and charge-state broadening can still become limiting. The higher operating temperature can substantially increase the available cryogenic cooling power for nearby control electronics. Large dilution refrigerators can provide cooling power of order mW near 100 mK, compared with only order tens of μW near 10–20 mK [94, 1316].

The often-quoted limit of about 10,000 cryogenic CMOS transistors near the qubits was an architecture-specific power-budget estimate, not a fundamental limit [93]. The achievable transistor count depends strongly on CMOS node, duty cycle, operating temperature and thermal anchoring. Large-scale spin-qubit systems will require quantum error correction. Architectures combining shuttling or resonator-mediated interactions are not necessarily restricted to nearest-neighbor coupling and could therefore support codes with different connectivity and overhead tradeoffs than a strictly local 2D surface-code layout.

At the state-of-the-art level, researchers from Australia, QuTech [1352] and Jason Petta at Princeton have demonstrated two-qubit gates in different geometries. To get to the next step, the challenge is to control the electrostatic potential between the quantum wells where the electrons are stored - and thus their spin - with a

	specs	pros	cons
Si-MOS	silicon quantum dot [49, 1284]	mastered fabrication technique and scalability potential [95, 96, 158, 1309]	qubit decoherence, poor entanglement, disordered potential in materials [48, 90, 1310, 1311]
FinFET	silicon quantum dot [1312, 1313]	mastered fabrication technique and scalability potential [158, 1314]	disordered potential in materials [90, 1310]
Si/SiGe or Ge/SiGe	electron spins in Si quantum wells with SiGe barriers, or hole spins in Ge quantum wells with SiGe barriers [91, 1295]	high-fidelity gates, epitaxial interfaces, strong electrical control for Ge holes, and demonstrated operation above 1 K for selected silicon-electron devices [148, 1315–1317]	silicon electron devices require valley-splitting control and low charge disorder; Ge hole devices instead face spin-orbit, confinement and materials-uniformity tradeoffs [1318–1320]
GaAs	landmark coupled-electron-spin qubit experiments in GaAs/AlGaAs in 2005 [1283]	stable dopants, single conduction band valley, easy to manufacture, test platform for many characteristics with knowledge transferable to Si-MOS/FinFET/SiGe qubits [1321–1323]	nuclear spins effect and very small coherence time (T_2) [1283, 1324]
atom donors	phosphorus atom spin donor [1285]	long coherence time [1325–1327]	complicated to manufacture, impact of impurities [1289, 1290, 1328]
carbon nanotubes	electron spin trapped in carbon nanotubes or nanospheres [1299, 1329]	extremely clean dielectric environments, electrostatic shuttling potential and compatibility with microwave resonators; theoretical spin coherence on helium can be very long, but this has not yet been demonstrated in a scaled processor [1307, 1331]	only one company (C12 Quantum), low TRL, manufacturing scalability [1329, 1330]
electrons on neon or helium	single-electron motional/charge qubits on solid neon and proposed or developing spin qubits on superfluid helium [1304, 1307]		low TRL for a complete gate-model processor; EeroQ pursues electron-spin qubits on helium while solid-neon demonstrations are presently charge/motional qubits [1332, 1333]

Table 5: Specificities, strengths and limitations of representative semiconductor spin-qubit and trapped-electron platforms. For spin-qubit figures of merit, see the review in [1334]. 🅭 Olivier Ezratty, 2022-2026.

number of grids that allow the qubits to be arranged not too far apart, typically on the order of a few tens of nanometers. Understanding how spins behave and decohere is still an area of research, with the need for digital simulations [1343, 1344].

Also, a lot must be done in materials design and process manufacturing [90], particularly to fight charge noise affecting the spins [47, 48, 108]. Other issues to address relate to the drift in control frequencies due to gate operations originated system heating [1353] (see also Figure 115).

Spin-photon interfaces are a promising route to long-range connectivity, but one should distinguish demonstrated coherent coupling from full quantum-state networking. Coherent coupling of a silicon electron spin to a microwave cavity photon was demonstrated in 2018, and strong coupling of a silicon hole spin to a microwave photon was demonstrated in 2023 [1345, 1346]. Deterministic high-fidelity conversion of stationary spin states into flying photons suitable for distributed quantum computing remains a major engineering challenge.

Shorter-range connectivity may use coherent electron shuttling. Delft experiments have transported electrons over micrometer-scale distances with high transfer fidelity [1354, 1355]. Quantum Motion proposed the "quantum snake on a plane" architecture in 2025–2026, using shuttling ancillas to reduce connectivity constraints in surface-code layouts [1356]. Robert Wille's group proposed compilation and lattice-surgery methods for such layouts [1357] (Figure 117). The SNAQ architecture, or Shuttling-capable Narrow Array of spin Qubits, similarly uses shuttling to reduce wiring and geometry overhead [1358]. Other proposed routes use spin-microwave-photon interactions and superconducting resonators [1347, 1348].

Finally, carbon-nanotube spin qubits can in principle use superconducting microwave cavities to mediate interactions beyond nearest neighbors [1359]. Millimeter-scale microwave resonators are physically compatible with such links, but scalable high-fidelity long-distance two-qubit gates between separated nanotube spin qubits have not yet been demonstrated.

1.4.3 Qubit operations

The general principle of gate-defined spin qubits is to confine a spin carrier, an electron or a hole, in an electrostatic quantum dot separated from neighboring reservoirs or dots by tunnel barriers. A static magnetic field lifts the spin degeneracy and produces a qubit splitting within a selected orbital state. The field is usually supplied by a superconducting or permanent magnet inside or near the cryostat, although external room-temperature magnets can also be compatible with spin-qubit operation [1360].

quantum dot spin key takeaways

highlights

- **two-qubit gate fidelity** reaching 99.5% in a two-qubit silicon device, with 99.8% single-qubit fidelity [1340].
- **compact electrical control potential**: exchange-only encodings can use baseband electrical pulses, while single-spin ESR/EDSR implementations still require microwave-frequency control.
- **fast two-qubit gates**: about 75 ns with Ge hole-spin [148].
- **operating temperature**: some devices could operate in the 500 mK-1 K range, increasing the available cooling power for nearby electronics [94, 1316].
- **2D architectures** usable with surface codes or color codes QEC, shuttling electrons potential (SpinBus [97]).
- **300 mm semiconductor fabs** leverage [95, 96].
- **cryo-CMOS developments** for scalable qubit drive [92, 93].
- **high density potential** thanks to quantum-dot gate pitches below 100 nm, although million-qubit operation, wiring and yield remain to be demonstrated [49, 115].

challenges

- **research started later** than other qubit technologies and is spread over several platforms (Si-MOS, Si/SiGe, donor spins).
- **smaller commercial ecosystem** than superconducting or trapped-ion computing, although semiconductor-company and startup investment grew since 2024.
- **qubit addressing** and still unsettled drive and readout techniques (ESR, EDSR).
- **fab and characterization cycles** can take months, particularly when devices use external semiconductor foundries.
- **multi-qubit scale is still modest**: 18-qubit silicon and germanium arrays demonstrated in 2026 by HRL [1341] and TU Delft [1342], but with limited multi-qubit entanglement.
- **high qubit variability** requiring per-qubit calibration [44].
- **charge noise** and other noise sources to mitigate, with scalability still to be demonstrated [47, 48, 108, 109].

variations

- **Si/SiGe electron-spin and Ge/SiGe hole-spin qubits**: distinct heterostructure families with different valley, spin-orbit and fabrication tradeoffs [91, 1296].
- **donor spins** on a phosphorus atom nucleus, harder to scale [1285, 1289].
- **carbon-nanotube spins**: potentially low nuclear-spin disorder and strong cavity coupling, but manufacturing reproducibility and processor-scale control remain low-TRL challenges [1299, 1303].
- **electrons on helium or solid neon**: EeroQ targets spin qubits on superfluid helium, while current solid-neon demonstrations encode qubits in electron motional/charge states [1304, 1307].

path to scalability

- **materials purity improvements**, isotopic and elemental [90].
- **faster manufacturing** cycling and characterization.
- **full-stack EDA** for digital device simulation [1343, 1344].
- **long-range on-chip coupling and electron shuttling** may support lower-overhead non-local QEC, provided shuttling errors remain sufficiently low.
- **cryo-CMOS integration** co-located with qubits [92].
- **low-temperature digital control electronics**, including cryo-CMOS and potentially SFQ-based control, provided their dissipation and induced noise are compatible with the qubits.
- **inter-processor or long-range connectivity** may use coherent electron shuttling and microwave spin-photon interfaces, with scalability being an open engineering challenge [1345–1348].

Figure 115: Quantum dot spin qubits highlights, challenges, variations and path to scalability. © Olivier Ezratty, 2021-2026.

Single-qubit rotations may be driven by ESR with an oscillating magnetic field or by EDSR with an oscillating electric field coupled to the spin through spin-orbit interaction or a magnetic-field gradient. Spin qubits are not immune to electrical noise. Charge noise couples to the spin through exchange, spin-orbit interaction, micromagnet gradients and charge admixture, while phonons contribute to spin relaxation. Two-qubit gates commonly use tunable exchange coupling, and readout generally begins with spin-to-charge conversion.

Let's now look at the details [1361, 1362]:

- **Qubit quantum state** is generally encoded in the spin of a confined electron or hole. The carriers may be confined at a GaAs/AlGaAs interface, in a Si/SiGe or Ge/SiGe quantum well, or at a semiconductor-insulator interface in MOS devices. These structures can host a two-dimensional electron or hole gas. In the absence of a magnetic field, time-reversal symmetry gives a spin-degenerate Kramers pair. The static magnetic field, not cryogenic cooling, lifts that degeneracy through the Zeeman effect. Low temperature is nevertheless required to suppress thermal excitation, improve initialization and stabilize the single-carrier charge state [1363].
- **Single-qubit quantum gates** are commonly implemented by ESR or EDSR. Resonance frequencies range from several to several tens of GHz depending on magnetic field and effective g factor, with about 16 GHz in [1364]. ESR uses an oscillating magnetic field, while EDSR uses an oscillating electric field converted into an effective transverse spin drive through spin-orbit coupling or a magnetic-field gradient. Pulse phase selects the rotation axis in the transverse plane and pulse area sets the rotation angle. Three-spin exchange-only qubits can instead be controlled with baseband exchange pulses. The resonant-exchange qubit is one particular three-spin encoding.
- **Two-qubit quantum gates** commonly use electrically controlled exchange between neighboring spins. Gate voltages tune the tunnel coupling and detuning of adjacent dots, changing the exchange splitting J between the two-electron singlet and triplet manifolds. The triplet manifold is not simply "parallel spins": T_+ and T_- are parallel-spin states, while

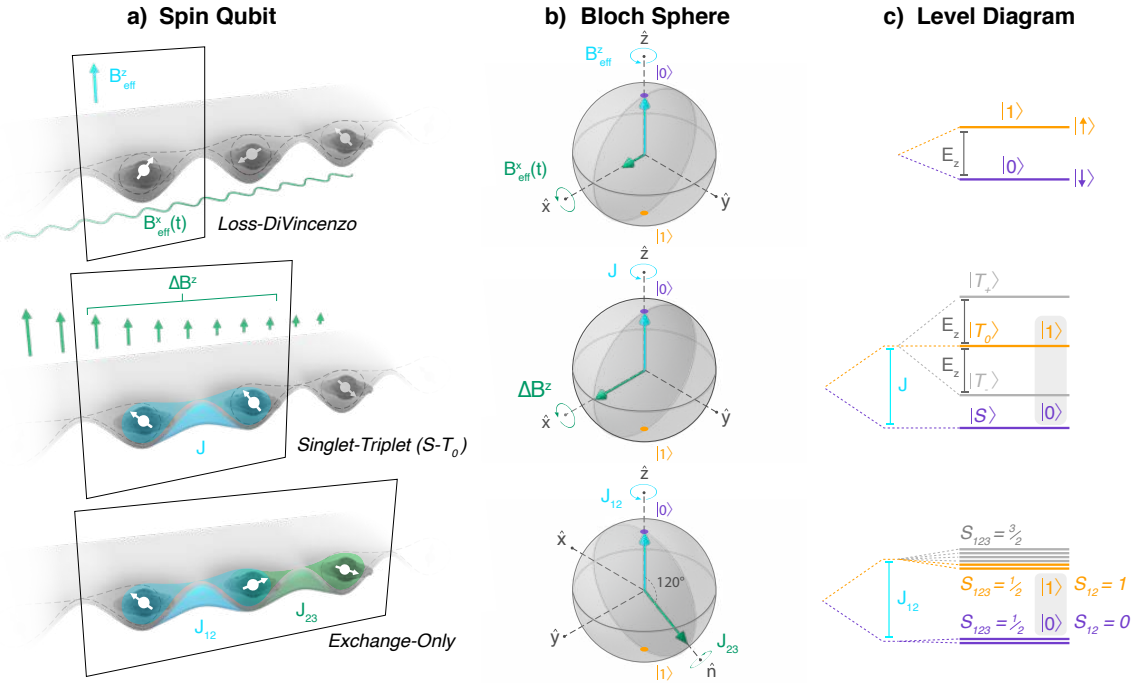

Figure 116: The number of quantum dots and spins used to encode a qubit depends on the chosen architecture and spin manifold. Representative encodings use one, two or three spins, although other encoded-spin schemes also exist. The one quantum dot per qubit corresponds to the Loss-DiVincenzo method. It encodes the physical qubit in a single electron spin and uses a static magnetic field B^z_{eff} to define the energy splitting, while single-qubit operations are driven by an oscillating transverse magnetic field $B^x_{eff}(t)$. On the Bloch sphere, the static field B^z_{eff} establishes the Z-axis, and the oscillating field $B^x_{eff}(t)$ is used to drive rotations around the X-axis. This is the most frequently used approach, by Intel, Quobly, Quantum Motion and Diraq. The two-spin singlet-triplet qubit uses two electron spins, usually in a double quantum dot. A common logical subspace is spanned by the singlet $|S\rangle = (|\uparrow\downarrow\rangle - |\downarrow\uparrow\rangle)/\sqrt{2}$ and the unpolarized triplet $|T_0\rangle = (|\uparrow\downarrow\rangle + |\downarrow\uparrow\rangle)/\sqrt{2}$. The polarized triplets $|T_+\rangle = |\uparrow\uparrow\rangle$ and $|T_-\rangle = |\downarrow\downarrow\rangle$ lie outside the logical subspace and are split by the Zeeman energy. Exchange J and a magnetic-field or Zeeman-energy gradient ΔB^z provide two non-commuting control axes. This encoding remains mainly a research platform rather than the dominant industrial single-spin approach [1349]. The three-spin exchange-only qubit encodes a logical qubit in the total-spin $S_{123} = 1/2$ subsystem of three exchange-coupled spins. Pulsing J_{12} and J_{23} provides universal single-qubit control without local oscillating magnetic fields. The logical basis can be labelled by the pair-coupling quantum number S_{12}, but the $S_{12} = 1$ logical state is a Clebsch-Gordan superposition within the total $S_{123} = 1/2$ manifold, not simply a bare triplet product state. HRL used this encoding in its 2026 processor containing 54 exchange-coupled quantum dots configurable as up to 18 exchange-only qubits [1341]. Single-spin, singlet-triplet and exchange-only encodings have all been demonstrated in semiconductor quantum-dot systems, but not every encoding has been demonstrated with comparable maturity in every Si, Si/SiGe and Ge/SiGe material platform. Germanium work is predominantly based on hole spins, while most industrial Si-MOS programs use electron spins. Source: [1350, 1351].

$T_0 = (|\uparrow\downarrow\rangle + |\downarrow\uparrow\rangle)/\sqrt{2}$ is an antiparallel-spin superposition. Exchange evolution generates SWAP-family, controlled-phase or equivalent entangling gates depending on the operating regime.

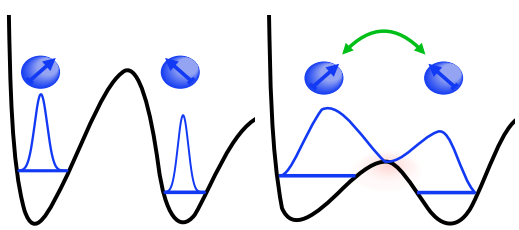

Figure 118: How a two-qubit gate is implemented with reducing the tunnel barrier between two spins. Source: Maud Vinet, in a past presentation.

- A J gate involves tuning exchange between two spins by changing the electrostatic barrier or detuning between their quantum dots. This is done with voltage pulses on barrier and/or plunger gates, not by intentionally injecting square current pulses into the qubit gates (Figure 118). Common primitive operations include $\sqrt{\text{SWAP}}$-family and controlled-phase gates, with many architecture-specific variants [1365].

- **Qubit readout** frequently begins with spin-to-charge conversion, after which a SET, quantum-point contact or gate sensor detects the charge configuration. In Pauli spin blockade, spin symmetry makes a selected interdot charge transition allowed for a singlet-like configuration but blocked for a triplet-like configuration. The mechanism does not "force the second electron spin to be opposite" to the measured spin [1366, 1367].

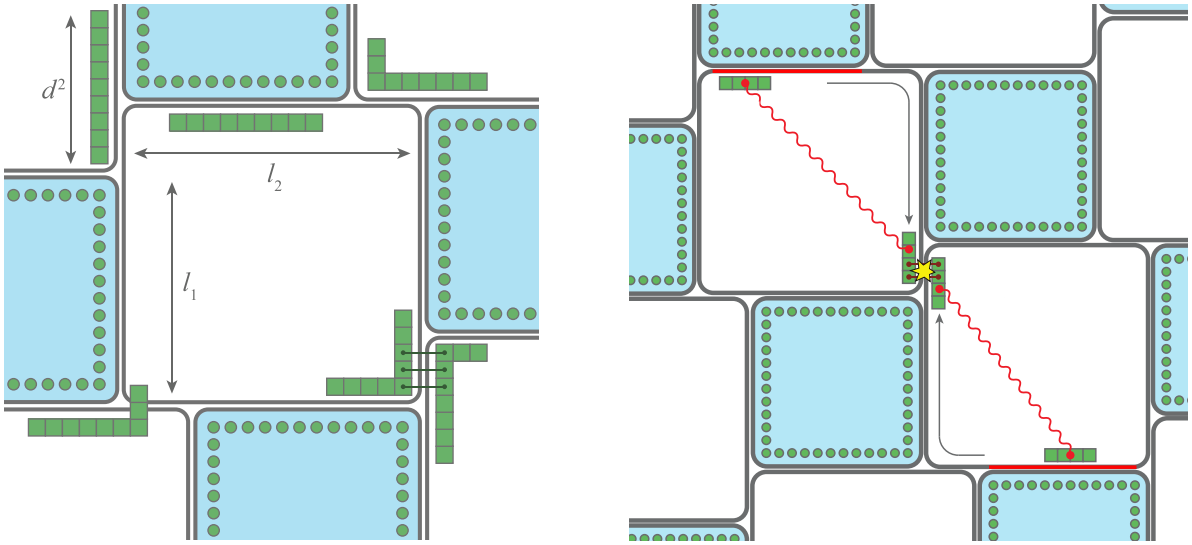

Figure 117: The snake-on-a-plane architecture proposed by Quantum Motion is shown on the left. Static data-spin locations are represented by green circles and shuttling ancilla electrons by green squares. The ancillas are intended to interact sequentially with separated data qubits for stabilizer measurements. On the right is a compilation and lattice-surgery proposal by Robert Wille's group using shuttling ancillas to connect distant data qubits. These are architecture proposals rather than demonstrations of a fault-tolerant processor. Sources: [1356, 1357]. Added in September 2026.

- Gate-based readout often applies a radio-frequency probe to a gate or resonator and detects the phase and amplitude of the reflected signal, a technique known as gate reflectometry [1368]. Quantum non-demolition (QND) readout does not avoid quantum-state projection. Instead, it is designed so that a projective measurement preserves the measured eigenstate with high probability, allowing repeated measurements. Silicon-spin QND readout has been demonstrated with an ancilla spin coupled through an Ising-like interaction [1369]. Other readout approaches use resonant tunneling or superconducting resonators [1370, 1371].

In typical circuits, qubit drive is usually implemented with several control lines: L, the reservoir lead; P, the plunger gate controlling dot occupancy; T or B, the barrier gate setting the tunnel coupling between quantum dots; and S and D, the source and drain.

1.4.4 Research

Here are now the main research laboratories that are exploring the silicon spin path, very often in multi-laboratory and multi-country partnership ventures. We'll focus first on the Netherlands, Australia, France and the USA, and will then cover other countries.

In The Netherlands, TU Delft and QuTech are among the most active research organizations in Europe around quantum dots based qubits.

This activity is centered in Lieven M. K. Vandersypen's lab at QuTech.

Two main technology paths are explored there with Si-MOS quantum dots in partnership with Intel since 2015, and on silicon-germanium qubits under the leadership of Menno Veldhorst and Giordano Scappucci. On top of his main role at Forschungszentrum Jülich in Germany, David DiVincenzo is also a professor at the EEMCS Department at the TU Delft and a contributing scientist at QuTech. TU Delft collaborates on germanium qubits with Purdue University in Indiana and Wisconsin-Madison University.

In 2020, Menno Veldhorst's team demonstrated fast two-qubit logic with hole spins in a Ge/SiGe heterostructure. The experiment reported about 75 ns two-qubit operation and roughly 98% two-qubit fidelity, with high-fidelity single-qubit control [148]. These devices are based on epitaxial Ge quantum wells with SiGe barriers, not on a conventional silicon-on-insulator (SOI) transistor substrate.

In 2020, the Delft group demonstrated two-dimensional germanium quantum-dot arrays and high-quality hole-spin control. The four-qubit Ge hole-spin processor, including coherent generation of a four-qubit GHZ state, was published in Nature in March 2021 [1296] (Figure 119).

In 2022, the Delft team prototyped phase-error correction with four Ge hole-spin qubits [1373]. They later extended operation to six qubits, with 99.77% single-qubit gate fidelity and 71% to 84% two-qubit gate fidelity in that device [1315]. Separate two-qubit silicon spin experiments exceeded 99% and reached 99.5% two-qubit fidelity [1340, 1374]. A surface-code threshold near 99% is often quoted for idealized local stochastic noise and suitable circuits, but the practical requirement is architecture- and noise-model-dependent. Fault-tolerant

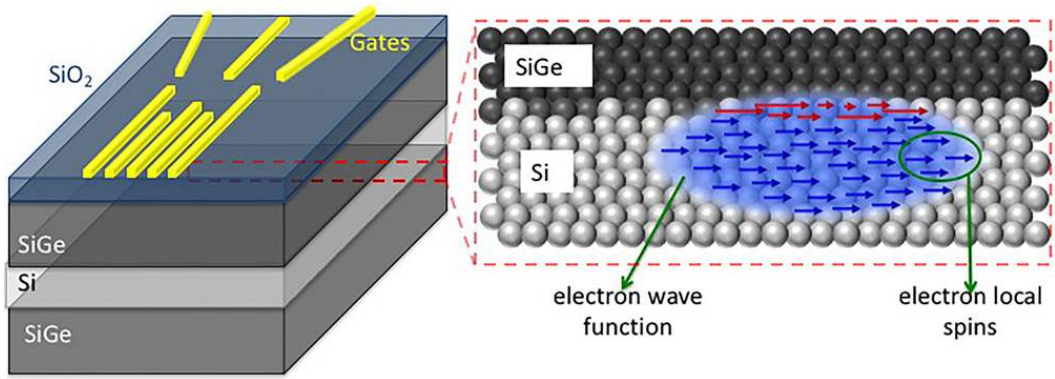

Figure 119: Silicon-germanium prototype qubits in 2020. Source: [1372].

operation also requires sufficiently good initialization, measurement, leakage control, correlated-noise suppression and decoding, not an arbitrary universal 99.99% gate-fidelity rule.

QuTech is partnering on the way to reduce charge noise in silicon spin qubits with the Seoul National University in South Korea [1375]. Sideways, the QuTech team, in collaboration with research teams from ICREA and IC2N in Spain, made interesting inroads with interfacing their SiGe qubits with a germanosilicide superconducting material. It could be useful in topological qubits design, to create gate-tunable superconducting qubits (**gatemons**), to create long-range coupling between spin qubits using superconductivity and microwave guides [1376, 1377]. At last, they demonstrated also in 2022 a 36×36 gate electrode crossbar supporting 648 narrow-channel field effect transistors (FET) to drive SiGe qubits [1378, 1379], and later developed a compiling solution to target this layout in the SpinQ project [1380].

QuTech and Intel demonstrated universal silicon spin-qubit logic at 1.1 K in 2020 [1316]. This is an important systems result because cooling power increases rapidly with temperature, although operation above 1 K can degrade initialization, readout and dephasing depending on device parameters.

Launched in 2022, the 4-year project ONCHIPS funded by the EU with €3M brings together a con-sortium of European research organizations: Universiteit Twente (the Netherlands, Floris Zwanen-burg), Technische Universiteit Eindhoven (Netherlands), Technische Universität München (Germa-ny), CNRS C2N (France), Universität Konstanz (Germany), Budapesti Műszaki és Gazdaságtudományi Egyetem (Hungary), and the Dutch company Single Quantum for photonic interconnect. The goal is to combine spin qubits for computation and photonics for communication on a SiGe platform compatible with traditional CMOS manufacturing.

Not far from Delft, **IMEC** is also testing silicon spin qubit chips, either other third party players like Quantum Motion, or for its own research. In 2025, they published some work related to the wiring of these chips which is challenging due to the small size of the quantum dots. They assembled in 3D the quantum dots chip and a cryo-CMOS chip, with the potential to scale up to 1,000 physical qubits [1381]. They also introduced in 2025 a multimode superconducting inductor architecture enabling radio-frequency reflectometry for qubit readout [1382].

In 2019, UNSW researchers were testing similar qubits at 1.5K [1383].

Australians are among the most active around silicon qubits, whether in the **CQC2T** teams at UNSW (University of New South Wales) or in other laboratories. Australian Universities are also teaming up with Microsoft Research. UNSW also received in 2018 a funding of $53M from the telecom operator Telstra, the Commonwealth Bank and the governments of Australia and the New South Wales region.

UNSW's **CQC2T** (Center for Quantum Computing & Communication Technology) laboratory is led by Michelle Simmons. She also cofounded and runs SQC, a silicon qubit startup that spun-out of UNSW. Their specialty is donor spin qubits using phosphorous atoms implanted in silicon wafers, along the Bruce Kane model created in 1998 at UNSW. This is a home run! In 2020, a team from the University of Melbourne showed how machine learning could help calibrate the placement of phosphorus atoms in a 2D structure of qubits on a silicon substrate [1384]. We'll cover these phosphorus-based qubits in the part dedicated to SQC a bit later in the vendor's list.

Two other key scientists at UNSW are Andrew S. Dzurak and Andrea Morello. Andrea Morello's team working with DoE's Sandia Labs published in 2022 results with a single-qubit gate fidelity of 99.95%, a C-Z two-qubit gate fidelity of 99.37% and 98.95% readout fidelity with two phosphorus nuclear spins coupled with a single silicon spin donor electron. They even produced a three-qubit entangled state (GHZ) with a fidelity of 92.5%. This was interesting but was not a "scalable" demonstration [1327].

Andrea Morello is best known for donor electron and nuclear-spin qubits in silicon, while Andrew Dzurak's group has been a developer of gate-defined SiMOS

quantum-dot electron-spin qubits. Their UNSW teams collaborated across these approaches. Pauli-spin-blockade and single-shot readout techniques were developed to enable scalable initialization and measurement [1385]. In 2019, Dzurak's group reported about a 2% two-qubit gate error and 99.96% single-qubit fidelity in a silicon quantum-dot device [1386].

Andrew S. Dzurak's group demonstrated in 2021 a global ESR-control approach using a potassium-tantalate dielectric resonator driven by a loop coupler [1387]. The resonator supplies a spatially broad microwave magnetic field for spin rotations, reducing the need for an individual microwave line beside every qubit. It does not by itself perform spin-state readout. Readout still requires spin-to-charge conversion and charge sensing. The architecture can therefore simplify microwave delivery while leaving separate challenges for frequency selectivity, DC addressing and readout.

The global ESR field in this prototype is generated by a dielectric resonator of about $0.7 \times 0.55 \times 0.3$ mm^3, much larger than the roughly 100 nm-scale quantum-dot structures (Figure 120). Individual qubits can be selected electrically by gate voltages that tune their resonance conditions, for example through Stark shifts or local electrostatic control, rather than by replacing all microwave signals with a "direct current tension". Spin readout remains a separate spin-to-charge and charge-sensing operation.

The next step is to implement the qubit circuit on isotopically purified ^{28}Si and check qubits coherence. While the solution simplifies the qubit chip wiring for some of the microwave lines, the prototype is based on using external microwave generators and readout systems, which doesn't scale at all. It circles back to a cryo-CMOS component that was developed by another Australian team and with Microsoft, which we describe in the cryo-CMOS section.

Andrea Morello's team is also studying remote coupling and quantum-memory concepts involving donor spins. For gate-defined quantum dots, the best-established spin-photon interfaces are in the microwave domain rather than direct visible-photon emission. Morello's group has developed donor-spin control methods that reduce flip and charge errors [1388]. It also demonstrated electrical control of the ^{123}Sb nuclear spin, whose $I = 7/2$ manifold provides eight nuclear-spin states [1389, 1390].

In France, the silicon qubit effort is driven by CEA and CNRS.

The involved groups are CEA-Leti, CEA-LIST, CEA-IRIG, CNRS Institut Néel and UGA (Université Grenoble Alpes). It also led to the creation in 2022 of Quobly, a spin-out of CEA-Leti and CNRS.

In October 2018, the Grenoble-based team of Silvano De Franceschi (INAC, CEA), Tristan Meunier (Institut Néel, CNRS) and Maud Vinet (CEA-Leti) obtained a €14M **ERC Synergy Grant** for their QuQube project, spread over 6 years to produce a 100-qubit electron spin CMOS quantum processor [1391].

Since March 2020, the Grenoble team is also coordinating the 4-year European Quantum Flagship project **QLSI** launched in February 2021. QLSI was a follow-up project from the European collaborative project **Mos-quito**, a 3-year project from 2016 to 2019 with €4M funding for studying the performance of different types of individual silicon spin qubits to provide recommendations for their large-scale implementation [1392]. QLSI was renewed as QLSI2 in July 2024 for 4 years. It consolidated fundamental research in silicon qubits, bringing together CEA, CNRS Institut Néel, Eviden, SOITEC and STMicroelectronics for France, IMEC (Belgium), Quantum Motion and UCL (UK), Infineon, IHP, U Konstanz, Fraunhofer and RWTH Aachen (Germany), UCPH (Denmark), TU Delft, U Twente and TNO (The Netherlands) and University of Basel (Switzerland). With a total budget of €15M (QLSI) and €25M (QLSI2), the goal is to manufacture and test 16 silicon qubits with gate fidelity of over 99%, and the preparation of a roadmap to scale beyond a thousand qubits.

The Grenoble silicon qubit project was led until 2022 by **Maud Vinet** (CEA-Leti) and **Tristan Meunier** (CNRS) until they launched **Quobly** in November 2022 (as Siquance). This story started about 10 years earlier when CEA-Leti got interested in silicon qubits as a way to extend a then flailing Moore's law. CEA-Leti implemented their first silicon quantum dots qubits in 2016 [1284].

Here are some of the specifics of this endeavor.

Different techniques. The Grenoble team mainly bets on Si-MOS silicon spin qubits. But they are still investigating SiGe qubits (CEA-IRIG), well as GaAs (for testing and calibration purpose) as well as silicon spin holes qubits, which are easier to control with a voltage on the quantum dot transistor gate [1393, 1394].

Manufacturing capacity is a key asset from CEA-Leti, being one of the few public laboratories in the world with a CMOS component test production platform (IMEC is their counterpart in Europe, in Belgium). It includes all the tools required to produce 200 mm and 300 mm wafers. It allows the production of all kinds of components in silicon, germanium and III-V materials (photonics, gallium arsenide, gallium nitride, etc.).

CEA-Leti's clean rooms are spread over several buildings, with the main one being 185 m long on 8,000 m^2 (Figure 121). Here, CMOS qubits manufacturing process uses 300 mm SOI wafers on with an additional thin layer of 99.992% purified 28-isotope silicon. The first test of spin control with isotopically purified silicon was achieved in 2011 [1325]. Validated production is to be later transferred to volume production in commercial

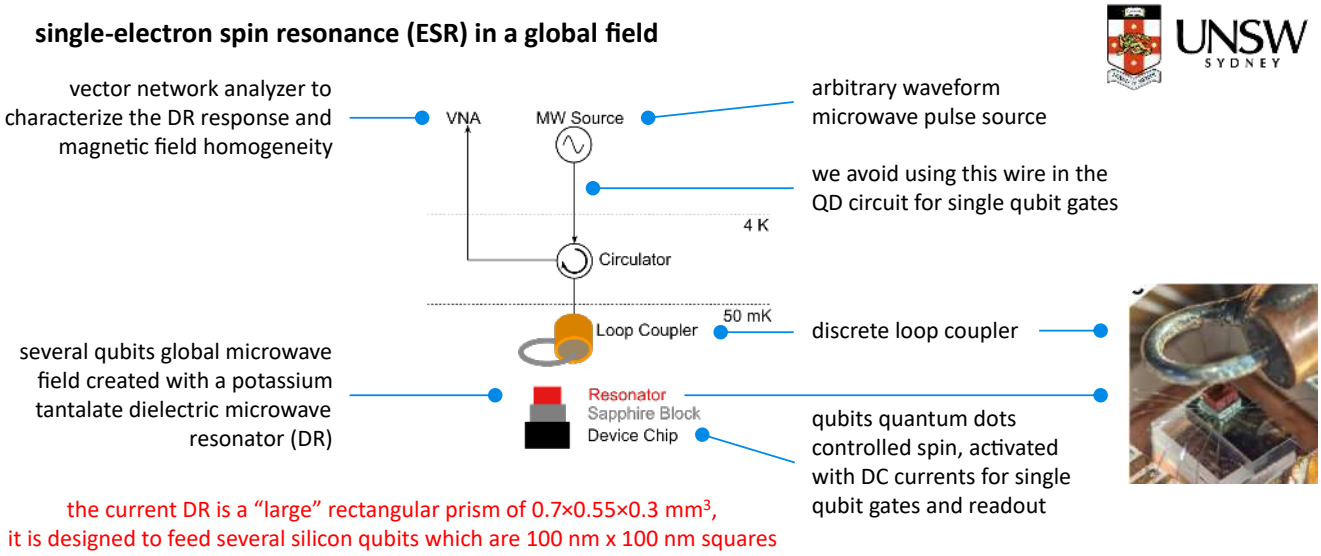

Figure 120: Proposal to improve the scalability of spin qubits with removing some the microwave circuits within the qubit chip and providing these microwaves to the qubit quantum dots with a dielectric microwave resonator. Source: [1387].

fabs such like those from STMicroelectronics in Crolles, France, or GlobalFoundries in the USA or Germany.

In its early stages, the size of the quantum computer market will be modest. In a conventional batch of 25 wafers alone, you can produce several thousand quantum chips in a single run, enough to power a large base of quantum supercomputers. But industry-grade clean rooms ensure quality processes that are not necessarily found in pre-production clean rooms.

Staging progress with the Grenoble team expecting to progress in stages over a six-year period starting in 2019: demonstration of a two-qubit silicon-based gate, demonstration of quantum simulation in a 4x4 array based on III-V material, demonstration six qubits in silicon, development of error correction codes and adapted algorithms, and fabrication of 100 2D array qubits in silicon at the end of this journey.

Control electronics with the Grenoble team creating control electronics operating at cryogenic temperature. The 2D architecture of Leti's CMOS chip contains several layers with silicon qubits and then the integrated electronics for control and qubit readout wiring. The qubits are distributed in 2D, but the integration of the components is also vertical within the components (Figure 122).

The measurement layer is located below the qubits while the layer for activating the qubits with quantum gates is above. For N^2 qubits, they would need 2N control lines (horizontal, vertical) instead of $2N^2$, which would generate an appreciable gain in connectivity. The technique would work to generate one- and two-qubit quantum gates [1396].

The great challenge of these architectures is their variability, i.e., the differences in behavior from one qubit to another and from one circuit to another. This leads to a need for precise calibration, qubit by qubit, of the microwaves controlling and reading the state of the qubits. As for superconducting qubits, this calibration can be done using dedicated machine learning software [44]. They use superconducting materials for the metal layer of these circuits, based on titanium nitride. This provides low resistance and reduces the noise of qubit state measurement.

3D stacking is used to arrange chips components in 3D [1397], which can help solve various scalability problems. CEA-Leti is using its CoolCube technology. The reference publications of these teams on CMOS qubits are numerous [1284, 1396, 1398, 1399].

Long-range coupling and shuttling are complementary research directions. Spin-photon coupling can mediate interactions through microwave resonators, while coherent electron shuttling physically moves the spin carrier between sites. At Institut Néel, coherent shuttling over micrometer-scale distances has been investigated. A few micrometers is already long compared with a typical quantum-dot pitch of tens to hundreds of nanometers [1323].

In the USA, on top of Intel, several research labs are working on electron spin qubits.

Let's factor in the already mentioned **DoE Sandia Labs**, **Purdue University** and the **University of Wisconsin-Madison** [1400]. They work on Si and SiGe device physics and error-correction architectures [1401–1403]. **Princeton University** and Jason Petta's team demonstrated a resonantly driven silicon spin CNOT gate in a paper published online in December 2017 and in Science in January 2018. The CNOT operation took about 200 ns. The reported greater-than-99% fidelities referred to single-qubit gates, while the generated Bell state had 78% fidelity after correction for state-preparation and measurement errors [1404]. They

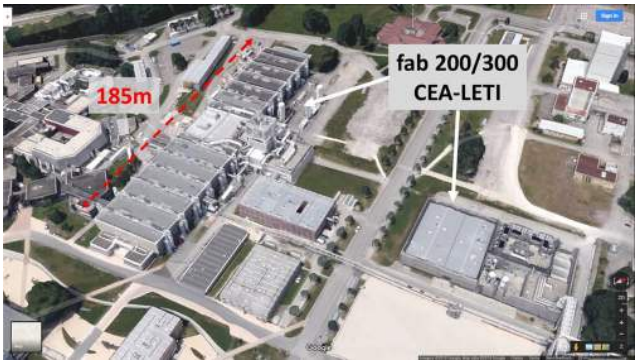

Figure 121: The CEA-Leti's pre-industrial 200/300 fabs aerial view in Grenoble as of 2018.

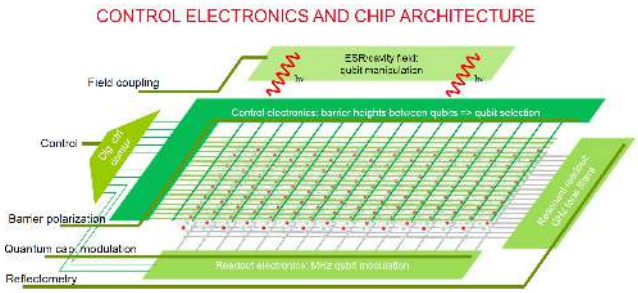

Figure 122: 2D wiring to access spin qubits with scalable wiring. Source: [1395].

continue to work on Si/SiGe qubit fundamentals [1405, 1406].

Princeton's key 2018 result in this context was coherent coupling between a silicon double-quantum-dot electron spin and a microwave photon in a superconducting resonator, not optical monitoring of the spin state [1345]. Subsequent work developed related microwave cavity-mediated coupling and readout techniques [1407].

UCLA and **Virginia Commonwealth University** are working on nanomagnets to drive silicon qubits [1408].

Finally, **HRL Malibu**, a joint research subsidiary of Boeing and General Motors located in California was working on both GaAs and Si / SiGe spin qubits. In 2022, they achieved a CNOT gate fidelity of 96.3±0.7%, SWAP fidelity of 99.3±0.5% with 6 silicon qubits arranged in a 1D array [1410]. They also work on triple-dot qubits with long lifetimes and better self-error correction [1411]. In 2025, they tested a "SLEDGE 2D" array of 15-qubit Si chip [1412]. In 2026, they realized a test chip with 18 SiGe hole spin qubits supported by 54 quantum dots [45].

Let's finish this list with a couple of other countries:

UK: another active country in silicon spin-qubit research, particularly at **Oxford University**, **Cambridge University** and **UCL** [1413], as well as through the startup **Quantum Motion**.

Switzerland: the Swiss National Science Foundation launched **SPIN** (Spin Qubits in Silicon) in December 2019. The project, led by the University of Basel [1314], also involves ETH Zurich, EPFL and IBM Research Zurich. IBM's work with silicon spin qubits is a research diversification that was completed by its acquisition of HRL Laboratories on August 26, 2026. Daniel Loss remains a central researcher in spin-qubit theory and collaborates with international teams [1414–1416]. EPFL's Andrea Ruffino has also worked with Hitachi Cambridge on integrated silicon-qubit and cryo-CMOS readout circuits [1417].

Germany: at the **University of Aachen**, researchers created double quantum dot of silicon with graphene [1418]. Also involved are Infineon, Leibnitz Institute IHP Microelectronics, Universität Konstanz and Fraunhofer IPMS with its own cleanroom, Weierstrass Institute for Applied Analysis and Stochastics [1320], and FZ Jülich [1419].

Denmark: **Niels Bohr Institute** and **CEA-Leti** collaborated to build a silicon qubit 2x2 matrix using single electrons quantum dots. These were fabricated on a classical 300 mm SOI wafer coming out of the CEA-Leti fab in Grenoble. While not being operational qubits, these quantum dot electrons were controllable with voltage pulses bases gates. They also implemented electron swaps, that could be useful in optimizing SWAP gates in future systems [1420]. In another work with Purdue University in the USA, NBI researchers implemented four GaAs qubits in a 2×2 array [1322, 1421].

China also explores silicon qubits. They now publish more papers on this type of qubits [1422–1425]. They even explore donor spins platforms in Peihao Huang's team in Shenzhen [1426, 1427], and SiGe in Tian Pei's team from BAQIS in Beijing [1428].

Taiwan is also exploring the silicon qubit domain, including Pei-Wen Li's team from NCTU, Hsi-Sheng Goan's team at NTU and Tzu-Kan Hsiao at NTHU who are working on SiGe quantum dot spin qubits [1429, 1430]. **Silicon Quantum Dot** is a stealth startup in that field.

Japan: silicon spin qubits are investigated in many laboratories. RIKEN and collaborators demonstrated quantum non-demolition readout of an electron spin in silicon in 2020. The protocol used a neighboring ancilla electron spin coupled through an Ising-like interaction and achieved repeated projective measurements with high non-demolition fidelity. It was not based on ferromagnetism or on measuring the spins of neighboring atoms [1369]. RIKEN-led teams have also worked on electron shuttling [1431, 1432], 99.5% two-qubit gate fidelity [1340], quantum error correction [1433] and correlated noise [1434]. Other Japanese work includes

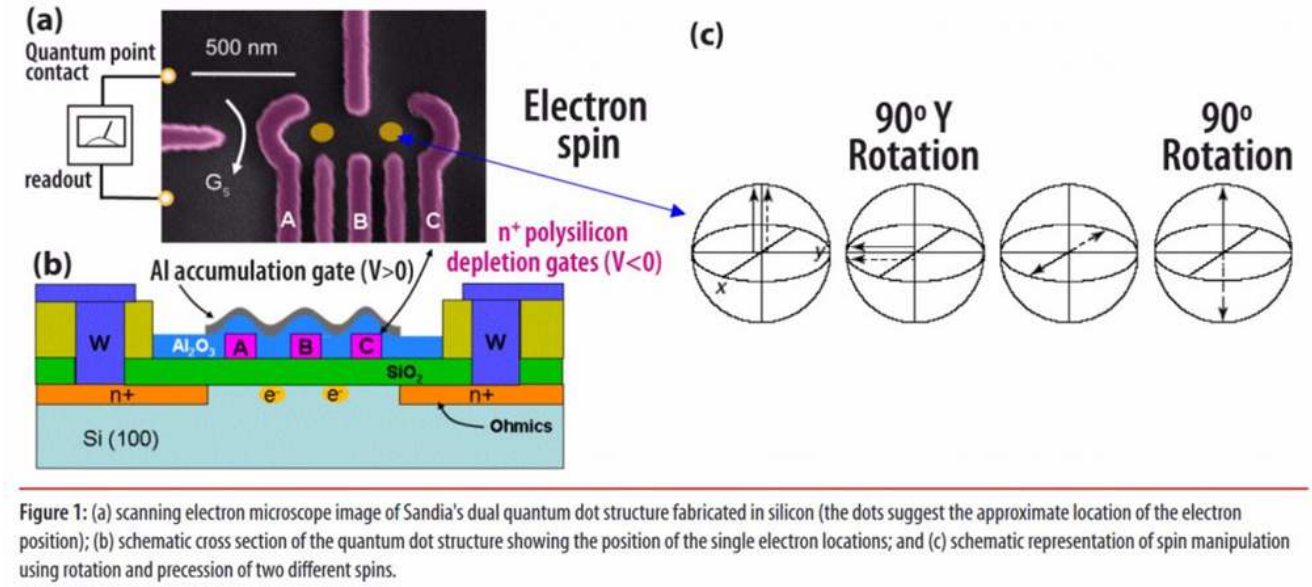

Figure 1: (a) scanning electron microscope image of Sandia's dual quantum dot structure fabricated in silicon (the dots suggest the approximate location of the electron position); (b) schematic cross section of the quantum dot structure showing the position of the single electron locations; and (c) schematic representation of spin manipulation using rotation and precession of two different spins.

Figure 123: Typical double quantum dot spin qubit. Source: [1409].

Waseda University and Hitachi programs in Si/SiGe spin qubits [1435–1439], as well as Hitachi-IMEC collaborations [1440, 1441]. Hitachi has also proposed magic-state-generation methods adapted to SpinBus-like architectures [1432, 1442, 1443].

1.4.5 Vendors

Key vendors are arranged here by qubit variation and alphabetical order: Si-MOS/FDSOI electron spins with **Diraq** (Australia), **QPi** (India), **Quantum Motion** (UK) and **Quobly** (France); Si/SiGe electron-spin architectures with **ARQUE** (Germany), **equal1.labs** (Ireland/USA) and **Intel** (USA); Ge/SiGe hole-spin qubits with **Groove Quantum** (the Netherlands); donor spins with **SQC** (Australia); carbon-based approaches with **C12 Quantum Electronics** (France) and **Archer Materials** (Australia); and electrons on helium with **EeroQ** (USA). These categories are approximate because several companies investigate more than one device variant.

Diraq

Australia, 2022, $114.8M

Diraq is a startup spun out of UNSW created by Andrew S. Dzurak that develops quantum dot spin qubits.

Company. The team contains a bunch of scientists and engineers like Arne Laucht, Henry Yang, and quantum theorist Stephen Barlett who joined the company in 2025. Andrea Morello from UNSW is also a scientific advisor for the venture. Morello and Dzurak were previously working with Michelle Simmons in her company SQC and they parted away in 2021. The founding team has a good track record in the advancement of quantum dots based qubits with many "firsts" achieved since 2014, including many patented processes (SiMOS - Silicon-Metal-Oxide-Semiconductor qubits, resonators, and qubit electrical control, etc.). They had a team of over 50 people as of mid-2025. Since 2026, Diraq's chairman is Scott McGregor, a former CEO of Broadcom.

Technology. The company has discussed an ultimate billion-qubit architecture. Its dated roadmap should be read separately from that long-term scaling study. Their roadmap published in 2025 includes three phases, a first one with 9 qubits, a second with 1,000 physical qubits and the first logical qubits, and a third one with millions of physical qubits ready to run commercially available algorithms (Figure 124). As of mid-2026, their experiments involved between 4 and 8 qubits.

Here are the various piecemeal scientific advances made by Diraq through various collaborative research publications: on their qubit initialization fidelities [1444], qubit control [1445–1448], direct spin readout with a microwave parametric amplifier [1449, 1450], error suppression techniques [1451], qubit gates fidelities variability [1310], benchmarking with about 99% two-qubit gate fidelity, corresponding to about 1% error, on a two-qubit chip [1311], multiple electron qubits [1452], GHZ state generation [1453], 2D quantum dots arrays architecture [1454], nuclei qubit entanglement with a CZ gate with each atoms binding separate entanglement intermediation electrons [1455–1457], a two-qubit Bell experiment with S=2.731 and a Bell state fidelity above 97% [1458], the use of "charge-driven spin" (CDS) control to apply some readout-based conditional logic locally without routing the information to the room-temperature classical layer and FPGAs [1459], and some work on the optimization of the operating qubit temperature which could be optimal at around 1 K [1460].

In work published in 2024, Diraq and UNSW demonstrated high-fidelity spin-qubit operation above 1 K, including single-qubit fidelities up to about 99.96% and

Figure 124: Diraq roadmap as of mid-2025. They plan to reach a million physical qubits by 2033. Source: Diraq website as of July 3rd, 2025.

two-qubit fidelities near 98.9% in the reported operating regimes [147]. The group also studies high-spin donor nuclei such as ^{123}Sb, which provide multi-level nuclear-spin qudits and support QND-style readout protocols [1461–1463], as well as coupling to ^{73}Ge nuclei [1464].

FTQC. Diraq works with Iceberg Quantum (Australia) for building resource estimates to support qLDPC codes based on Iceberg's Pinnacle architecture introduced in 2026. They announced in September 2026 the support of 1,000 logical qubits with 150K physical qubits, with no companion scientific paper.

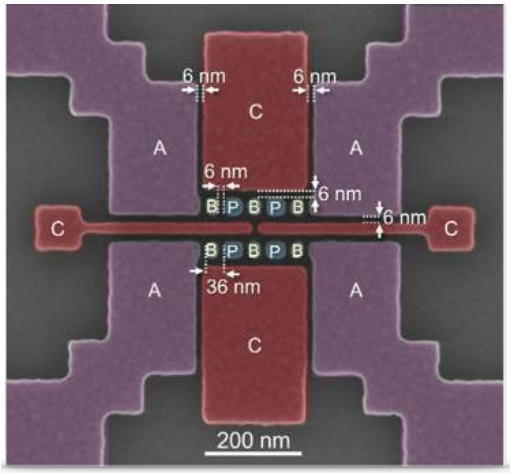

Figure 125: IMEC prototype 4-qubit SiMOS chip presented in 2026 with High-NA EUV lithography with gate gaps of 6 nanometers between the plunger (P) and barrier (B) gates. Source: [1465].

Manufacturing. In 2024, Diraq reported single-qubit gate fidelities above 99.9% [1466]. In July 2024, Diraq and academic partners showed that cryo-CMOS control could be used with limited degradation of qubit performance [92]. Their devices involve GlobalFoundries and IMEC manufacturing flows, including 300 mm wafers and High-NA EUV process development [95, 96, 1467, 1468] (Figure 125). In May 2026, the U.S. Department of Commerce announced a letter of intent for up to $38M in planned CHIPS R&D funding for Diraq. The program stated that recipients would provide the government a minority, non-controlling equity stake as a condition of the incentives. Diraq is also in Phase 2 of DARPA's Quantum Benchmarking Initiative.

Energy. Like most silicon spin qubit vendors, Diraq plans to support a million physical qubits at a very modest cost, including with power consumption. It even estimates that as the number of qubits grows, the share of cryogenic costs will become significantly smaller. In the end, the main cost will come from classical control, and particularly from quantum error syndrome detection [1469].

Fidelities. In 2025, they announced single and two-qubit gate fidelities over 99% and SPAM fidelity over 99.9%, in a two-qubit chip thanks to more efficient ways to limit charge noise [95]. They upscaled their experiment to 8-qubits in December 2025, but without characterizing two-qubit gates [1470] (Figure 126).

Side project. In March 2025, Diraq and Fermilab were awarded the DOE's Quandarum project under the QuantISED program, for developing quantum sensors to detect axions in the investigation of dark matter. They are reusing some of their process to create a quantum sensor based on their spin qubits along with Fermilab's cryogenic analog to digital converter.

Customers. In September, Diraq announced the deployment in October 2026 of a 8-qubit system in Equinix's data center in Australia. They are supposed to test quantum and classical AI applications integration.

Qpi

India, 2019, $6.5M

Qpi is a QML software and hardware development company, providing the QpiAI library. They are working on creating the ASGP (AI System Generating Processor), a hybrid classical-quantum compute chip.

Practically speaking, they planned first to introduce a qubit control chip in September 2021 operating at 4K and produced in a 22 nm TSMC CMOS process [1471]. This chip was to control the microwaves sent to both superconducting and electron spin qubits processors. They later announced a room temperature control chip named QpiAISense. They are now developing a

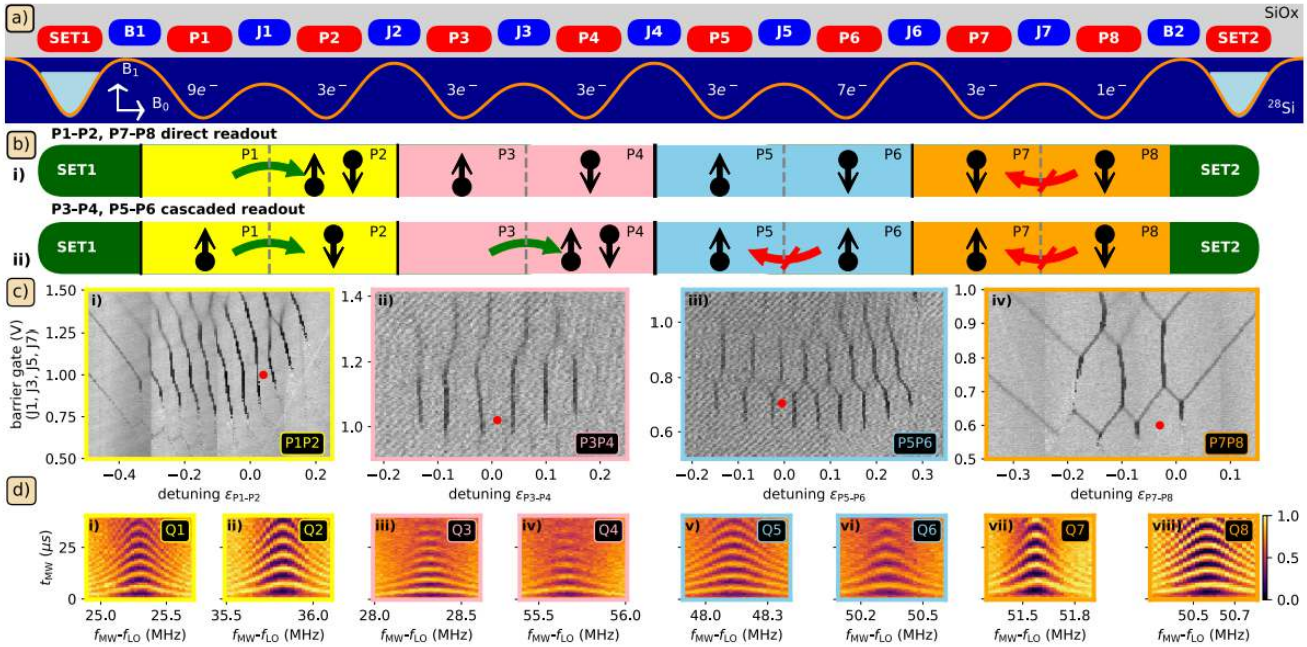

Figure 126: Diraq 8-qubit SiMOS chip manufactured in classical CMOS technology by IMEC in 2025, just before adopting High-NA EUV as shown in Figure 125. It details in a) a cross section of the device with silicon substrate (28Si), oxide layers, and plunger electrodes (Pi and SETi) and barrier (Ji and Bi) gates, in b) the spin-to-charge conversion readout techniques, in c) the charge stability maps, red circles marking the charge configuration used for the measured qubits and in d) the Rabi-chevron measurements for qubits 1-8. The Rabi chevrons show coherent oscillations, with peaks in bright yellow and white representing a high probability of spin-up and troughs in dark purple and black. Gate fidelity requires a calibrated benchmarking protocol and cannot be inferred from contrast alone. Source: [1470].

full-stack classical and silicon qubit solution in a single package. It is supposed to contain a classical chip for optimization (ASGP for "AI System Generating Processor"), their microwaves cryogenic control chip and a silicon spin-qubit based QPU (quantum processing unit).

They signed a partnership with QuantrolOx in April 2022 to develop their QPU and set-up a lab in Finland for that purpose, where part of QuantrolOx team is installed. Their goal is to start with releasing a functional 25 qubits system. They plan later to create a one-million-electron-spin-qubit processor. No public demonstration documents a device between the announced 25-qubit system and that target. QpiAI Tech is a subsidiary selling software services for quantum computing and AI to transportation, materials, manufacturing, finance, and pharmaceutical business.

Quantum Motion

UK, 2017, $223M

Quantum Motion is a UCL and University of Oxford spinout developing high-density silicon spin-qubit processors.

Company. Quantum Motion was co-founded by John Morton (UCL) and Simon Benjamin (University of Oxford) to industrialize silicon quantum-computing architectures developed across the UK academic ecosystem. In February 2026, it opened offices at the nanoGUNE Quantum Tower in Spain to support European development, integration and deployment.

Technology. Measurement was supposed to be carried out with a magnetic probe mechanically moved on the surface and making "square" movements, guided by a MEMS (micro-electro-mechanical device). This probe system was designed to avoid the use of control electronics and allow a better separation between the qubits [1472]. The paper is co-authored by John Morton and Simon Benjamin who are two cofounders of the startup Quantum Motion Technologies. Their Si-MOS qubits are mixing planar and 3D SOI components and are laid out to enable surface code error correction. A data rate separation process with intermediate mediation rates was limiting leakage effects [1473]. It seems that this technology is not the one they are now implementing.

In January 2021, Quantum Motion presented with Hitachi Cambridge, University of Cambridge and EPFL a 50 mK cryo-CMOS including quantum dot qubit arrays, row-column control electronics lines and analog LC resonators for multiplexed readout, using 6-8 GHz microwave resonators. This was a first step to implement time- and frequency-domain multiplexed scalable qubits readout [1417]. This work was extended in 2024 with a multi-module integration of a quantum dot qubit chip with a low-noise amplifier cryo-CMOS chip and a switch chip [1474]. They also assessed the thermal impact of this chip on the qubit chip [1475] and how to obtain readout fidelities of 99.2% using single elec-

tron box sensors [133]. They even developed their own cryo-CMOS based low temperature thermometer [1476].

In 2021, Quantum Motion and collaborators reported a single-spin relaxation time $T_1 = 9 \pm 3$ s at 1 T in a CMOS-fabricated silicon quantum dot, rather than a generic 9-second phase-coherence time [159]. Quantum Motion and UCL are also part of the Quantum Flagship QLSI program and have worked on remote capacitive charge sensing in silicon nanowire devices [1477].

Their roadmap consisted of producing 5 qubit "small cells" by 2022 in a structure that could then be reproduced in matrix patterns. They believe they can create a quantum computer with 100 logical qubits by 2029, a typical milestone for most quantum computer vendors. They provided an update on their architecture in an arXiv preprint in August 2022 [1478]. They then showcased in October 2022 the Bloomsbury 3×3mm^2 chip manufactured at Global Foundries containing 1,024 quantum dots and a year later, how they were efficiently characterizing the chip (Figure 127 and Figure 128) [1479].

Meanwhile, they are still designing their two-qubit gate, a $\sqrt{SWAP}$ [1480] and qubit readout along with IMEC [1481]. In 2025, they published work related to qubit readout using a compact dispersive spin-qubit sensor, a single-electron box (SEB) [1482] and an algorithm to recompile and simplify a circuit of consecutive multi-qubit phase rotations, to create fault-tolerant circuits for $|CCZ\rangle$, $|CS\rangle$ and $|T\rangle$ gates with a minimum number of T and CNOT gates [1483].

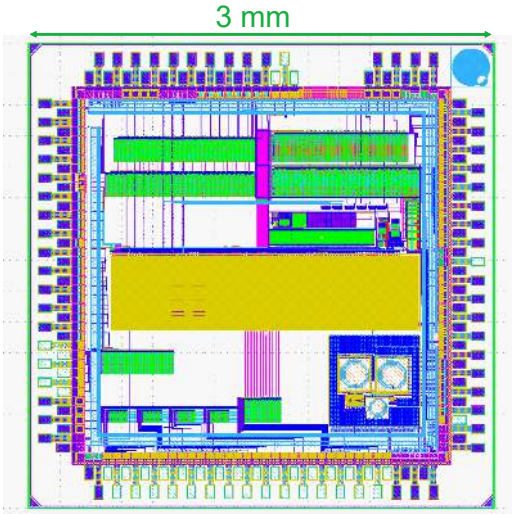

Figure 127: Quantum Motion Bloomsbury chip manufactured by Global Foundries. Source: Quantum Motion Q2B Santa Clara December 2023 presentation. Added in 2024.

In June 2023, they published a preprint describing an original pipelining architecture designed to facilitate the run of several similar shots serially on a single chip. Instead of using a grid with $\sqrt{N} \times \sqrt{N}$ qubits, they create an array with $N \times D$, D being the number of times a given shot must be executed. It can be useful for example for NISQ VQE algorithms where the same (Pauli string related) shot must be executed up to a million times, It is proposed for repeated-shot workloads under shuttling assumptions, and does not transpose generically to fault-tolerant computation, where syndrome cycles and logical circuits impose different constraints. The N qubits are shuttling from left to right in the circuit layout as shown in Figure 130 and are subject to series of rotation and coupling gates that are mandated in variational circuits using a QAOA gates ansatz. This supposes that electron shuttling works at this scale. In 2025 and 2026, they digitally simulated SiMOS electron shuttling and identified various problems and solutions to render it operational [1485] and they described how electron short-range shuttling could enable them to implement non-local quantum error correction codes using folded surface codes [1486]. In March 2026, Tim Chan from the University of Oxford proposed the Snowflake QEC decoder which improved decoding vs Union Find decoding on surface codes [1487]. In August 2026, it was tested at room temperature and at 4K running on AMD FPGAs [1488]. The conclusion was that, due to heat dissipation, operating such a decoder at 4K is unpractical.

In July 2026, they proposed an electron-shuttling based probe to detect charge noise, which is attributed to two-level fluctuators (TLFs) [109]. These are localized microscopic charge traps or defects at semiconductor-oxide interfaces in the qubit chip that randomly switch between two distinct charge configurations, generating charge noise that shifts electron spin qubit resonance frequencies and limits gate fidelity.

Software. Quantum Motion developed QuEST, an open-source, hybrid multithreaded and distributed, GPU accelerated simulator of quantum circuits. It works both on any laptop or on supercomputers. It supports pure (computational state vector) and mixed states (density matrices) to reproduce the effects of noise and decoherence [1489, 1490].

Customers. In February 2024, Quantum Motion was selected by the UK's National Quantum Computing Centre (NQCC) to build a QPU test bed [1491]. It got an additional public funding of $8M to develop a proof-of-concept. It was delivered in September 2025 [1484] (Figure 129).

Quobly

France, 2022, >€155M

Quobly, formerly Siquance, is the silicon qubit startup launched in November 2022 by Maud Vinet, Tristan Meunier and François Perruchot out of CEA-Leti and CNRS Institut Néel.

Company. They had a team of 100 as of mid-2026, including its academic partners. Since mid-2025, their Chairman is Philippe Delmas, a former VP from Airbus. On top of a first round of funding of €19M announced in July 2023, they got an EIC Transition grant of €2.5M. In 2025, they got an additional funding from the EIC, from

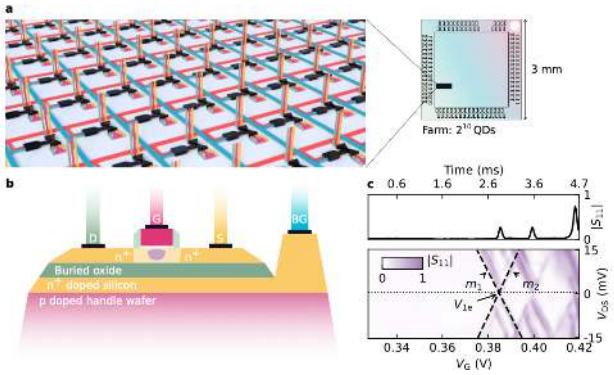

Figure 128: Quantum Motion chip layout with 1,024 integrated silicon quantum dots created in 2023. Source: [1479].

Figure 129: Quantum Motion's first full-stack system delivered to the UK NQCC in September 2025. The public announcement did not specify either the number of operational qubits or any gate-fidelity metrics. The separately mentioned 99.9% value refers to charge-sensor state discrimination, not to spin-qubit readout or gate fidelity. Source: [1484].

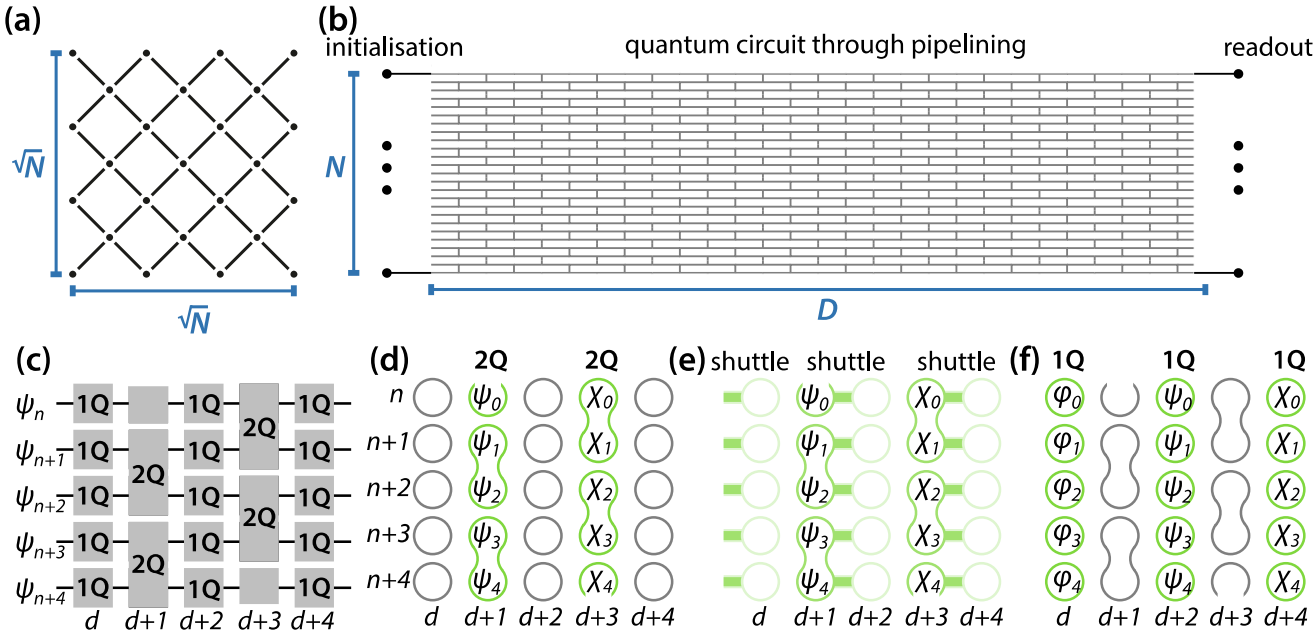

Figure 130: Quantum Motion's proposed pipeline architecture is adapted to running many shots of the same circuit. N spin carriers are physically shuttled horizontally through a 2D device and are subjected to sequences of single- and two-qubit operations as they move. The architecture aims to execute up to D serialized repetitions while reusing spatial control zones. This remains contingent on sufficiently coherent and low-error electron shuttling at scale. Source: [1492].

Bpifrance and VCs, totaling over €30M. They closed a Series A funding round of €115M in June 2026. They now have offices in Singapore (for their partnership with A*Star and Entropica Labs) and in Sherbrooke, Canada, to connect with the Montreal's software ecosystem.

Technology. They use SiMOS silicon spin qubits (Figure 133) but they are also investigating in parallel in silicon hole spins [1346]. They plan to create a QPU with a very low 12 m^2 footprint thanks to the use of low-power room temperature and cryo-CMOS control electronics (Figure 132). Their focus is manyfold, with tuning manufacturing processes to ensure the best qubit quality and with an end-to-end system approach, looking at ways to optimize cryogenics and control electronics, including CryoCMOS qubit control chips.

They developed a manufacturing process to pattern a micromagnet on top of a CMOS device, to enable coherent manipulation of an electron spin through electric-dipole spin resonance [1493]. In September 2024, at the SiQEW conference in Switzerland, Quobly and its academic partners presented two coupled quantum dots realized with a GlobalFoundries 22FDX process [1494], which they later benchmarked with analyzing the effective mobility of six process using varying channel type, front-gate

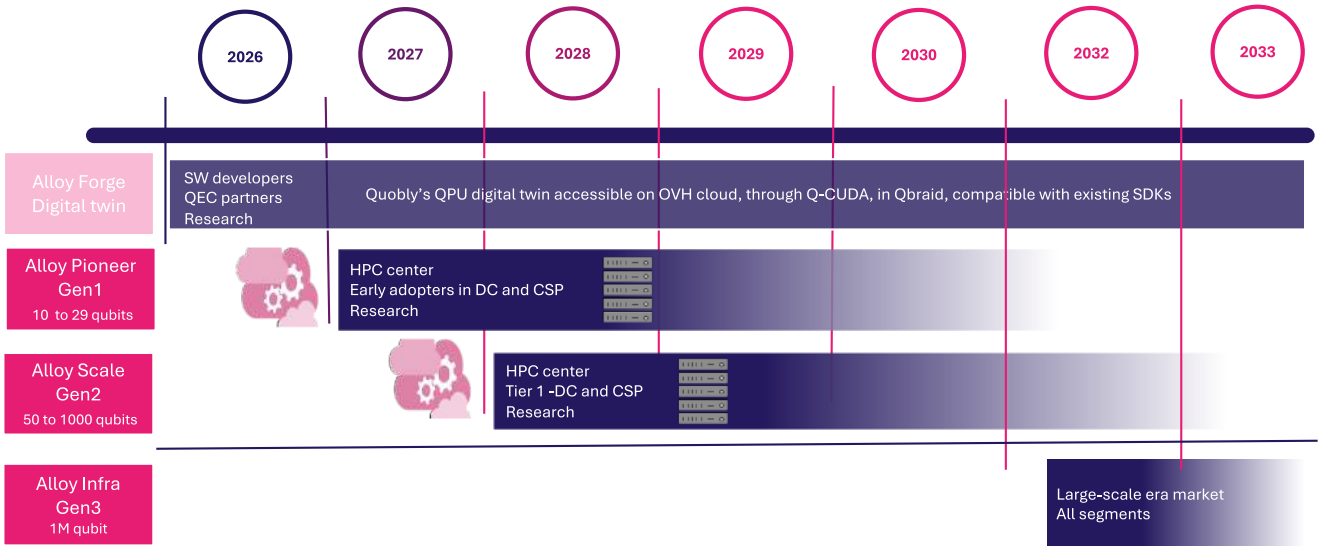

Figure 131: Quobly updated roadmap. The number of logical qubits and supported circuit size are not indicated. It will depend on the physical fidelities obtained with their qubits. Source: Quobly, June 2026.

stack and front-gate equivalent oxide thickness (EOT) [1495].

At ESSERC 2024, Quobly and its academic partners demonstrated cryogenic readout electronics integrated with quantum-dot test structures. A reported 99.9% fidelity in 2.2 μs at 4 K referred to charge-state discrimination using co-integrated single-electron transistors, not to end-to-end single-shot spin-qubit readout. They also demonstrated frequency-multiplexed readout of two SETs with 1 MHz spacing without one resonator per sensor [1496, 1497]. This is an important readout-integration result, but the spin-to-charge conversion fidelity and the charge-sensor fidelity should be kept conceptually separate. In 2025, the CEA/Quobly ecosystem also reported parallel characterization of many quantum devices with low cryogenic-electronics power [1498].

In July 2025, they published a paper on the viability of XZZX distance-3 surface code error correction, along with CEA-Leti and Eviden [1499]. It found that QEC converts non-Markovian physical noise into Markovian logical noise, leading to a quartic improvement in logical qubit coherence time. This resilience extends to spatially correlated noise and sparse architectures, demonstrating the surface code's robustness. However, exchange energy noise can dominate and saturate logical qubit performance even when physical coherence times improve, limiting overall gains. The paper also does not consider the impact of state preparation and measurement (SPAM) errors in its logical coherence time evaluations.

Manufacturing. In December 2024, Quobly announced a partnership with STMicroelectronics to adapt FDSOI fabrication lines for quantum devices. One isotopic-enrichment chain starts from enriched SiF_4, which Air Liquide can convert to SiH_4, silane, for epitaxial silicon growth. "Silicane" is not the name of SiH_4. Soitec and STMicroelectronics then participate in substrate and device processing. In 2026, Quobly reported receiving initial wafers from STMicroelectronics, but those manufacturing results had not yet translated into published randomized-benchmarking data for both single- and two-qubit gates. Quobly also works with Singapore's National Quantum Federated Foundry and with TNO's QITT facility for device characterization.

Roadmap. Quobly's 2026 roadmap has three main steps: Alloy Gen 1 with 10 to 29 physical qubits in 2027, Alloy Gen 2 with 50 to 1,000 physical qubits in 2028, and Alloy Gen 3 targeting one million physical qubits by 2032 (Figure 131). These are roadmap targets rather than demonstrated processor sizes.

Software. In March 2024, the company announced a partnership with Nanoacademic Technologies (Canada), for their use of QTCAD, a digital simulation and modeling tool supporting finite-element modeling of spin qubits. In March 2025, Quobly and BGene Genetics (France) started a collaboration to study the hardware and software needs to solve life sciences problems. In June 2025, they launched the emulator QLEO, a customized version of QPerfect's MIMIC, and hosted at OVHcloud. It supports up to 31 qubits in vector state mode. In July 2025, they also initiated a research partnership with Inria, focusing on the field of quantum error correction and middleware. In January 2026, Quobly also introduced SpinPulse, an emulation software supporting low-level spin pulse control simulation [1500].

Partners. In 2026, Quobly announced a partnership with Entropica Labs (Singapore) for the development of their FTQC software architecture, with Foxconn, for the development of a QPE toolbox for chemical simulations and other needs, with Orange Quantum Systems on chip testing, with TNO for device characterization, materials analysis and systems engineering, and with Absolut System on cryogenics with the QCube 100-Class

Figure 132: Quobly Alloy QPU form factor. Source: Quobly, 2026.

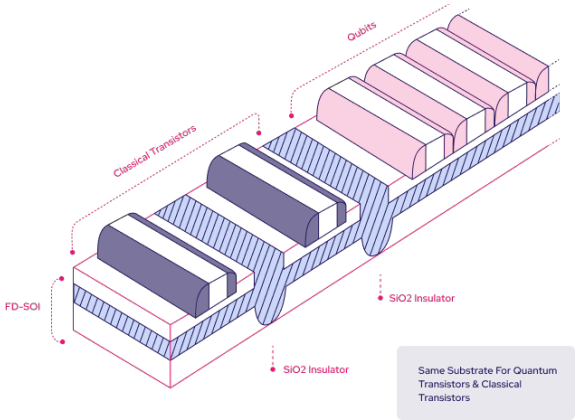

Figure 133: Quobly silicon spin qubit principle. Source: Quobly, 2025.

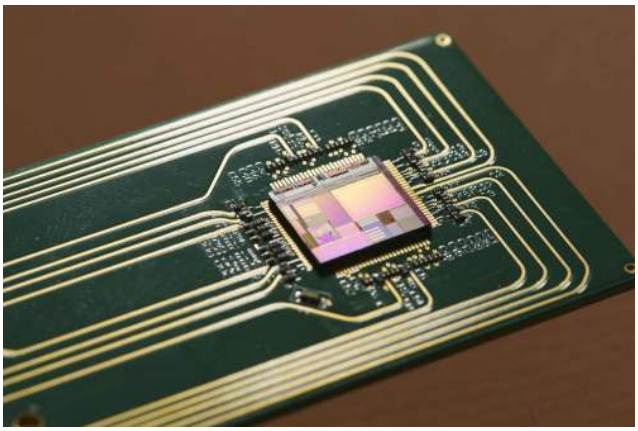

Figure 134: Quobly heterostructure test chip as of 2025. Source: Quobly, 2025.

Figure 135: Quobly cryo-prober from aFore-Bluefors that speeds up their characterization of a full chip wafer. Source: Quobly, 2025.

3 cryogenic systems, which provides 100 mW of cooling power at 500 mK.

Arque Systems

Germany, 2023

ARQUE is a spin-off of the JARA Institute for Quantum Information at RWTH Aachen University and Forschungszentrum Jülich, created by Markus Beckers (CEO), Hendrik Bluhm (CSO), Jan Klos (CTO) and colleagues. It develops silicon spin-qubit architectures centered on electron shuttling.

Their roadmap targets 2–4, 50, 200, 10,000 and eventually one million qubits using GaAs development devices and Si/SiGe spin qubits. They plan to use electron shuttling in the SpinBus architecture, related in spirit to the shuttling concepts shown in Figure 117, and target gate fidelities around 99.9% [97, 1501]. In August 2023, ARQUE announced that Infineon would manufacture qubit chips. Subsequent work has addressed long-distance spin shuttling and industrially compatible fabrication [1502, 1503]. They also use the Helmholtz Nano Facility at Jülich. In December 2024, the company formed a partnership with the Jülich Research Center to deliver a 5-qubit QPU and integrate it with the JUNIQ platform at the Jülich Supercomputing Centre (Jülich Unified Infrastructure for Quantum Computing). They later plan to scale to hundreds of qubits. JSC is used as a testbed for ARQUE development chips with low-level characterization, not up to the point of running a quantum circuit. Experimental chips support 34 and 51 quantum dots [1319, 1504–1507].

equal1.labs

Ireland/USA, 2017, $85M

equal1.labs was co-founded by Dirk Leipold, Mike Asker and Robert Bogdan Staszewski as a spin-out from University College Dublin (UCD). The company later expanded teams across Ireland, the Netherlands, Canada, Romania and California.

Technology. Equal1 develops a silicon quantum system-on-chip architecture combining spin qubits, cryogenic control, readout electronics and classical process-

ing. EDSR, electric-dipole spin resonance, is a spin-control mechanism, not the readout mechanism itself. Readout generally uses spin-to-charge conversion followed by a double-quantum-dot or charge-sensor measurement [1508]. Their architecture also explores on-chip classical processing and shuttling-based layouts for future error correction [1509, 1510].

Manufacturing. equal1 relies on TNO's cleanroom in the Netherlands to produce their SiGe qubit chip and their quantum system-on-chip (QSoC) processors, and on GlobalFoundries in Dresden 22 FDX process (22 nm FD-SOI) for the cryo-CMOS [1511]. Their design and test cycle lasts 6 months with GlobalFoundries and 4 months for TNO. The chip is integrated into a 4U Server including a compressor, a cryocooler, a vacuum pump, and a system motherboard. They indeed designed their own cryostat that does not require a dilution (Figure 137). It uses a classical MRI cooler, *ala* Cryomech, and another cooler to reach 3.3K with a cooling power of 200 mW with a very good power efficiency, needing only 1,5KW, which can use a regular single phase power supply on a wall plug.

In 2021, Equal1 described an Alice mk1 test system containing a large array of quantum-dot structures, sometimes marketed as a 422-qubit test chip. The demonstrated functionality was substantially below 422 coherently controlled qubits. It focused on single-electron loading, device characterization and simulation or development of one- and two-qubit operations [1512, 1513]. The Bell-1 system provided a clearer processor-level milestone with six physical qubits.

In May 2021, equal1 uncovered a prototype chip operating at 3.7K and including 10 million transistors handling qubits controls and readout with arbitrary waves generation (AWGs), all coupled to an external FPGA, as well as some classical cryogenic memory (Figure 136). As of December 2023, they had prototyped 7 generations of qubit chips. They target 98% two-qubit gate fidelities, 99% single qubit gate fidelity, 50 to 100 ns gate time and readout time of 10 μs with a target of 500 ns. Their current T_1 is 50 ms and T_2 is 4μs targeting 40 μs. They also plan to implement $R_x(\theta)$ and $R_z(\theta)$ single qubit gates for NISQ applications.

At the APS Global Summit in Anaheim in March 2025, equal1 presented its Bell-1, the first integrated SiGe spin qubit QPU. It contained a chip with 6 physical qubits (they call it now UnityQ) and a cryocooler reaching 300 mK, given the qubits could potentially operate up to 700 mK [1514]. All this in a single rack. The company is confident it can scale with a much larger number of qubits with this form factor (Figure 137). Introduced in 2026, the RacQ is the successor of the Bell-1, which fits in a datacenter rack and weighs 400 kg. It still has 6 physical qubits, with a system power consumption of 1,600 W at that prototype stage. Like all silicon qubit vendors, they plan to someday support a million physical qubits and thousands of logical qubits, although with no timeline.

Software. equal1 published some research work on NISQ quantum algorithms [1515, 1516]. In 2026, they announced some partnerships with Kvantify for scientific and industry application development, and with Q-CTRL for the integration of autonomous calibration software in their system. They also developed a finite-elements-based digital simulation tool for their SiGe and related micromagnets [1517].

Customers. Equal1's first customer is the ESA (European Space Agency), where a RacQ system was installed in July 2026 at their Space High Performance Compute Centre in Italy.

Groove Quantum

the Netherlands, 2024, €26M

Groove Quantum develops germanium hole-spin qubits in Ge/SiGe heterostructures.

Company. The startup was cofounded by Anne-Marije Zwerver (CEO), Nico Hendrickx (CTO, from Twente University) with Giordano Scappucci, Menno Veldhorst and Lieven Vandersypen as scientific advisors, the three main spin qubits researchers at Delft University, who previously collaborated with Intel.

Technology. Groove uses Ge/SiGe heterostructures with hole-spin qubits, building on research from TU Delft and QuTech. These devices exploit strong spin-orbit coupling for electrical control and avoid the silicon conduction-band valley-degeneracy problem, while still requiring demanding epitaxial and fabrication uniformity. The company combines linear and 2D arrays, modular architectures, resonator coupling and shuttling as possible scaling routes.

Scientific developments in Delft's team between 2024 to 2026 include a 4-qubit 2×4 germanium quantum dot array with full and controllable interactions between nearest-neighbor spins [1518], two-qubit gates between two mobile electron spins carried towards each other in separate traveling potential minima in the circuit, with tunable interaction using their spatial separation, with an average two-qubit gate fidelity of about 99% [1519] and with even better results published in August 2025 [1520], a 6-qubit chip with readout, shuttling and single-qubit gates optimization with readout fidelity, shuttling fidelity over a distance of 10μm, and >99.5% single-qubit gate fidelity [1521, 1522] even reaching 99.99% in some settings [1523], running two-qubit operations without changing the barrier gate voltage to improve qubit scaling [1524], implementing a three-qubit $C^2Ry(\pi)$ gate in 2025 with potentially achieving error rates of $\leq 10^{-4}$ in 80-100 ns [1525] (unitary matrix shown below), testing a three-dimensional quantum dots array in 2025 with four stacked 2×2 arrays, which due to strong coupling could be used for analog quantum simulations [1526], testing parity check measurements on quantum dots in 2026 [1527] and shuttling electrons over a distance of 200 nm, which will be useful for using non-local quantum error correction codes [1528], achieving single-qubit gate

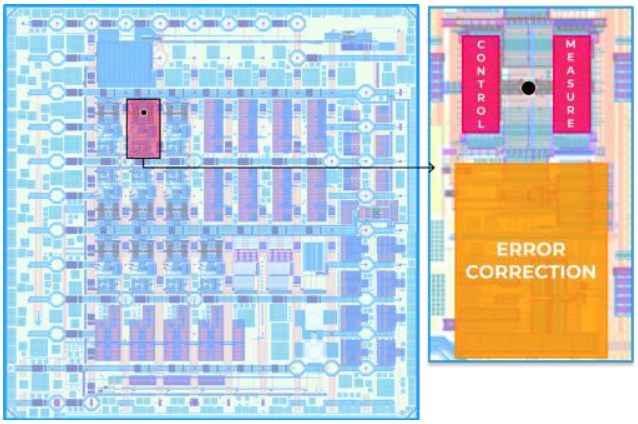

Figure 136: equal1 cryo-CMOS processor layout featuring signals control and quantum error correction support.

Figure 137: equal1 Bell-1 integrated QPU with its integrated cooler that reaches 300 mK for supporting their qubit chip operating temperature. Photo: Olivier Ezratty, May 2025 in Amsterdam at Q-Expo.

fidelities above 99.999% in 2026 [1364], and improving quantum dots characterization and calibration methods in 2025 [1529, 1530].

$$C^2\mathrm{Ry}(\pi) = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & -1 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \end{bmatrix}.$$

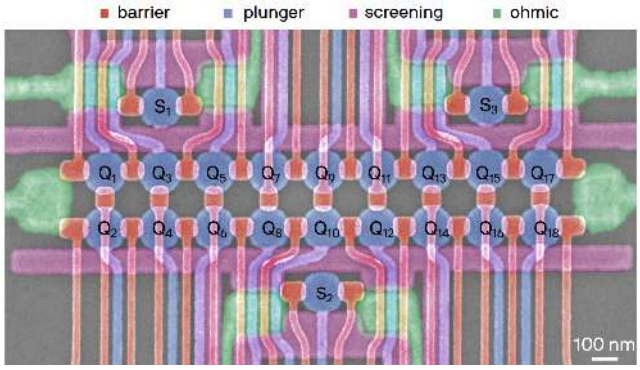

Figure 138: Groove Quantum experimental 18-qubit Ge/SiGe hole-spin array disclosed in 2026. All 18 qubits were operated simultaneously, while the reported multipartite GHZ state involved three qubits. Source: [1342].

Roadmap. In 2026, Groove demonstrated simultaneous initialization, control and readout across an 18-qubit germanium array, with average and median single-qubit gate fidelities of 99.8% and 99.9%, respectively [1342] (Figure 138). The experiment characterized nearest-neighbor exchange couplings and generated a three-qubit GHZ state. These were not 18 entangled qubits. Groove has announced a next scaling target around 100 qubits.

Intel

USA, 1968

Intel is a key contender in the race for silicon qubits. They started working on superconducting qubits, but it seems it was a secondary route for them. Their quantum work is managed under the direction of **Anne Matsuura** [1531, 1532] and **James Clarke** for hardware.

Early chips. Intel began fabricating silicon spin-qubit test devices in the late 2010s. A 2018 Intel announcement described qubit structures about 50 nm across and stated that roughly 1,500 such qubits could fit across the diameter of a human hair. It did not report a functioning 1,500-qubit processor. The 2018 chip was a small test device fabricated in Intel's D1D fab to study manufacturability and single-electron quantum-dot structures.

In 2022, Intel did show again some interesting data related to their qubits manufacturing capacity, producing chips with 3 to 55 quantum dots on 300 mm wafers and a >95% production yield, using 193 nm Deep UV immersion photolithography instead of electron beam lithography [158].

These SiGe qubits had a relaxation time of >1s (T_1), coherence times of >3 ms (T_2) and single qubit gates of >99% (and no published data for two-qubit gates…). These qubits had to be characterized by the DoE Argonne lab in Chicago in its Q-NEXT research center [1533] (Figure 140).

Cryo-prober. As part of their efforts in manufacturing, Intel is using, like CEA-Leti, a cryo-wafer prober provided by Afore and Bluefors, that enables testing entire wafers at 1.6K, significantly accelerating the testing and characterization process (Figure 141 and Figure 142) [1309].

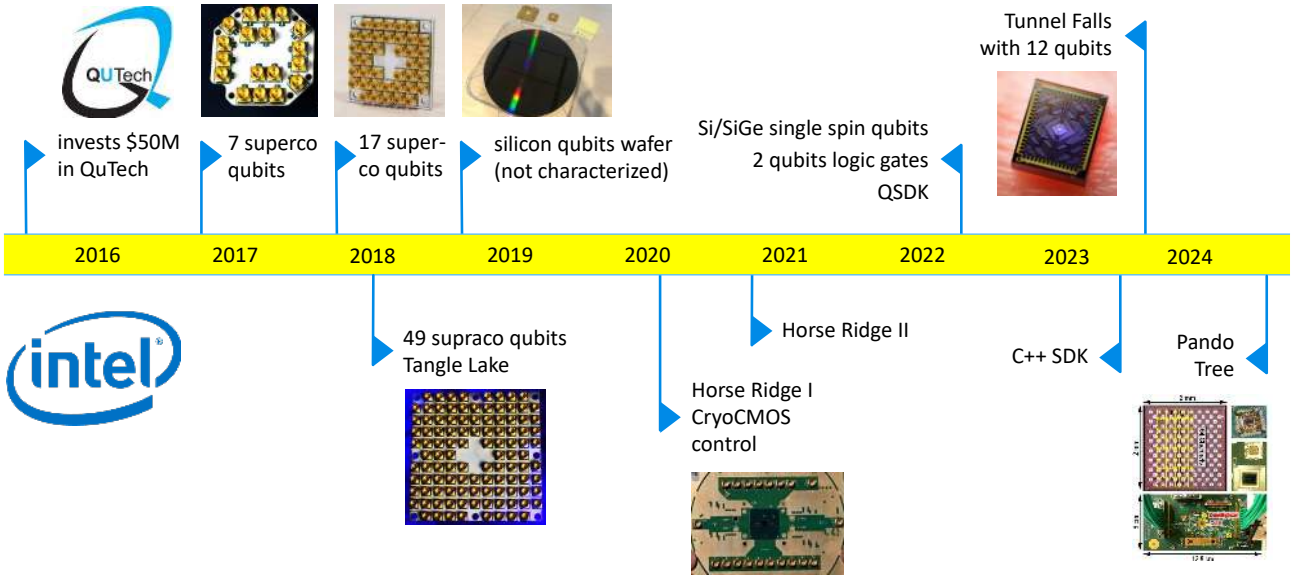

Figure 139: Intel quantum computing timeline. Olivier Ezratty, 2022-2024.

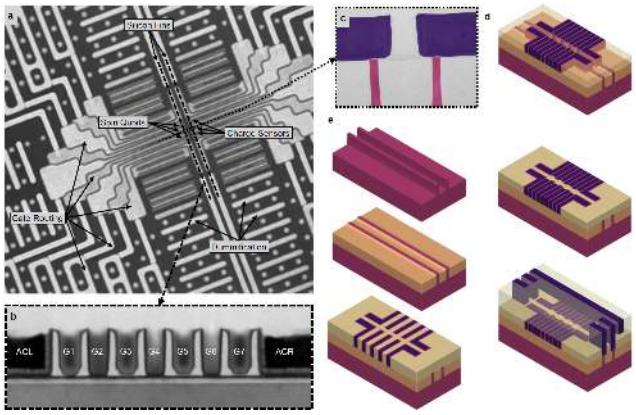

Figure 140: Intel SiGe quantum dots circuit implementation and process quality. Source: [158].

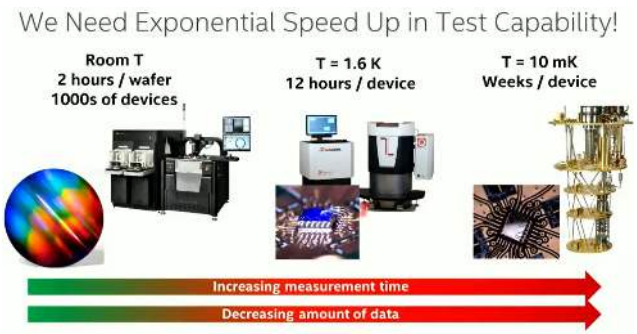

Figure 141: How Intel is saving time with a Bluefors/a-Fore cryo-prober. Source: Intel.

QuTech and Intel work together on these qubits. QuTech got a $50M investment from Intel in 2015 to explore it. Intel announced in 2018 that it had succeeded in controlling a two-qubit SiMOS processor with single and two quantum gates running Deutsch-Jozsa and Grover algorithms on a very small scale. These silicon-germanium qubits manufactured by Intel were tested by the Vandersypen Laboratory at the University of Delft, part of QuTech [1534].

HorseRidge and Pando Tree. At the beginning of 2020, Intel announced that it had developed with QuTech the HorseRidge cryo-CMOS chip operating at 4K. It generates the microwaves used to drive both superconducting and silicon qubits. A second version was announced in 2021. We cover it in the section dedicated to cryo-CMOS electronics. Then, in 2024, Intel introduced Pando Tree, a cryogenic chip for demultiplexing control signals coming from its Horse Ridge II pulses generator operating at 4K.

Tunnel Falls. In June 2023, Intel released Tunnel Falls, a 12-dot silicon spin-qubit research chip for academic and federal laboratories [1535]. It was fabricated on 300 mm wafers using EUV lithography and showed about 95% wafer yield. The often-quoted roughly 50 nm dimension refers to an individual qubit or gate-feature scale, not to the physical die size of the packaged chip. Intel reported 24,000 quantum-dot test chips per wafer and 99.8% yield for tuning the 12-dot structures to the single-electron regime. Depending on tuning, the 12 dots can form four to twelve qubits [1536]. Intel and partners have continued to characterize later generations [1318, 1537, 1538] (Figure 144).

Intel made several presentations at the 2024 Minneapolis APS March meeting including one that disclosed two-qubit gate fidelities of 92% [1539].

Later in 2025, Intel and QuTech tested a six-qubit chip and executed circuits using the full register. Performance was limited by dephasing of idling qubits and

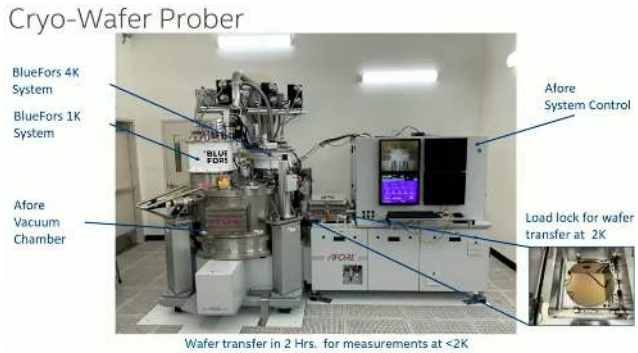

Figure 142: The aFore-BlueFors cryo-prober.

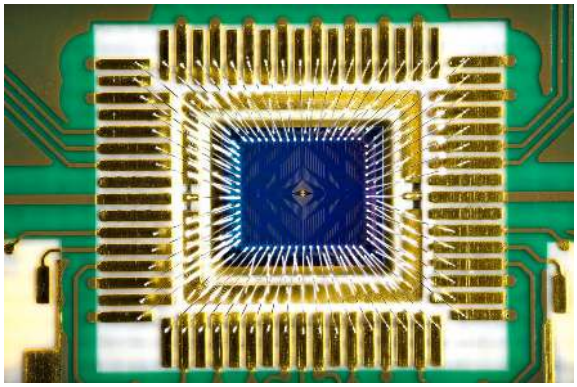

Figure 143: Intel Tunnel Falls 12-qubit chip. Source: Intel. 2023.

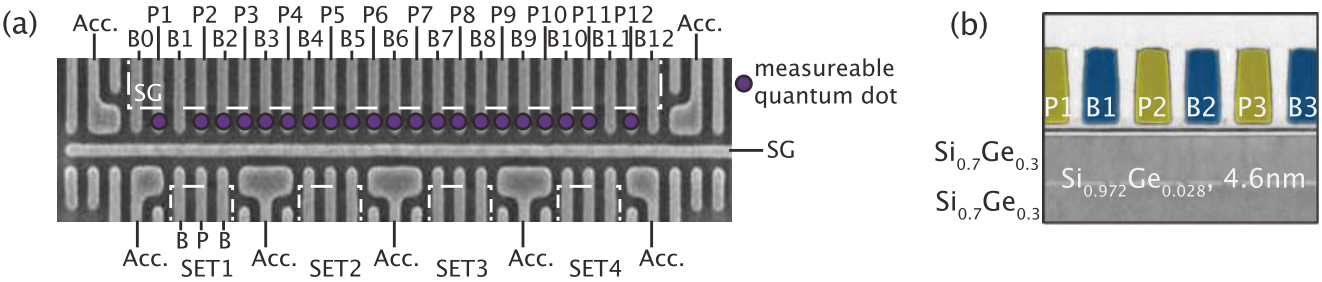

Figure 144: Intel Tunnel Falls 12-qubit chip 2025 version as tested by Q-NEXT at the DoE Argonne Labs. Source: [1318].

significant state-preparation-and-measurement errors [574, 1540, 1541].

In May 2023, Intel and RIKEN announced a research partnership covering classical supercomputing and silicon qubit quantum computing. But it is not clear what they will do respectively in this partnership. In 2025, another partnership in Japan was announced, with AIST's G-QuAT research center.

SQC

Australia, 2017, $173.4M

SQC (Silicon Quantum Computing) is a spin-out from UNSW and CQC2T launched by Michelle Simmons.

Company. In 2017, their goals were to reach 10 qubits by 2022 [1542] and 100 physical qubits by 2028. That was before logical qubits and quantum error correction were becoming mainstream in vendor roadmaps! Mid-2021, Andrea Morello and Andrew S. Dzurak quit SQC where they had been involved from the beginning. They preferred to focus on SiMOS qubits instead of donor spin qubits, SQC's technology. It led to the creation of Diraq. As a result, SQC sold in May 2022 its patent portfolio and special equipment related to SiMOS to SiMOS Newco, a company created in December 2021, and related to Diraq, that was created a month later [1543].

Technology. SQC uses the spin donor technique, trapping phosphorus atoms on a ^{28}Si substrate [1544]. Their qubit is made by controlling the association of the phosphorus atom nucleus spin and one electron spin from the phosphorus valence shell, not bound to the silicon atoms. Phosphorus (group V) happens to be on the left of silicon (group IV) in the Mendeleev table of periodic elements. Relative to silicon, phosphorus contributes one additional valence electron, and in silicon that electron can be weakly bound to the positively charged donor core.

Phosphorus has an extra valence electron bound to the positively charged donor core by a screened Coulomb potential. In silicon the dielectric constant is about 11.7 and the effective electron mass is roughly $0.2m_e$, leading to a donor binding energy around 45.6 meV and an effective Bohr radius of order 1.8 nm [1545]. The 45.6 meV binding energy corresponds to about 530 K on the k_BT scale. By contrast, $k_BT \approx 0.86$ μeV at 10 mK and 8.6 μeV at 100 mK. For an electron with $g \approx 2$ at 1 T, the Zeeman splitting is about 116 μeV. Thus spin initialization is set by the Zeeman-to-thermal-energy ratio, not by the much larger donor binding energy.

The qubit is the spin, either from the ^{31}P nuclear spin, the donor electron spin, or both together. In Bruce Kane's 1998 proposal, phosphorus donors are placed in an array about 20 nm apart and roughly 20 nm below the surface, with metal A gates above each donor and J gates between adjacent donors. Applying a voltage to the A gate creates a local electric field that pulls the electron wavefunction away from the ^{31}P atom nucleus and toward the surface. This changes the overlap of the

electron cloud with the nucleus. It tunes the contact hyperfine interaction and shifts that specific nuclear spin in or out of resonance with a globally applied RF field. The J gate implements two-qubit gates by adjusting the overlap between neighboring donor electrons and the exchange coupling that mediates a controllable qubit-qubit interaction [1546]. The benefit is that in an isotopically purified ^{28}Si host with zero nuclear spin, so the ^{31}P nuclear and electron spins are isolated from magnetic noise, giving them long coherence times.

Manufacturing. These spins are manufactured on a ^{28}Si wafer covered with a single layer of hydrogen atoms, which acts as a resist. An STM (scanning tunneling microscope) tip removes hydrogen atoms in selected locations in the hydrogen mask. Six silicon sites are thus processed. The surface is dosed with phosphine gas, PH_3, which sticks to the exposed bare silicon. The wafer is heated to about 350°C to dissociate the phosphine and incorporate the phosphorus atom in the silicon lattice. After this, a low-temperature epitaxial silicon layer encapsulates the donors. The caveat is the manufacturing yield and positioning of these phosphorus atoms. They improved their manufacturing capabilities with precisely positioned phosphorus donor dots in silicon [1547, 1548]. They announced working with Skywater in November 2025. We'll see how it turns out now that Skywater belongs to IonQ.

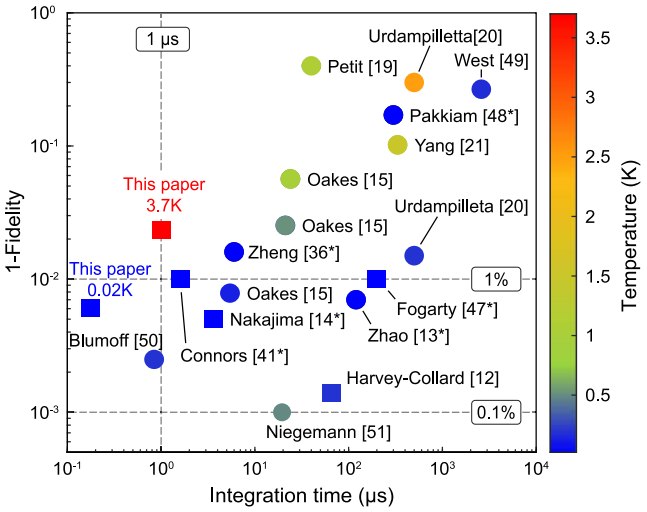

Figure 145: The record high-temperature and high-speed spin readout obtained by SQC in 2025. Source: [132].

Fidelities and small processors. In 2019 and 2020, SQC reported very high single-spin control fidelities in donor devices and sub-nanosecond exchange dynamics in specialized structures [1328, 1549]. In 2022, however, the Nature paper often described as about a "quantum circuit" was not a ten-gate-model-qubit processor. It used a linear array of ten donor-based quantum dots as an analogue quantum simulator of the interacting Su–Schrieffer–Heeger model, with transport spectroscopy as the principal observable [1550]. In 2024, SQC reported exchange coupling between donor structures about 17.5 nm apart [1551]. Separate work demonstrated about 99% readout fidelity in 2022 [1552] and, in 2025, 99.44% single-shot electron-spin readout in 175 ns at millikelvin temperature and microsecond-scale readout above 3.5 K [132]. Numerical device modeling has also projected two-qubit CNOT fidelities approaching 99.98% under optimized conditions [1553].

Analog simulation. In February 2026, SQC and UNSW published a Nature experiment using an array of 15,000 atom-based quantum dots arranged on a 100×150 lattice [177]. These 15,000 sites were not 15,000 gate-model qubits. The device is an analogue quantum simulator of interacting-electron physics, including Mott-Hubbard and disorder-driven metal-insulator behavior. Much of the Hamiltonian is engineered lithographically through dot geometry and spacing, while experimental parameters such as electrochemical potential, temperature and magnetic field are dynamically tunable. Readout is collective transport and spectroscopy rather than individual single-shot measurement of 15,000 qubits. The result is a major scale-up of atomically engineered quantum-dot analog simulation.

Processors. In 2024, they implemented a Grover search using 4 qubits, 3 phosphorus atoms and one electron spin. Their two-qubit gate fidelity was 99.32% [123]. We are of course far from useful the NISQ and FTQC realm. In June 2025, they demonstrated an 11-qubit chip made with two multi-nuclear spin registers (with respectively 5 and 4 phosphorus nuclei hooked to an electron spin) linked together via an electron exchange interaction, a unique feat that NV center QPU vendors are also trying to create [124]. Single qubit gate fidelity ranged from 99.5% to 99.99% while the Bell-state fidelity reported in [124] reached 99.5% and a two-qubit CZ gate also reached 99.9% fidelity. In August 2026, they published a preprint describing how they could generate T and CCZ states efficiently, by combining color codes and bilayer surface codes, with what they called the "Magic Scroll" [1554].

Customers. In August 2025, SQC announced a contract from the Australian Defence Ministry for a QPU named Watermelon to run quantum machine learning applications. This project was awarded to SQC, CSIRO, Macquarie University, the University of Melbourne, the Royal Melbourne Institute of Technology and the University of Technology Sydney as part of the Advanced Strategic Capabilities Accelerator's (ASCA) Emerging and Disruptive Technologies (EDT) program and with A$6 million in funding over three years [1555]. SQC declared that "*Watermelon works exceptionally well when applied to sparse, fuzzy datasets. Delivering intelligence and spotting patterns beyond classical AI and ML approaches*" without giving any indications of the number and quality of qubits in Watermelon. We can guess it is not in any quantum advantage regime and cannot run any machine learning application that couldn't be run for cheaper on a regular PC. CSIRO is tasked with developing QML algorithms to "*detect and mitigate adversarial and spoofing attacks*".

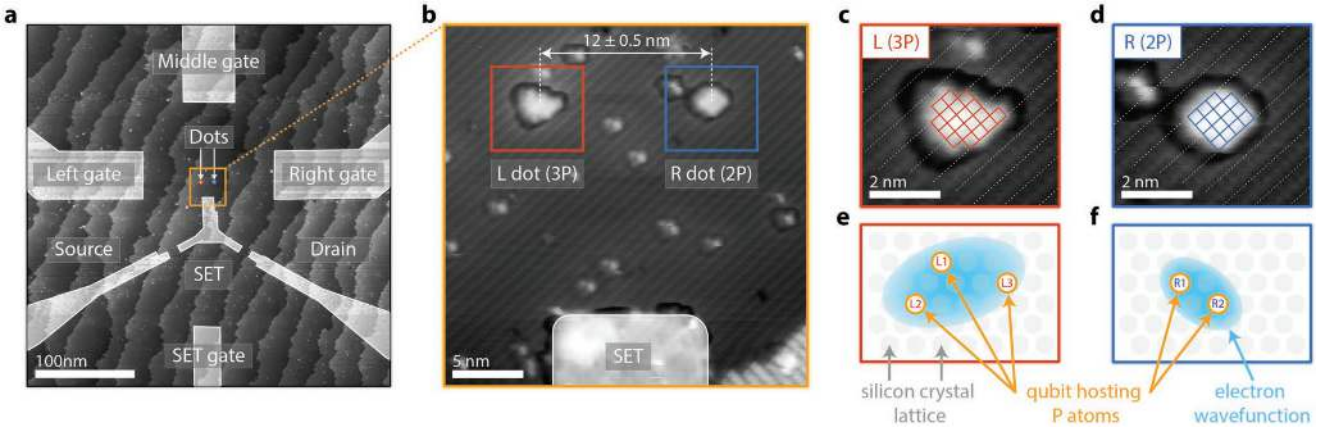

Figure 146: The atomic dots in SQC chips are precisely positioned. They contain several atoms. Source: [1547].

Archer Materials

Australia, 2017, N/A

Archer Materials develops carbon-based quantum-device and sensing technologies intended to operate at substantially higher temperatures than conventional semiconductor spin qubits [1556]. As of September 2026, the company still described a carbon-based qubit demonstration as a roadmap milestone. Its published and announced device work should therefore not be presented as an already operational room-temperature quantum processor.

The company was cofounded by Mohammad Choucair who invented their ^{12}CQ chip design and by Martin Fuechsle who contributed to the development of the single electron transistor and worked at UNSW with Michelle Simmons. Like with C12, 12 is not the number of qubits. It is the mass number of the spin-zero carbon isotope used in these nanospheres, which trap an electron and its spin. Electrons are delocalized around the nanosphere and not sitting inside it, contrary to the C12 Quantum Electronics electrons that are stored within nanotubes.

In April 2021, Archer Materials announced it would sell off all its mineral traditional business to iTech Minerals, to focus on quantum technologies.

Archer fabricated early carbon-nanosphere and carbon-film test structures and demonstrated electronic transport and ESR-related detection at room temperature. These are necessary ingredients for a spin qubit but do not by themselves establish coherent initialization, universal gate control, quantified T_1/T_2, high-fidelity readout and entangling operations in a processor. Earlier material studies reported room-temperature spin lifetimes of order 100 ns, and Archer subsequently developed SET and resonator structures to improve readout. The company continued to describe a working carbon-based qubit demonstration as a future milestone through 2026.

In February 2022, through a collaboration with EPFL, they demonstrated the use of a single-chip integrated electron spin resonance (ESR, seemingly at 9.4 GHz according to their patent) detector based on high electron mobility transistor (HEMT) to detect and characterize their qubit at room temperature [1557].

The road ahead is still quite long for them. Based on this 2022 milestone, the company CEO forecasted "*mobile quantum computing*" use-cases, quite an overselling statement.

In December 2020, Archer launched a partnership with **Max Kelsen**, another Australian company, specialized in QML software development. Max Kelsen and Archer will develop QML algorithms based on Qiskit, eyeing a future execution on Archer's processor. They also announced that GlobalFoundries would become the manufacturer of their ^{12}Q qubit chip. The company is also developing graphene-based biosensor chip aka "lab on chip". This is a nearer-term and more credible product proposal than their room temperature spin qubits. Archer Materials created in September 2024 two proof-of-concept chips implementing spin detection capabilities for its ^{12}CQ quantum chip.

One 2024 proof-of-concept circuit contained eight superconducting resonators intended for selective electron-spin detection at 4 K [1558]. This demonstrated a readout-device component, not an eight-qubit quantum processor.

In June 2023, the company announced that their chip was operating not only at room temperature but also in the air, without requiring vacuum conditions. In 2024, the company also prototyped a graphene field effect transistor ("gFET") chip to be used for some medical quantum sensing application, signaling a potential pivot for the startup [1559, 1560].

So, we have nanotubes and nanospheres. How about carbon nanoribbon? It is investigated at the research stage but there is no related startup on the radar [1561]!

C12 Quantum Electronics

France, 2020, €38M

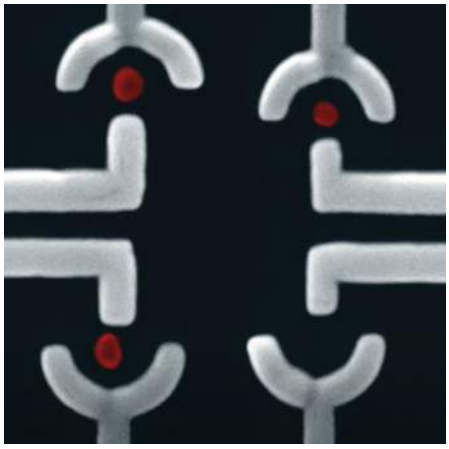

Figure 147: Archer qubits. Source: Archer.

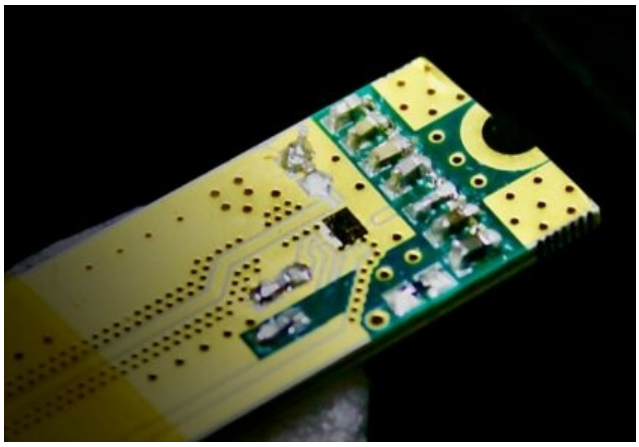

Figure 148: Archer-EPFL spin-resonance circuit. Source: Archer.

C12 Quantum Electronics is a carbon-nanotube spin-qubit startup.

Company. It was launched by Matthieu Desjardins (CSO) and his twin brother Pierre (CEO). It is a project originating from the LPENS at ENS Paris and 15 years of research from Takis Kontos and Audrey Cottet, with contributions from Jérémie Viennot at Institut Néel Grenoble. The company had a team of 85 as of September 2026.

Technology. Their goal is to use carbon nanotubes to trap electrons used in electron spin qubits and build the surrounding control circuitry on silicon substrate (Figure 149). This technology can improve qubit isolation and coherence time, while keeping a strong coupling for fast qubit manipulation. The qubits can be set to different modes by baseband electrode potentials for gates, readout, or an isolated memory state. Qubit readout uses a coupling of the qubit with a resonator. The connection between two qubits is based on microwave cavities, exploiting cQED (Cavity Quantum Electrodynamics).

Challenges include materials control, reproducible nanotube placement, scalable manufacturing, control electronics, connectivity and error correction. C12's roadmap targets two-qubit gate fidelities above 99.9%, T_2^* coherence times above 1 ms and connectivity zones containing up to 128 qubits. These are targets, not current measured processor specifications. The proposed ability to switch qubits between more isolated memory configurations and cavity-coupled interaction configurations could reduce residual coupling, but its large-scale performance remains to be demonstrated.

In 2025, C12 and collaborators reported coherence of about 1.3 μs in a carbon-nanotube double-quantum-dot device coupled to a microwave cavity [1303] (Figure 149). This is a good improvement over earlier nanosecond-scale results, but the implication for computation depends on the achievable gate time, gate fidelity and error model, so the coherence time alone is insufficient to declare the device unusable. C12 aims to extend coherence toward the millisecond regime through materials and process improvements. In July 2026, the company published a simulated proposal for an iSWAP-like qubit-boson gate [1562].

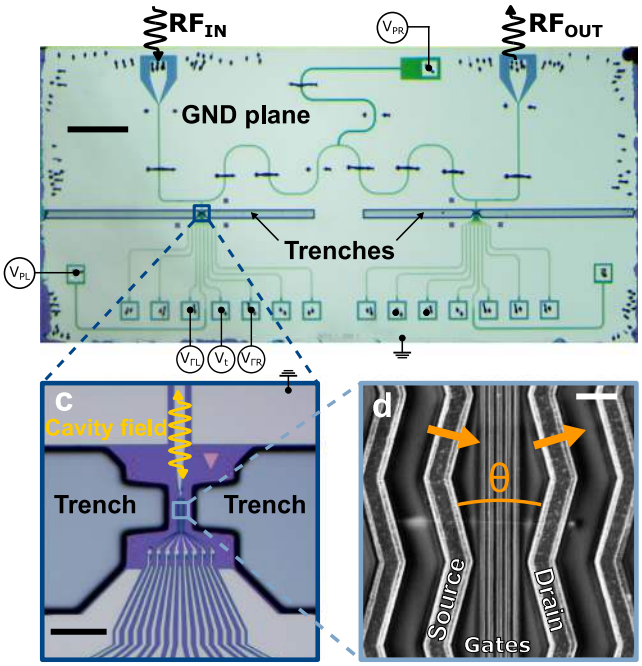

Figure 149: C12's nanotube circuit layout showing how voltage is controlled around the quantum dot. Source: [1303]

Manufacturing. The nanotubes are mechanically integrated into the circuit at the end of the manufacturing process [1329]. The carbon nanotubes are grown by C12 using a CVD process (chemical vapor deposition). In March 2022, C12 announced it was starting a manufacturing partnership with CEA-Leti. These will provide their quantum chips on silicon on 200 mm wafers. These will contain the superconducting electronics controlling the state of their carbon nanotubes that will be positioned on the chips. In October 2023, the company

opened its new headquarters in Paris with a small fab handling most processes from building, characterizing and pre-selecting nanotubes with the right chirality, and their underlying silicon handling chip, plus two cryostats for testing (Figure 150). As of December 2025, they had tested a chip supporting 18 carbon nanotubes, but with no gate fidelities.

Figure 150: C12's testing room with two cryostats, a typical setup for many quantum computing startups nowadays. They have two other floors for their carbon nanotube and related circuits manufacturing tooling. Photo: Olivier Ezratty, 2023.

Roadmap. C12 published its first full roadmap in April 2026 [1330] (Figure 152). One interesting characteristic is the goal to support 100K physical qubits by 2033 with a power of only 50 kW. It is probably not fully burdened, particularly at the stage of quantum error correction support. They work with QC Design Plaquette for the implementation of their FTQC architecture as well as with Classiq for the compiler.

Software. On the software engineering side, Eviden works with C12 to develop its quantum compiler, to create digital simulation models of its qubits and for co-designing quantum gates. It was announced as Callisto on OVHcloud in June 2023, which they tested at small scale in 2025 to implement a quantum walk algorithm [1563]. They are also teaming up with Air Liquide on a case study for the simulation of Zr precursor of ZrO_2 (zirconium amino cyclopentadienyl complex). It led to some work done published in 2025 and tested with Quantinuum QPUs [1564].

EeroQ

USA, 2016, $7.5M

EeroQ is developing a quantum-computing architecture based on electrons trapped above superfluid helium, with the electron spin intended as the qubit degree of freedom [1565].

Company. The startup was launched by Johannes Pollanen from the University of Michigan (CSO), Dave Ferguson, Nick Farina (CEO) and Faye Wattleton (EVP) [1333]. In May 2021, Steve Lyon, a Princeton University Professor, joined them as their CTO. The company got some undisclosed NSF and private funding from VCapital in 2022. In 2025, SEALSQ made an undisclosed investment in the startup.

Technology. Proposals for quantum computing with electrons above liquid helium date to Platzman and Dykman and related work around 1999–2000 [1566]. A 2006 spin-based proposal by S. A. Lyon estimated electron-spin coherence times exceeding 100 s because of the exceptionally weak spin-orbit and nuclear-spin environment [1307]. This was a theoretical decoherence estimate, not an experimental measurement of T_1 or T_2 in an operational qubit. The same proposal described electron shuttling and magnetic dipole-dipole two-qubit interactions.

EeroQ's roadmap targets spin coherence above 10 s, high connectivity, mobile electrons and two-qubit gate fidelities around 99.9%, with eventual scaling to 10,000 qubits on a monolithic chip. As of September 2026, these are engineering targets. They have not yet been demonstrated together in a functioning multi-qubit spin processor.

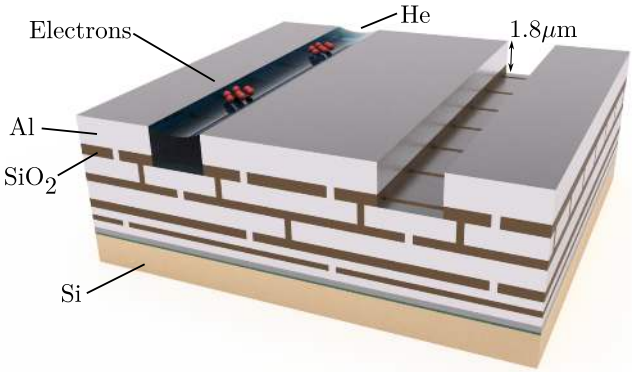

Figure 153: A cross-section of the EeroQ Wonder Lake chip. Electrons and superfluid helium occupy channels between patterned aluminum layers. The channel walls contain silicon oxide and aluminum, while CCD-style control electrodes route and shuttle electrons. This structure is infrastructure for future spin-qubit operation rather than a demonstrated 2,432-qubit processor. Source: [1567].

The papers they published since then relate to low-level physics experiments [1570], to qubit drive with high-impedance titanium nitride resonators [1571], on the improvement of superconducting resonators [1572], on the spatial control and detection of single electrons above the surface of liquid helium at >1K [1573] and on coupling a microwave photon to an electron on the helium surface [1331].

Manufacturing. EeroQ's Wonder Lake CMOS chip is a scaling and electron-transport platform described by the company as a "2,432 future qubit system" using only about 30 external control lines [1574]. It did not contain 2,432 functioning spin qubits. EeroQ reported trapping, measuring and shuttling small packets of electrons in these structures, with a two-spin entangling gate still identified as a next step. A 2025 version of Wonder Lake was fabricated by SkyWater [1567] (Figure 153 and Figure 154).

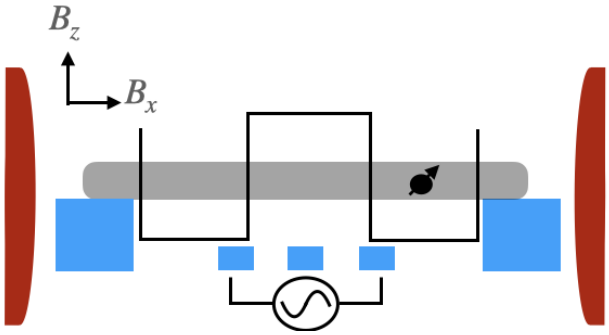

Figure 151: C12's spin qubit where an electron is hosted in a carbon nanotube (grey tube), suspended over five electrodes (blue squares) generating a double quantum dot (black squared well) trapping the particle (black arrowed dot), and immersed in an asymmetric magnetic field. Single qubit gates are realized by changing the dot's voltage (black wave) and two-qubit gates by embedding two qubits within the same microwave cavity (red resonator plates). Source: [1563].

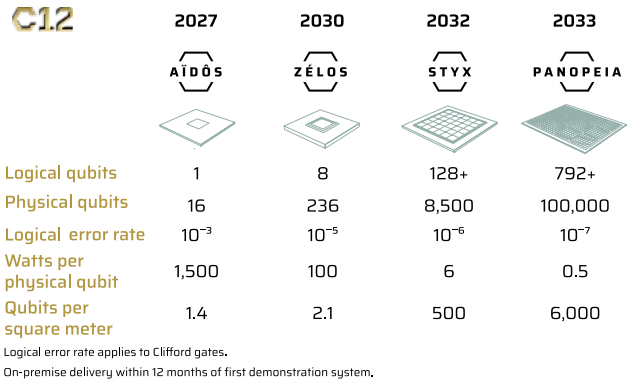

Figure 152: C12 roadmap published in April 2026. The plan is ambitious in its ramp-up of physical-qubit count, leading to a target of 792 logical qubits in 2033 and circuit size of 10 million in breadth × depth. These are company roadmap targets, not experimentally demonstrated resources. Source: [1330].

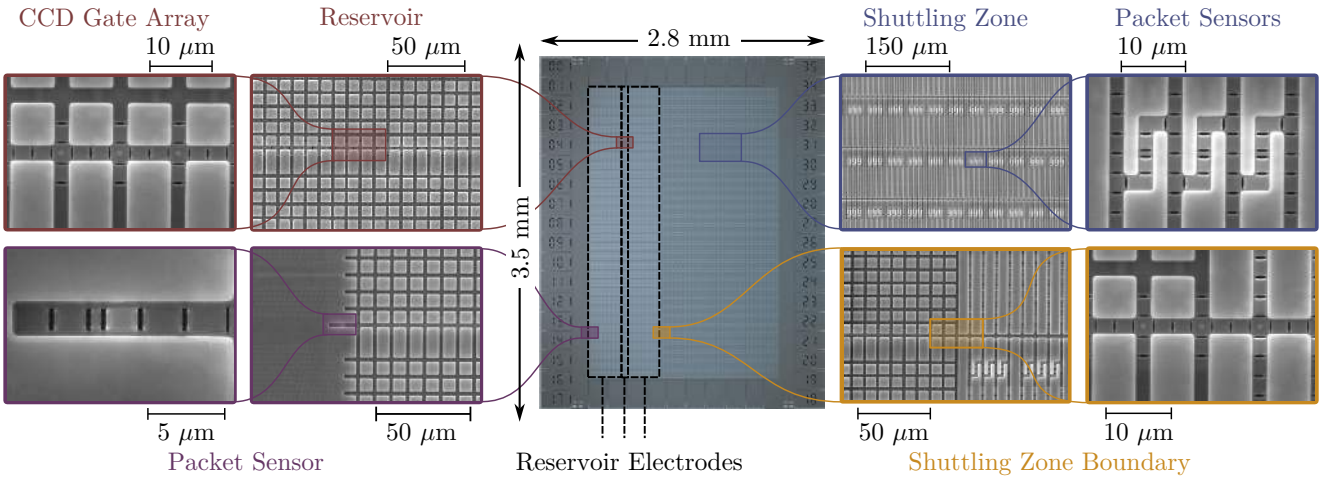

Figure 154: The 2025 Wonder Lake chip manufactured by SkyWater uses a 130 nm process and measures about 2.8×3.5 mm. It is designed to demonstrate electron shuttling between storage and detection zones across 128 transport microchannels. This is a transport/control milestone and not about supporting 128 or 2,432 operational spin qubits. Source: [1567].

Quantum sensing. EeroQ is also exploring with CERN the use of its technology to create quantum sensors for elementary particle detection, using entangled array of electrons. They could detect energy transfers far below the keV to detect light and ultra-light dark matter, hypothetical milli-charged particles that would carry an electric charge smaller than the elementary charge e, or hidden-sector bosons such as dark photons, axions or axion-like particles [1575].

Key spin qubit quantum computing reviews

Here is a selection of semiconductor spin qubits scientific reviews to dig into the concepts presented in this section:

Spins in few-electron quantum dots by Hanson *et al.*, October 2007 (49 pages): the founding review from the GaAs era, single-electron charging, spin relaxation and dephasing, Pauli blockade readout and exchange control [1321].

Semiconductor spin qubits by Burkard *et al.*, June 2023 (about 60 pages): the reference review covering the four spin qubit flavors, single spin, donor, singlet-triplet and exchange-only, plus valleys, spin-orbit coupling, exchange physics, noise filter functions and spin-photon hybridization [1350].

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This **Quantum dots spins qubits** subsection contains 320 bibliographical references and notes containing at least 4,126 pages.

1.5 NV centers qubits

An NV center is a point defect in diamond formed by a substitutional nitrogen atom adjacent to a missing carbon atom, the vacancy. In the negatively charged NV^- state, the electronic ground state has spin $S = 1$ and can itself encode a qubit. Nearby ^{14}N or ^{15}N and ^{13}C nuclear spins can provide additional, longer-lived qubits, forming a small register around one NV electron-spin ancilla [1576].

1.5.1 History

Defects in diamonds have been studied since 1930 with the examination of infrared absorption. This made it possible to distinguish two categories of diamonds: type I with an absorption band of 8 μm in the infrared and type II without this band. The defects explain the color of diamond gems.

It was not until 1959 that these impurities were found to be related to the presence of nitrogen, at 7.8 μm and that nitrogen atoms were well isolated in the diamond crystal. In 1975, it was discovered that some heat treatment could control the diffusion of nitrogen atoms in the diamond. These nitrogen centers explain the diamond color. It has four types: one nitrogen atom isolated in a gap, two nitrogen atoms, three nitrogen atoms surrounding a gap and four nitrogen atoms.

It is the first type that is interesting for both quantum computing and quantum sensing. We can visualize these defects with a confocal microscope (having a very shallow depth of field) by illuminating them with a green laser beam that will generate some red light.

These NV-center diamonds are slightly pink. These properties make it possible to generate single-photon sources thanks to the isolation of an NV center. Nitrogen-rich artificial diamonds are used to manufacture these NV centers. Gaps are generated with irradiation.

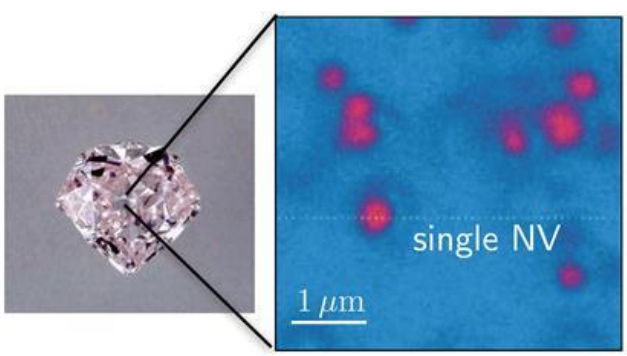

Figure 155: How NV center cavities look in real diamonds. Source: [1577].

Vacuum annealing at about 800°C-900°C makes irradiation-created vacancies mobile, allowing some of them to diffuse next to substitutional nitrogen atoms and form NV centers [1578, 1579] (Figure 156). The relevant magnetic degree of freedom of NV^- is the spin-triplet electronic ground state localized around the defect.

Diamonds containing NV centers can also be produced with vacuum deposition of hydrogen and methane (CVD, for Chemical Vapor Deposition) to create a perfect diamond crystal structure [1580]. It can then use ion implantation with nitrogen ion beams [1581] (Figure 155). NV centers implantation could potentially be done with DNA-based patterning according to a proposal from UCSB made in 2025 [1582].

The carbon structure surrounding a NV center protects the cavity area. The state of the gap is unstable and quantum. It is controlled by lasers and microwaves. The qubit state readout is performed using a laser excitation to measure fluorescent brightness.

1.5.2 Science

The NV^- center contains six electrons associated with the defect. Its electronic ground state is the spin-triplet $^3A_2$ manifold with total spin $S = 1$ and spin projections $m_s = 0, +1, -1$ [1576]. The electron spin can be coherently controlled with microwave and static magnetic fields and can be hyperfine-coupled to the nitrogen nuclear spin and to nearby ^{13}C nuclear spins. Approximately 1.1% of natural carbon is the spin-1/2 isotope ^{13}C, while the dominant ^{12}C isotope has zero nuclear spin.

Commonly used NV centers are called NV^- because of the addition of an external electron into the cavity. The cavity has 6 electrons, three from the surrounding carbons, two from the nitrogen valence shell and one captured from the bulk.

There are other variations like vacancies without this captured electron (NV^0), which are less optically active than the NV- or the positively charged NV^+ and NV^{2+} centers that are optically inactive. For these reasons, they are not commonly used.

Figure 160 contains a diagram that describes what a NV center can look like in practice considering that there are many different implementations, knowing that NV centers are used not only for computing but, in a dominant manner, in quantum sensing as well as for the creation of individual photon sources used in quantum communications and cryptography. NV centers can be integrated into circuits fabricated on an SOI silicon wafer with a layer of SiO_2 insulator. It is then covered with a matrix Fresnel lens, used to focus a control and readout laser [1583]. It is frequently associated with other photonics components when the NV center spins are used to generate photons for quantum communications [1584].

Figure 157 explains how these rather complex qubits operate with the various energy levels and transitions of the cavity and its free electrons using microwaves and green photons. The vertical arrows represent useful energy transitions [1585]. This is applicable to the NV^- species. The vacancy qubit state is controlled with 2.87

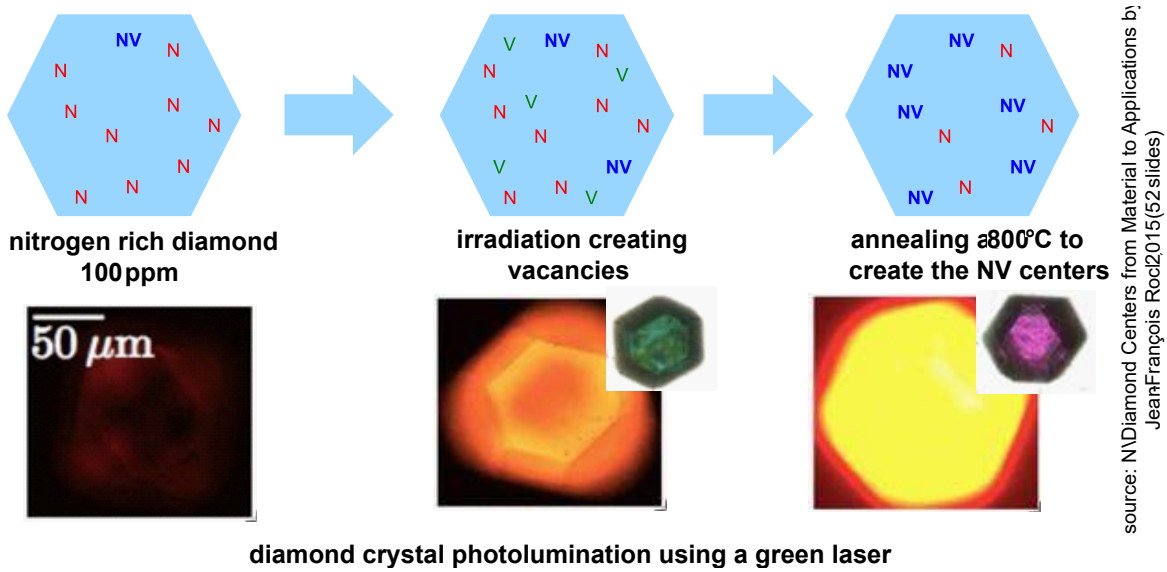

Figure 156: How are nitrogen vacancies created. Source: [1578].

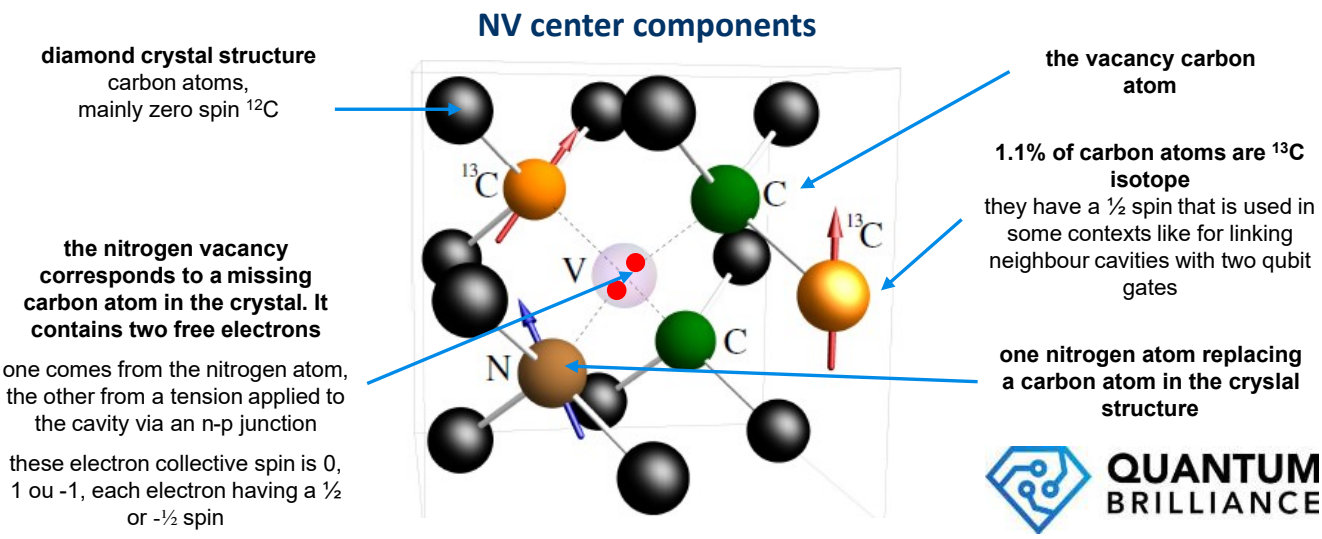

Figure 157: A nitrogen vacancy contains two free electrons with similar or opposite spin which store one qubit of information. The nuclear spins from surrounding ^{13}C are also used to store each one qubit of information, in relation with the cavity spins qubit. ⓒ Olivier Ezratty, 2021.Image source: [1576].

GHz microwaves that change the spin state of the vacancy electrons and switches the vacancy state between $|0\rangle$ and $|1\rangle$. The degeneracy of the spins 1 and -1 at the ^{3}A level (meaning: same energy level for different quantum states) can be lifted by exposing the qubit to a static magnetic field. Other techniques are used to change the qubit state of the surrounding ^{13}C and ^{14}N nucleus spins.

The vacancy qubit readout uses an incoming green photon, usually at 532 nm. It results in an excitation to a state with energy higher than the triplet excited state ^{3}E. Then, the electron relaxes to the ^{3}E state by transmitting part of its energy to atomic vibrations also known as phonons. Subsequently, the relaxation might follow two different paths:

- Back directly to the ^{3}A state by emitting a 637 nm photon (red light).
- Through a channel involving a non-radiative transition from the ^{3}E state to the ^{1}E state assisted by phonons, a radiative transition from the singlet state ^{1}E to the singlet state ^{1}A, which emit an infrared 1042 nm photon and a relaxation back to the ^{3}A state. When following this relaxation path, the final spin state is always zero, regardless of the initial value of the spin.

The probability to follow one or the other relaxation path depends on the spin state. For zero spin state, the first relaxation channel has the highest probability, whereas for ± 1 spin state, the second relaxation channel has the highest probability. As the probability of follow-

ing one of the two paths is never zero regardless of the spin state, this results in an error in the assignment of the spin state, and therefore generates some spin state readout noise.

For the usual NV electron-spin qubit, the computational basis is selected from spin sublevels of the $^3A_2$ electronic ground state, commonly $m_s = 0$ and one of $m_s = \pm 1$. At zero magnetic field the ground-state splitting is about 2.87 GHz, with Zeeman and hyperfine shifts in an applied field. Microwave pulses resonant with the selected transition generate Rabi oscillations and single-qubit gates. The approximately 1.42 GHz resonance belongs to the ^3E excited-state spin manifold at room temperature [1576].

NV-center quantum operations have been experimented at room temperature. A programmable two-qubit processor using the NV electron spin and the ^{14}N nuclear spin implemented universal two-qubit control and small algorithms under ambient conditions [1586]. Room-temperature electronic-spin coherence T_2 can exceed 400 μs even in milled nanodiamonds under dynamical decoupling [161]. In optimized bulk diamond, room-temperature T_1 sits typically in the ms range and T_2 can approach the ms range. A three-qubit room-temperature register consisting of the NV electron, ^{14}N and a nearby ^{13}C was benchmarked in 2025 with an estimated quantum volume of 8 [1587]. That's valid for a single cluster connecting a cavity and a couple surrounding atom nuclei but not yet beyond it. Scalable photonic networking brings different requirements. It needs narrow, stable optical transitions, resonant spin-photon interfaces, high-fidelity single-shot optical readout and high photon indistinguishability, which all require cryogenic temperatures of a few kelvin. Thus "room-temperature NV quantum computing" is valid only for small local spin registers, which can't bring any quantum advantage. It has not been demonstrated for a scalable optically interconnected, fault-tolerant architecture.

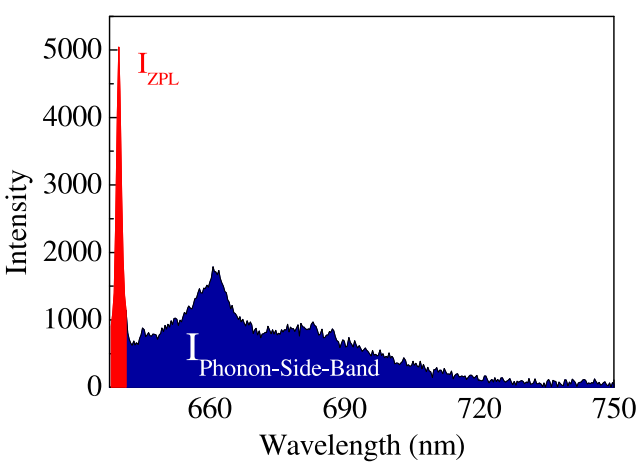

Figure 158: Visualizing a ZPL and phonon-side-band. Source: [1588].

NV centers have a relatively low Debye-Waller factor, of order 3%, meaning that only a few percent of the optical emission is in the 637 nm zero-phonon line while most emission occurs in the phonon sideband [1576]. This mainly reflects electron-phonon coupling and is not simply a thermal effect that vanishes on cooling. Cryogenic operation is nevertheless crucial when the ZPL itself is used as a coherent photonic interface: cooling suppresses phonon-induced homogeneous broadening and resolves the low-temperature excited-state fine structure, enabling narrow resonant transitions, improved spin-selective optical readout and much better photon indistinguishability. This is the key reason that leading NV network experiments use temperatures of a few kelvin, whereas off-resonant fluorescence-based spin control and readout can operate at room temperature.

This interdependence between hyperfine spectral lines and temperature is not unique to diamond cavities. They are common in crystalline structures because temperature modifies many parameters such as the relative arrangement of the atoms in the crystals which leads to changes in electrical and magnetic gradients and therefore spins.

A QuTech-Element Six team demonstrated fault-tolerant building blocks for one logical qubit in 2022 [1589]. The diamond register contained one NV center coupled to 27 ^{13}C nuclear spins. The fault-tolerant protocol used five ^{13}C data qubits, the NV electron spin as an auxiliary qubit and the ^{14}N nuclear spin as a flag qubit. So, 7 physical qubits were actively used. The experiment operated at 4 K. The logical-qubit fidelities did not yet outperform the underlying physical qubits. In November 2024, Fujitsu and QuTech announced an extension of their research partnership for integrated NV-center control and quantum error correction.

In 2025, the same QuTech and ElementSix team implemented a universal gates set using electron spin and nitrogen nucleus spin operating at 4K with excellent fidelities of 99.94% for single-qubit gates ($R_x(\pi/2)_e$, $R_y(\pi/2)_e$ or $I_n \otimes R_{x/y(\pi/2)_e}$) and 99.93% for two-qubit gates (Controlled-$R_x(\mp\pi/2)_n$) [176].

In 2024, the same team obtained a two-qubit gate fidelity of 99.93% using a nitrogen atom nucleus spin coupled to a vacancy. So, only two qubits [175]. Another team, in Japan, implemented a similar error correction code with a Shor-3 code using 6 qubits [1590].

1.5.3 Qubit operations

The general operating principles for these NV-center qubits are as follows [1576]:

- **Qubit quantum state** is based on a two-state computational basis, with $|0\rangle$ corresponding to the ^{3}A energy zero spin base level and $|1\rangle$ to the same level but with a non-zero spin. The computational basis is sometimes $|+1\rangle$ and $|-1\rangle$ corresponding to the two non-zero spin levels of the ^{3}A basis. Most techniques use the neighboring ^{13}C and ^{14}N atoms nuclear spins

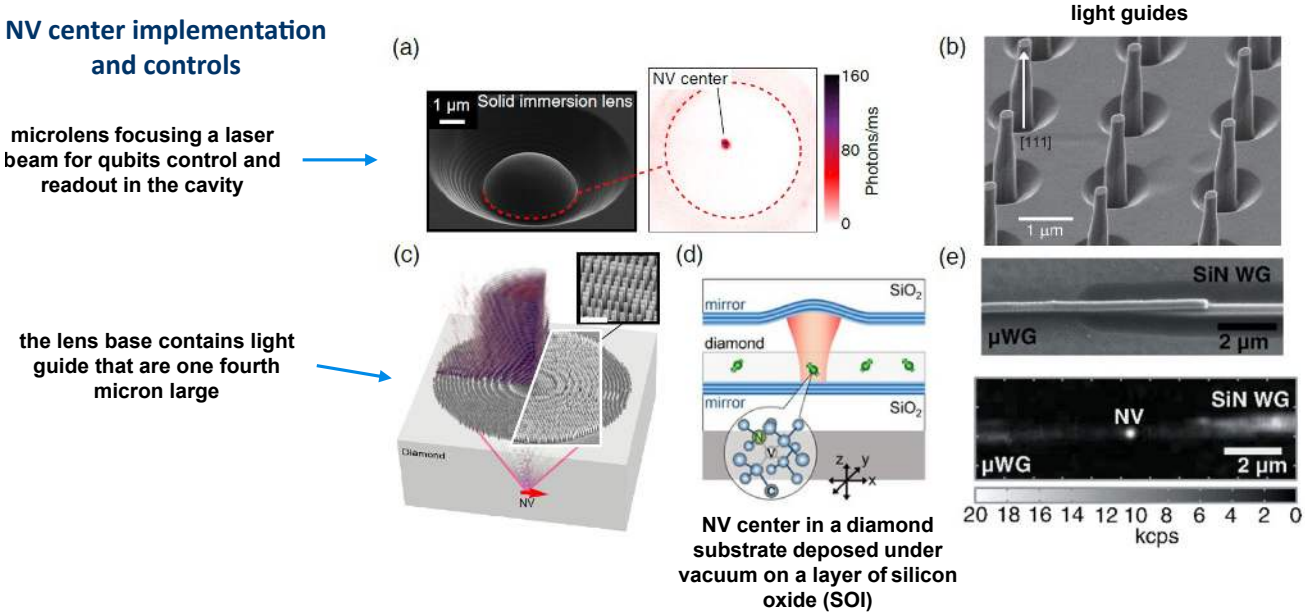

Figure 159: Examples of NV centers implementation and controls to guide laser light on the cavities. Source: [1583].

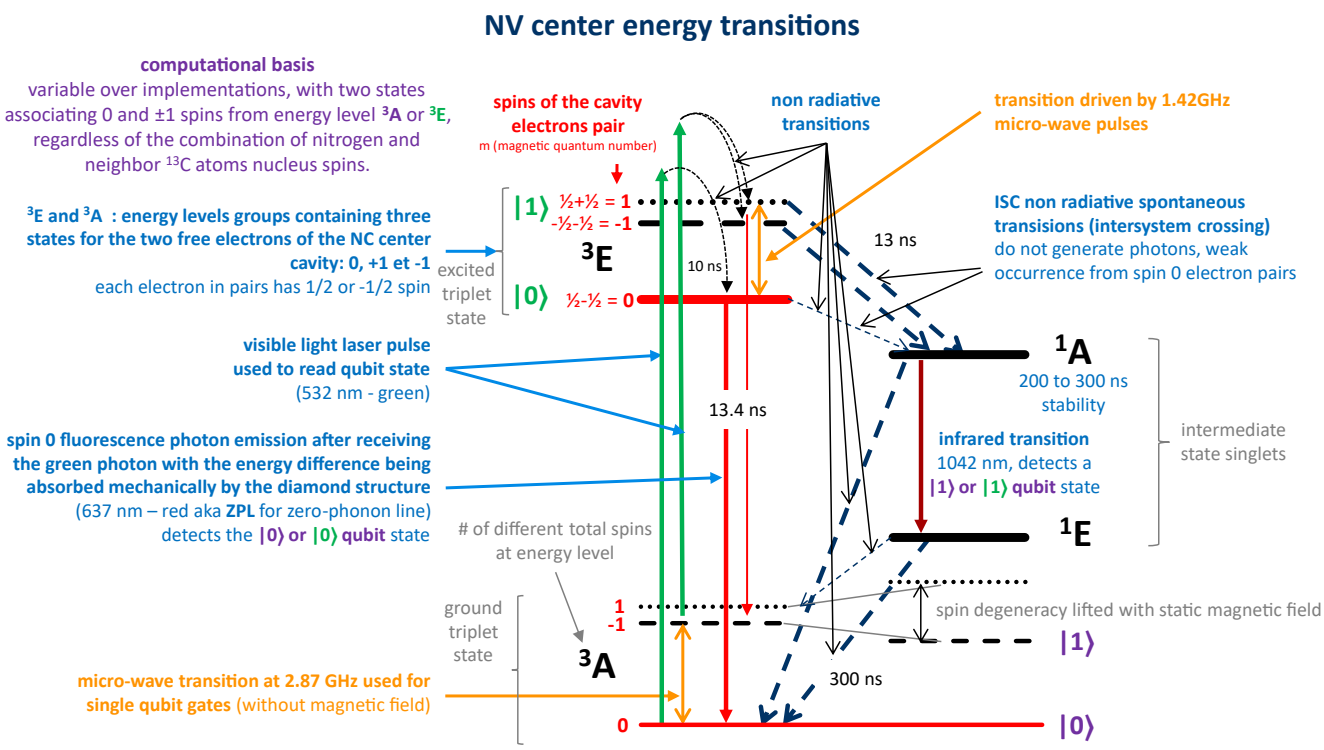

Figure 160: Energy transitions in an NV center, just at the level of the two electrons in the vacancy, regardless of the interactions with the surrounding nucleus spins of ^{13}C and nitrogen atoms. 🅭 compilation by Olivier Ezratty, 2022-September 2026.

as qubits and are arranged in clusters, the NV center electrons spin being used as a mediator to control the neighbor atomic spins.

- **Single-qubit quantum gates** are microwave-activated and exploit spin-state energy transitions at a frequency of 2.87 GHz. Hyperfine transitions are energetic transitions of low energy electrons, here in the microwave regime, which are generally related to the interaction between the magnetic polarities of the nucleus of the atoms with the magnetic field generated by the electrons. Knowing that here we are talking about electrons that do not rotate around the nucleus of an atom but in a cavity. They could use nanoscale magnets [1591].

- **Two-qubit quantum gates** inside one NV-centered register exploit hyperfine coupling between the vacancy electrons and nearby ^{13}C or ^{14}C nuclear spins, with the electron spin acting as a fast ancilla and

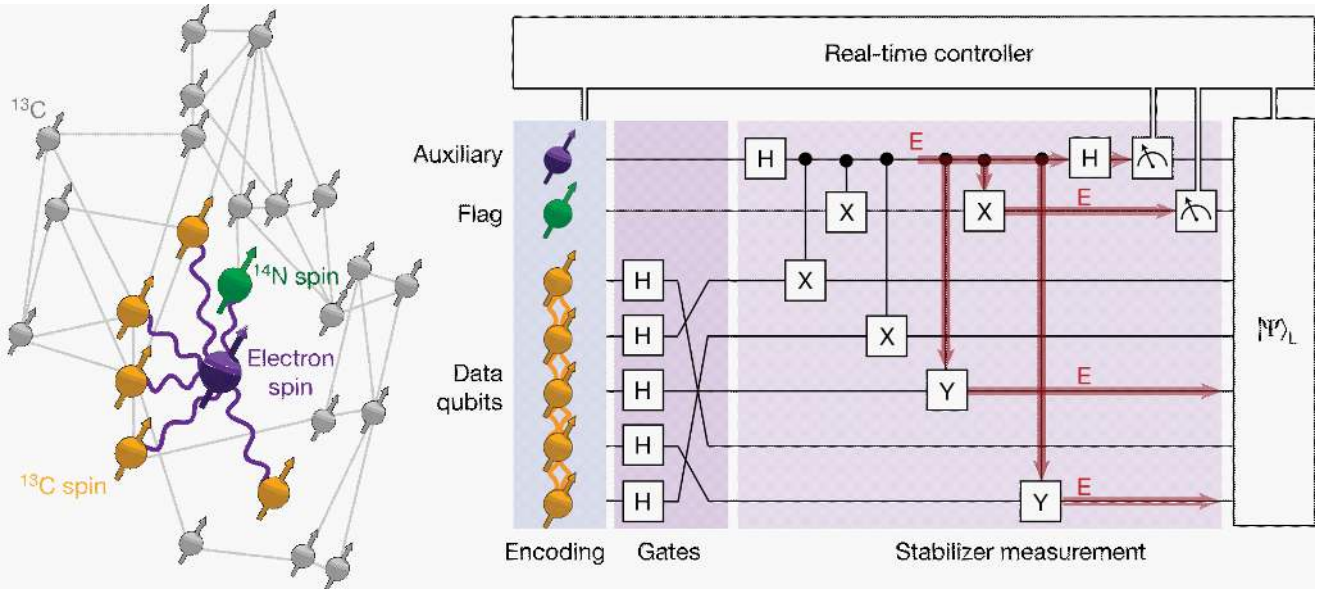

Figure 161: An error correction code implemented with NV centers qubits. Source: [1589].

communication bus. Direct dipolar coupling between nearby electron spins is another short-range option. Connecting separate NV-centered registers is much harder because the useful nuclear spins are only strongly coupled over nanometer scales. The most mature register interconnect solution is optical: each NV electron spin is entangled with an emitted photon, photons from two nodes are interfered and detected to herald remote spin-spin entanglement. Then, local electron-nuclear gates and teleportation implement a non-local gate. This route has progressed from heralded remote entanglement to an unconditional teleported CNOT between nuclear-spin qubits in two separate diamond nodes [1592]. Mechanical resonators provide a more speculative alternative for programmable interactions [1593].

- **Qubits readout** commonly uses spin-dependent fluorescence. Off-resonant green excitation is typically near 532 nm and excites the NV^- optical transition into the ^3E manifold. The $m_s = \pm 1$ states have a larger probability of entering the non-radiative intersystem-crossing path through the singlet manifold than $m_s = 0$, so they produce less visible fluorescence. The NV^- zero-phonon line is at 637 nm, not 689 nm, with a broad red-shifted phonon sideband. ODMR combines this spin-dependent fluorescence with microwave excitation of the spin resonance. Ensemble and single-NV fluorescence readout can operate at room temperature. Cryogenic temperatures become important for resonant optical excitation, high-fidelity single-shot electron-spin readout and coherent spin-photon networking. Alternative techniques include spin-to-charge conversion [1594] and repetitive or ancilla-assisted readout using nearby nuclear spins.

Figure 162 shows a schematic diagram of the control mechanism for these qubits [1595]. The few full-stack experiments use between 2 and 5 qubits, all related to a single cavity [1596]. Scaling is still a challenge, particularly with qubit readout [134].

One of the strongest scalability arguments for NV centers is their spin-photon interface. Delft experiments have demonstrated heralded entanglement over metropolitan fiber and, in 2026, an unconditional teleported CNOT between ^{13}C nuclear-spin qubits in two separate NV-center registers [1592]. Each node is still very small, but this is a concrete demonstration of the modular architecture needed to connect local electron-nuclear spin clusters.

The technology is not easy to industrialize on a large scale, whether it is the chip itself or the control lasers (Figure 163). There are also numerous challenges at the diamond substrate level on for the ions implantation [1597]. Manufacturing at scale can use laser-cutting method, electron-beam lithography (EBL) with a two-step transfer pattern utilizing a silicon nitride hard mask material associated to reactive ion etching (RIE) [1598], or use silicon masks to define large arrays of nanoscale optical structures [1599].

1.5.4 Research

The main countries involved are China, the Netherlands (TU Delft and QuTech which demonstrated a 10-qubit prototype with a coherence time of one minute and working at 3.7K in 2019 [162]), Australia (University of Melbourne, Quantum Brilliance), Germany (University of Ulm), Japan (NII and NTT, Fujitsu along with QuTech, who work on tin-vacancy (SnV) centers, and NV centers [176, 1610]), some laboratories in France

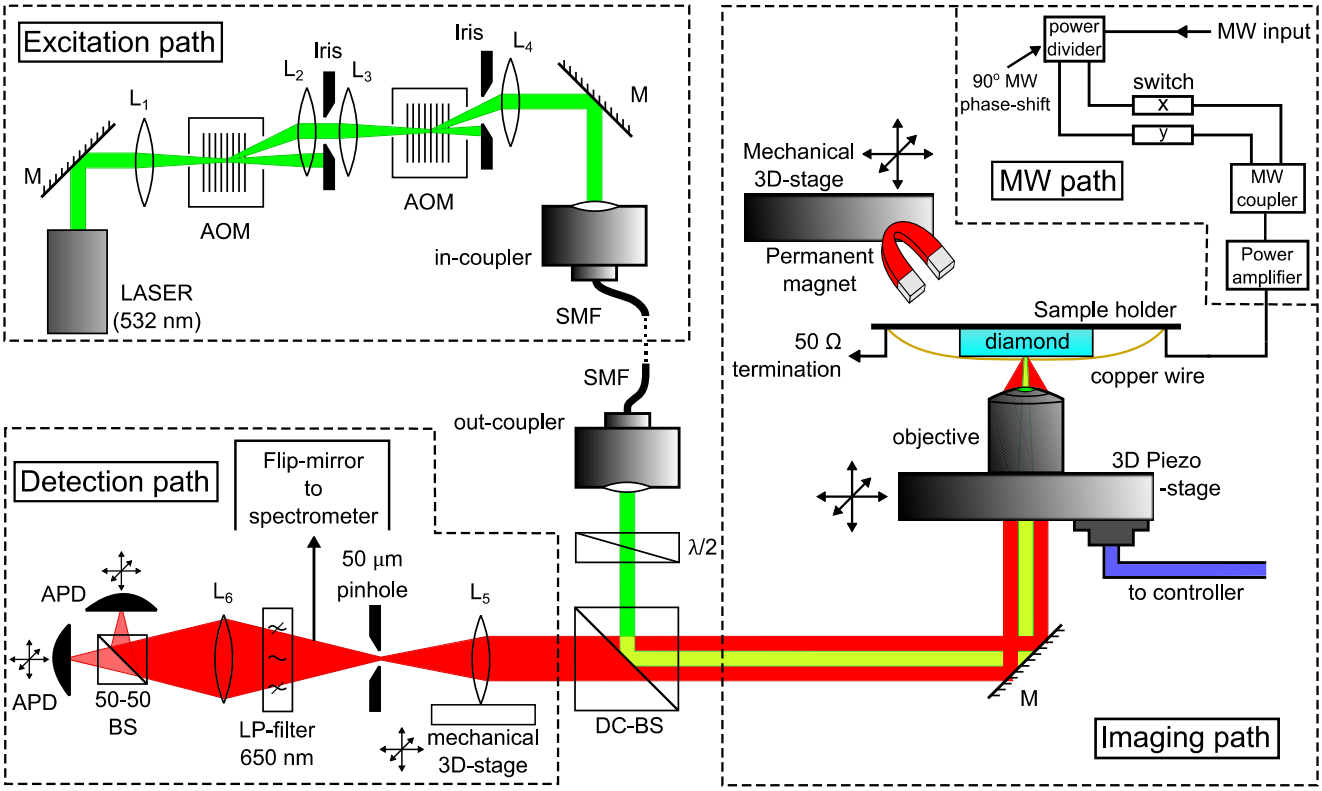

Figure 162: Characterization of NV centers setup. Source: [1595].

(such as CEA SPEC) and of course in different labs in the USA (Harvard, MIT, …).

NV Centers based quantum computers have been very low key for a few years. It seemed that NV centers have more promising uses in quantum sensing for the creation of precision magnetometers or for quantum memories interoperable with qubits realized with other technologies such as superconducting qubits in hybrid systems. This is a path explored by the University of Delft [1611], in Japan [1600] and by CEA-SPEC with Patrice Bertet as shown in Figure 164, with a superconducting qubit linked to a NV center memory qubit.

There are also variants of NV center techniques with defects introduced in phosphorus-doped silicon carbide. It would have the advantage of creating qubits whose readout is more accurate since being based on the emission of a narrow frequency fluorescence [1612].

In a similar fashion, **MIT** prototyped in 2020 a NV centers chip replacing nitrogen with silicon and germanium, a technique also explored in Europe [1613]. They assembled 128 qubits, but these were not operational [1614]. Researchers in China are also experimenting with NV-center qubits but so far, their prototype had only 3 qubits in 2024 [1615].

They said they could reach 99.92% CNOT fidelities in 2022, to no avail [1616]. In another work, Australian researchers were able to implement single Clifford group qubit gates with NV^- centers with a fidelity of 99.3% [1617]. Harvard researchers are working on creating entanglement gates using nanomechanical resonators with programmable connectivity via mechanical transport of qubits in nanopillars. It is weird but interesting [1618].

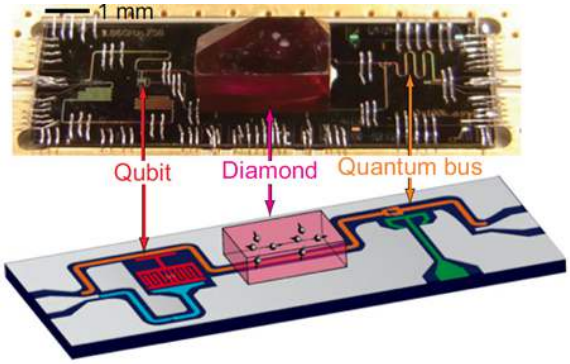

Figure 164: NV center used as a quantum memory for a superconducting qubit, which could lead to create heterogeneous qubits. Source: [1619].

1.5.5 Manufacturing

Artificial diamonds are produced either with high-pressure high-temperature processes (HPHT) or with chemical vapor deposition (CVD) [1581]. The latter is used for quantum use cases.

One of the challenges to create functional NV centers quantum processors is the precise implantation of vacancies and nitrogen atoms in diamonds. NV centers are manufactured using various methods. NV vacancies are usually produced by electrons, neutrons, protons, or

NV centers key takeaways

highlights

- **room-temperature local operation is real**: coherent control, local electron-nuclear entangling gates and small algorithms have been demonstrated at ambient temperature, but the best coherent optical interconnect and single-shot readout demonstrations remain cryogenic [1586, 1587].
- **works at 4K**, with simple cryogeny without dilution and helium-3 [164].
- **long coherence time**: above 1 ms.
- **strong and stable diamond structure**.
- can also help create **quantum memory** for other qubit types, like superconducting qubits [1600].
- possible to integrate NV center qubits with **optical quantum telecommunications** [1584].

challenges

- **room-temperature scalability is oversold**: RT 2-qubit gates experimentally established, but no RT architecture has been demonstrated with optical networking between registers [1586, 1587].
- **local two-qubit gate fidelity is OK**: with about 99.93%, but this does not extend to register interconnect and photonic links [176].
- **scaling remains modular and experimentally immature**: registers reached $\leq$10 spins, but photonic interconnect demonstrated between tiny registers. [134, 1592].
- **qubit control is complex**, mixing lasers and microwaves, and is not easy to scale [1595].
- **applications** are more centered on quantum magnetometry and sensing than on computing.
- **circuits manufacturing** is complicated at scale [1597, 1598].
- **two-qubit gates are probabilistic** for the spin-photon flavor used by T centers [1601].

variations

- **silicon carbide (SiC)** and **T centers** [1602, 1603].
- **silicon in diamond vacancies (SiV)** [1604, 1605].
- **tin vacancies (SnV)** [1606, 1607].

path to scalability

- **scale through modular photonic links**: use the vacancy electron as the spin-photon interface and local bus to nuclear memories, herald remote electron-spin entanglement, then teleport gates between nuclear-spin qubits. Demonstrated at 2-node scale but limited by entanglement rate, photon collection, indistinguishability, loss and switching overhead [1592].
- **manufacturing improvements** for cavities and nuclear-spin placement [1599, 1608].
- **on-chip qubit control** densification and routing [1583].
- **laser and optical control** at scale [1609].

Figure 163: NV centers qubits key takeaways: highlights, challenges, variations and paths to scalability. Olivier Ezratty, 2022-2026.

ions irradiation to create the vacancies followed by thermal annealing at temperatures above 650 °C to move the vacancies close to the defect atoms (here, nitrogen). A tiny share of nitrogen atoms impurities is deposed during the CVD (chemical vapor deposition) production of artificial diamond.

One technique makes use of targeted ion depositions of ion beams with masking and ebeam lithography nanopatterning, as shown in Figure 165 [1620]. The University of Bristol created a variation of this process with positioning nanodiamonds on a silicon-nitride wafer and using an array of optical fibers to control it [1609]. Another promising technique created by Berkeley Labs is based on gold ions implantation that could scale to thousands of qubits [1608].

1.5.6 Vendors

Quantum Brilliance (2019, Australia), **Turing Inc** (2016, USA), **XeedQ** (2021, Germany) and **SaxonQ** (2021, Germany) are the startups dedicated to creating NV center-based quantum computers.

Public vendor products remain in the few-qubit regime when judged by independently characterized, jointly controllable registers, even though some vendors advertise much larger "multi-core" aggregate qubit counts. The central scaling issue is not creating many defects but coherently connecting NV-centered electron-nuclear registers. Short-range hyperfine and dipolar couplings work within a local cluster. Between clusters, the leading architecture uses photons to herald remote entanglement and then gate teleportation, making the platform closer to a modular quantum network than to a monolithic nearest-neighbor chip.

Quantum Brilliance

Australia-Germany, 2019, $49.4M

Quantum Brilliance develops NV centers QPUs operating at room temperature, created by ANU (Australian National University) researchers, Andrew Horsley (CEO) and Marcus Doherty (CSO). The company also has offices in Singapore, Japan, and the UK.

Technology. They estimate that their solution will be size/weight/performance/cost/power competitive and bring some quantum advantage earlier than competing systems from Google and IBM that they brand « quantum mainframes ». They want to create "quan-

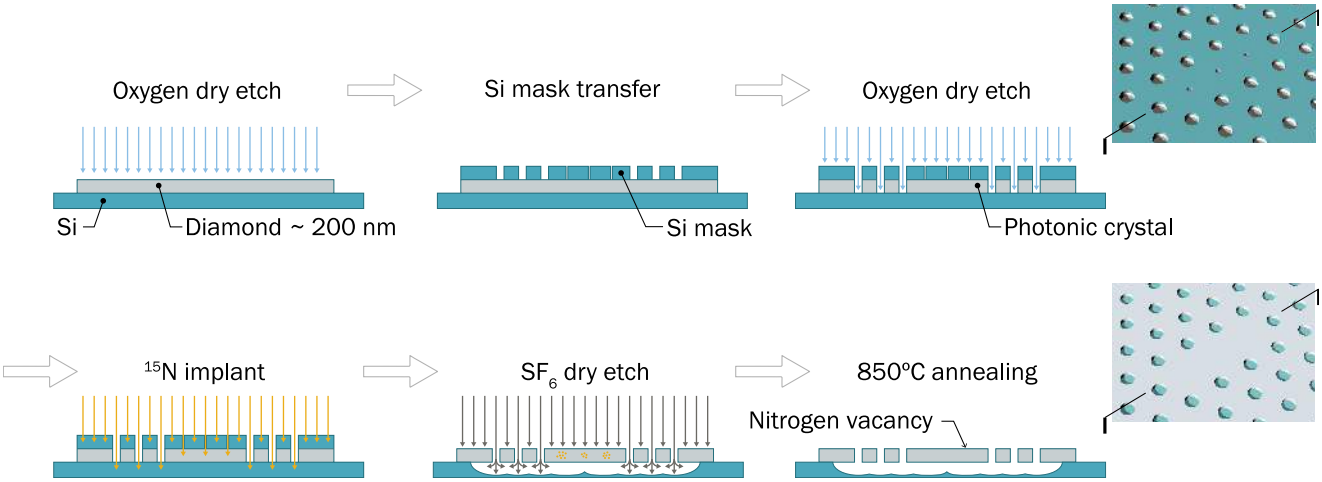

Figure 165: Example of NV center implantation technique using a mask. Source: [1620].

tum desktops" that operate at room temperature [1621]. Based on this promise, they were selected in September 2024 by the Agency for Innovation in Cyber Security in Germany to build a portable quantum computer for the army as part of a €35M program split over three projects (with them, Oxford Ionics and neQxt (trapped ions).

They introduced in March 2021 a five-qubit prototype fitting into a 2U classical 19-inch server form factor [125]. They expect to reach 50 to 100 qubits by 2028 and to then scale up this architecture by connecting several units together [1622, 1623]. One future step is to fit their whole system into a large PCI board as shown in Figure 166.

Fidelities. To learn more about these systems, you need to look at the scientific papers coauthored by Marcus Doherty [1624–1626]. You find that they have an error rate of 10^{-5} for single qubit gates, which is fine, and expect to have a similar level for two-qubit gates. But what is documented is a 99.2% two-qubit gate fidelity, which is not stellar nor sufficient to implement fault-tolerant quantum computing.

In January 2022, Quantum Brilliance announced the launch of DE-Brill, a joint research project with the Fraunhofer Institute for Applied Solid State Physics IAF and the University of Ulm funded by the German government quantum plan. The partnership is focused on the development of manufacturing (Fraunhofer) and control (Ulm) techniques of NV center qubits. The total investment of this 5-year project starting in December 2021 was €19.9M with 78.4% funded by BMBF, the German ministry of research. The project was then completed by the SPINNING project with an enlarged number of academic and industry partners. It demonstrated in October 2024 the entanglement of two registers of six qubits over a distance of 20 meters and a high mean fidelity. The SPINNING project involves QINU, a cryostat vendor created out of KIT in Karlsruhe. This does not by itself show that Quantum Brilliance's local spin processor requires cooling. It does, however, illustrate that cryogenic operation remains relevant when the R&D objective includes narrow-line optical interfaces, high-fidelity readout or photonic interconnection.

Quantum Brilliance deployed its QB-QDK2.0 QPU at Fraunhofer IAF in June 2025, which fits in a standard 19 inches rack without cryogenics. It seems it is always stuck with 5 or fewer qubits. NV centers are far away from showing an exponential growth in qubit numbers! It's flatland.

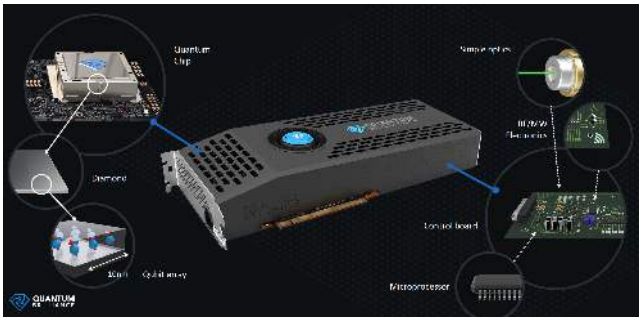

Figure 166: Quantum Brilliance PCI board. Source: Quantum Brilliance.

In April 2022, the company launched a joint R&D hub with La Trobe University and RMIT University around material design and manufacturing. This and other German universities working on NV centers [1627] create a critical mass of skills in NV centers aimed at quantum computing. Germany's involvement deals with manufacturing these NV center based chips with high precision. Fraunhofer IAF purchased a Quantum Brilliance QPU in 2024.

Customers. At home in Australia, the **Pawsey Supercomputing Research Centre** announced in June 2022 the installation of a Gen1 Quantum Brilliance quantum accelerator with two qubits. In their current QPU, ^{13}C nucleus spins are controlled with radiofrequencies, microwaves for the cavity electron spins and optical channels for fluorescence readout, with the electron getting its spin from surrounding ^{13}C nucleus, implementing a

QND (non-demolition measurement). At this point, the system does not require any cooling, but qubit fidelities and other figures of merit may need cooling at some point. All control electronics fit in a 6U 19 inch chassis. Supported qubit gates are RX, RY and CZ. It uses a typical star model with several ^{13}C atoms surrounding one nitrogen vacancy. Quantum Brilliance even tested some QML algorithm on this QPU [1628]. In September 2024, the company announced a partnership with Oak Ridge National Laboratory (ORNL) to test their system.

Software. In April 2021, Quantum Brilliance announced a partnership with **Quantum-South** (Uruguay) and to develop proof of concepts optimization quantum applications for air and maritime cargo companies.

In 2023, Quantum Brilliance released its Qristal software suite that contains the Qristal Emulator, supporting C++ and Nvidia CUDA APIs, Nvidia QODA programming environment and MPI (Message Passing Interface, an open library standard for distributed memory parallelization used in large-scale parallel computing [125]). They are developing small scale machine learning quantum algorithms [1628].

Turing Inc

USA, 2016, $15.5M

Turing Inc is a startup willing to create quantum computing hardware and software, based on NV centers qubits and operating at 4K [1629].

They also develop error correction systems that they market to other industry specialists. A way to avoid putting all your eggs in the same basket! Finally, they seem to work on some form of quantum memories that could be useful in entanglement based QKD deployments.

XeedQ

Germany, 2021

XeedQ develops XQ1, an NV-center-based multi-qubit mobile quantum processor running at room-temperature (Figure 167). Their XQ1 fits in a desktop format with 4 qubits and with a power of only 150 W. It has two-qubit gate fidelities of >90% and single qubit gate fidelities of 95% which is quite average.

The company created by Gopalakrishnan Balasubramanian, formerly at the Max Planck Institute for Biophysical Chemistry in Göttingen and is based in Leipzig. He published a wealth of papers on the physics of NV centers but not on NV-centers-based quantum computers nor how do you entangle such qubits at room temperatures.

They planned to release a 256-qubit version by 2026 and to deliver their first QPU "Baby Diamond" to Goethe University as of early 2024 (it was done in November 2024). It is weird to read on their web site that "*quantum systems offer encryption standards that are virtually impossible to breach. Welcome to future-proof quantum secure communications on a mobile footprint*". Someone should tell them that PQC doesn't need a quantum computer to run.

In 2023, XeedQ got a €30 M grant from DLR for the development of their scalable quantum computing technology, with a 32-qubit, fault-tolerant quantum computer target by 2026. They are also exploring analog quantum computing approaches. In September 2024, it announced the creation of "Quantum Information Technology Centres" in Telangana and Tamil Nadu in India for the democratization of quantum computing, and to which the company is to deliver 32-qubit QPUs.

In 2026, researchers from Deutsche Telekom, TU Dresden and the University of Bologna experimented a 2-qubit room-temperature XeedQ system to implement a QAOA for MAX-CUT. The physical qubits were the NV cavity electron and the ^{14}N nuclear spin. The circuit contained only 7 gates (2 H, 2 CNOT, and 3 single qubit rotations) and had a 12.3% average error. The two-qubit CNOT gate lasted 13 μs [149]. The paper was published on April 1st.

SaxonQ

Germany, 2021

SaxonQ is based in Leipzig and was cofounded by Marius Grundmann (CEO), Dominique Bouwes (COO) and Jan Meijer (CTO). It wants to create some NV center based mobile quantum computer. The system is mobile, on wheels, and has a size of about half a rack (Figure 168).

The startup website references some old scientific papers focused on the manufacturing of their chip [1630, 1631]. They also mentioned that they offer 80-qubit multicore QPUs with multiple NV chips working simultaneously to accelerate runtimes.

In April 2025, they demonstrated along with Quantum Machines their room temperature QPU at Hannover Messe 2025, showcasing some hydrogen quantum chemical calculations and image recognition, without any mention of the circuit depth or breadth. Their system power consumption is of 600 W [1632].

In June 2025, they deployed a 4-qubit QPU at the Dresden branch of Fraunhofer IWU. And in 2026, they introduced the SXQ128 with 16 cores of 8 qubits, and the SXQ512 with 32 cores with 16 qubit each, this last number being surprisingly high. As of September 2026, no public independent benchmark or peer-reviewed disclosure of these systems was identified. Also, needless to say that this cannot bring in any quantum advantage given a GPU-based emulator is faster than a QPU below 30 qubits.

In 2026, the company published a roadmap in a white paper Figure 169. It exhibits a scale-in and scale-out approach. Scale-in comes with increasing the number of qubits in a single core, around a vacancy and several nu-

Figure 167: XeedQ XQ1 tower desktop format QPU. Source: XeedQ.

Figure 168: SaxonQ mobile QPU. Source: SaxonQ.

cleus spins, supposedly 9 in 2026 and over 10, plus some connection between the spin-nucleus clusters. Scale-out comes from arranging multiple cores on a system, to run small circuits in parallel, the topmost goal being 80 physical qubits per core in 2030, without any indication of the qubit connectivity and potential operation fidelities at that scale. Aggregating independent small cores increases throughput of parallel small circuits execution, but does not increase the Hilbert-space dimension of a quantum circuit. Therefore a 16-core system of 8-qubit processors is not equivalent to a coherent 128-qubit processor. There is no universal qubit-count threshold below which quantum advantage is mathematically impossible, although generic circuits on only a few tens of qubits are usually easy to emulate classically. Even an 80-physical-qubit core would remain a NISQ-scale device unless it supported sufficiently high-fidelity error correction and logical qubits.

In September 2026, they published a preprint on the implementation of a Grover search using 3 nuclear spin qubits [1633]. Without some scaling potential, which is already questioned for Grover due to the cost of prefactors, one can wonder where it can lead them.

	2023	2025	2026	2027	2030
# of NV	1	2	3	4	>8
# of nuclei per NV	3	5	9	10	>10
qubits per core	4	12	30	>40	>80
# of cores	1	2	4	32	128
total # of qubits	4	24	120	>1.000	>10.000

Figure 169: SaxonQ quantitative roadmap given the 2025 and 2026 milestones didn't seem to be achieved as of September 2026. Source: [1632].

Quantum Transistors

Israel, 2022, €17.5M

Quantum Transistors is building a NV center-based quantum processor. It was cofounded by Shmuel Bachinsky (CEO) and Moshe Tordjman (CTO), who was previously a researcher from Technion and MIT.

In July 2024, they got a funding of a total of €17.5M from the EIC Accelerator and EIC Fund [1634]. Quantum Transistors is one of the 9 Israeli startups who got €130M in grants from the EIC Accelerator Program out of a total of €411M awarded to 68 companies. Israel was third in the number of grant recipients after Germany and France with 13 companies each.

They published in December 2025 a preprint describing how they plan to implement low-error quantum gates, reaching 2×10^{-5} error rates for two qubit gates operating at 4K [116].

They further documented their platform in [116] with introducing PUDDING (Power-Unaffected, Doubly-Detuning-Insensitive Gates), a theoretical framework to create conditional quantum gates like a CNOT that are inherently immune to the most common types of hardware errors. They use SNSPDs for qubit readout in place of the SPADs that they were using initially. They use silicon nitride (SiN) chips for the photonic operations.

They experimented error rates of 1.9×10^{-4} for single qubit gates and 4.5×10^{-4} for two qubit gates when using the PUDDING protocol at room temperature. They then extrapolated these values for operations at 4K, yielding 2×10^{-7} CNOT error rates (Figure 170).

They use optical photons, non-local connectivity between the qubits, designed a 16-qubit chip, stacked chips of 20 × 20 mm with 25 qubits per mm^2, and a

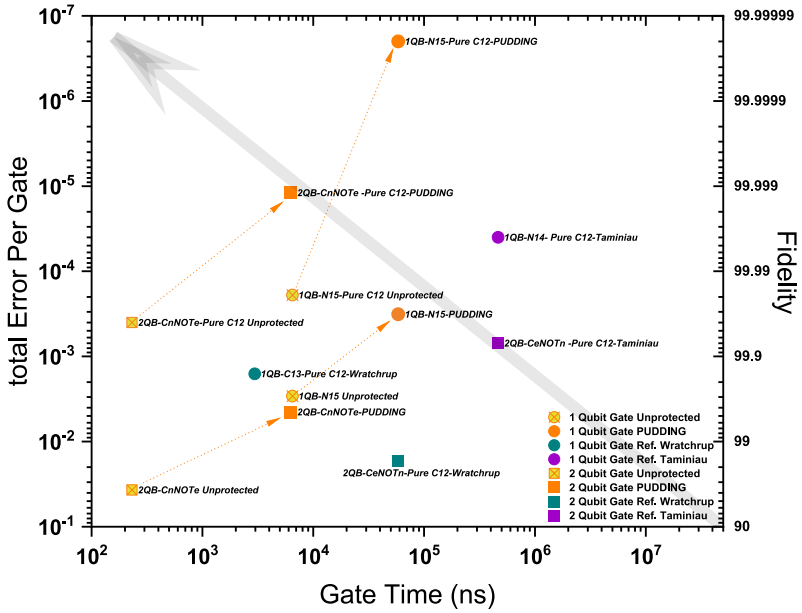

Figure 170: Quantum Transistor single and two-qubit gate fidelities. Source: [116].

total of 10K qubits. Their diamond qubits are 4 μm long. Their roadmap is to support 250K qubits by 2030 with 10^{-5} error rates. They use their own diamond fab from the diamondSEMI-IL consortium in Israel.

1.5.7 Other spin cavities variants

Besides NV centers, another similar technique is investigated at the research stage that uses various vacancies:

- Silicon carbide (SiC) vacancies can be missing nearby couples of carbon and silicon atoms, called divacancies ($V_{Si}V_C{}^0$) or just a missing silicon atom ($V_{Si}{}^-$) [1602]. SiC qubits could theoretically work at ambient temperature [1635, 1636] and reach a minute of coherence time [1637].
- Magnesium oxide MgO NV^- cavities [1638].
- Silicon T, W, G and C centers which involve vacancies, carbon defects and sometimes hydrogen defects [1603]:
  - T centers have a substitutional carbon atom paired with an interstitial carbon atom, forming a complex defect. They can emit light in the infrared and are used in silicon photonics and quantum communications. These are used by Photonic Inc.
  - W centers use four silicon atoms arranged in a tetrahedral configuration [1639].
  - G centers are related to the presence of carbon in silicon where a carbon atom is paired with an interstitial silicon atom. They are also used in silicon photonics.
  - C centers involve a pair of oxygen atoms (an oxygen dimer) occupying interstitial sites within the silicon lattice.
- Silicon in diamond vacancies (SiV) [1604, 1605, 1640].
- Germanium vacancies (GeV^-) and tin vacancies (SnV^-) [1606, 1607, 1641].
- Transition metal defects with chromium, vanadium, molybdenum, tungsten [1642], erbium [1643] and hexagonal boron nitride (h-BN) [1644–1647].
- Oxygen vacancies (aka ST1) implantation in diamond are studied in China [1648] and in Hungary [1649].

In 2022, a research team from the DoE Argonne National Lab created a prediction model of the coherence time of vacancies depending on their characteristics, which can help investigate new materials. [1650, 1651] shows that the coherence time T_2 of vacancies is dependent on the cavity spin density (n_i) of nucleus i, the crystalline structure, the nuclear spin-factor (g_i), and the nuclear spin quantum number (I_i) according to the formula:

$$T_{2,i} = 1.5 \times 10^{18} \left|g_i\right|^{-1.6} I_i^{-1.1} n_i^{-1.0} \text{ (s)}$$

While these vacancies could be used to create qubits and quantum processors like with NV centers, they are currently aimed mostly at quantum photonics applications.

SiC vacancies have fluorescence wavelengths corresponding to fiber optics telecom wavelengths in the near infrared band around 1.5 μm, in the so-called 4H-SiC hexagonal lattice version [1652, 1653] (Figure 171).

SiC vacancies can indeed be used as interesting sources of single or entangled photons in quantum communications and cryptography. SiC photon sources are implanted on nanophotonic devices [1654, 1655]. It could also be used in quantum repeaters thanks to relatively long spin coherence times above 50 ms. Also, SiC vacancies can

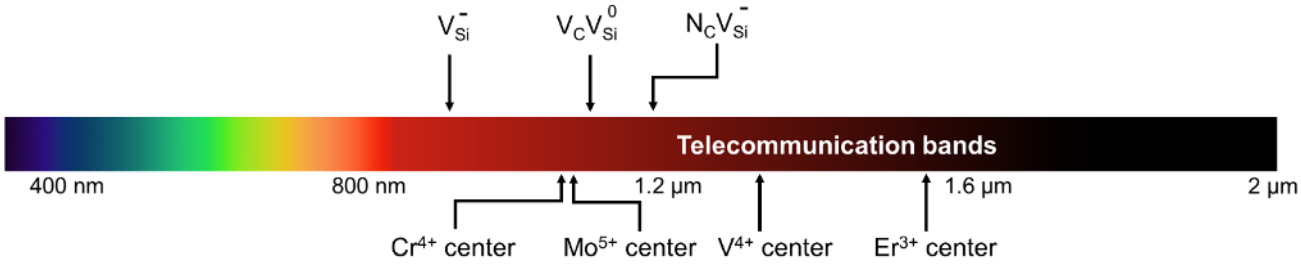

Figure 171: Other cavities are interesting due to their transition frequencies that sit in the telecommunication wavelengths. Source: [1652].

show a much better DWF (Debye-Waller factor) than diamond NV centers. However, their readout contrast must be improved [1656].

In quantum information processing, SiC vacancies are investigated in various areas such as with quantum simulation and measurement-based quantum computing. There are some specific technology paths like using SiC spin qubits that are coupled by photons [1657].

SiC vacancies have very long coherence times in the seconds range [1658]. It leads to theoretically long computing time, although, it would work with solving many other problems like large entanglement capacities and high two-qubit gate fidelities. Thus, when you read in the media that SiC could achieve a hundred million operations, you may get skeptical and right to be so [1659]. Indeed, the related paper simply computes this number of operations by dividing SiC qubit coherence time of 5 seconds by a single-qubit gate time.

They have not implemented it yet, particularly given it is useless to do that on a single qubit. It would be nice to have a tomography of a 2-qubit gate...:)! Then, you must deal with the specifics of the readout of ^{29}Si and ^{13}C nuclear spins readouts used in such devices [1660].

Photonic Inc

Canada, 2019, $317.5M

Photonic Inc is a spin-off from the Silicon Development Lab at Simon Fraser University in Vancouver with Stephanie Simmons as their Chief Quantum Officer, Don Mattrick as the new CEO since March 2026, Paul Terry as CTO (formerly CTO), and 150 employees as of Mid2026. Microsoft is one of their investors in their 2023 round of $100M. A subsequent funding of $130M was announced in January 2026. In 2025, it announced the creation of a R&D center in the UK which would host 30 scientists.

Technology. Photonic's technology is based on "T" defects in silicon, *aka* "T centres", using similar techniques as with SiC and NV vacancies [1661–1663]. At the physical level, processing and memory qubits are handled with nuclear spins of hydrogen and ^{13}C atoms in a ^{28}Si substrate [1664]. Silicon vacancy electron spins are used for the indirect non-demolition measurement of these nuclear spin qubits and to create spin-photon interactions in the telecommunications wavelength band O (around 1,326 nm). The whole nuclear and electron spin ensemble form these T centres and are placed in optical cavities connected in a many-to-many fashion through a web of optical fibers and (not detailed) routing. This helps create short and long-distance entanglement sharing between qubits (but heralded, so in a probabilistic manner), enabling gate teleportation (two-qubit gates) [1601]. As a result, high connectivity demanding qLDPC quantum error correction codes can be used. It led the company to create its own qLDPC codes [1665].

Papers published in 2025 showcase the very low TRL of the technology. Like where they excite the silicon T centre with nanophotonic waveguides and cavities with p-i-n diodes, leading to an initialization fidelity of 92% [1666], when they test the dynamics of spectral wandering of individual silicon T centres using spectral correlation measurements [1667] or when they test deuterium T centre variants (an isotope of hydrogen), which have longer lifetimes than regular hydrogen atoms in the cavity [1668].

In August 2026, the company published a preprint about using singly-ionized interstitial aluminum donor in place of T centers (Al_i^+). This enables the generation of photons in the telecommunications band (1.56 μm and 1.31 μm) [1669]. While they didn't state it would be their production architecture, it shows that they may not yet be sure about it.

Roadmap. The company expects to create chipsets handling up to 1,000 T centres and 4,000 optical fibers, all this being driven by global and local electric and magnetic fields. The way they plan to manufacture these chipsets is not clear yet, particularly with regards to the precise positioning of the T centres in the ^{28}Si substrate. The chip is operating at about 1K to 2K.

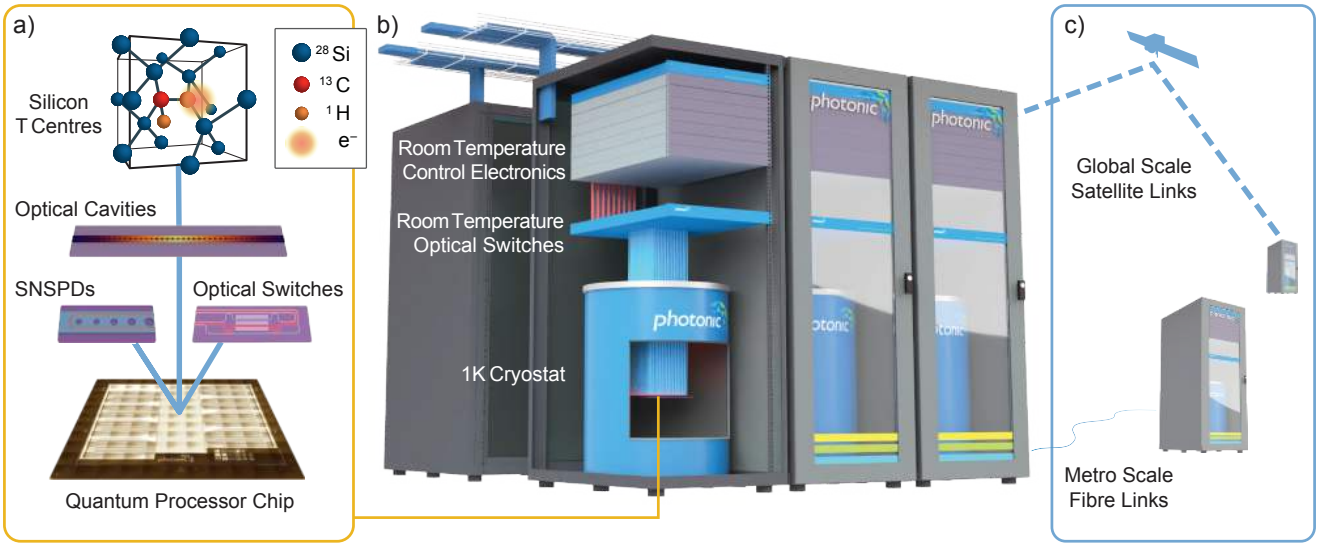

Figure 172: Photonic Inc concept view of their QPU and related photonic connectivity. Source: [1661].

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This **NV centers qubits** subsection contains 103 bibliographical references and notes containing at least 1,732 pages.

1.6 Topological qubits

In this category of qubits and quantum computing, we must create a distinction between the notion of "topological" which defines a type of qubit based on anyons and the "Majorana fermions" or "Majorana Zero Mode" (MZM) which are a variant of anyons to create topological qubits. Of all the qubit modalities, they are the most mysterious and complex to understand [1670, 1671]. They are also the most controversial, due to the wishy-washy history of Microsoft in the domain. This is a very low TRL technology (Figure 174).

1.6.1 History

Ettore Majorana predicted in 1937 the existence of a new class of particles that are their own anti-particles. These were labelled "Majorana fermions". The notion of anyon "quasiparticle", i.e. particle representation models that describe the state of electron clouds around atoms, in the superconducting regime and in 2D, was first proposed by Jon Magne Leinaas and Jan Myrheim from the University of Oslo in 1976-1977 and then elaborated by Frank Wilczek in 1982 [1672–1674]. He provides an excellent simplified view of what are anyons, braiding and quasiparticles. The author explains three specifics of quasiparticles: fractionalization (where quasiparticles have properties that are subparts of usual whole-number multiples like spins or unit of electron electric charge or angular momentum), flux tubes (fractional angular momentum made possible by particles orbiting around tubes of magnetic flux like in type II superconductors) and dimensional reduction (with point-like structures).

Majorana fermions are a specific type of these quasiparticles organized along various types of superconducting structures, one of them being a nano superconducting wire. They have collective electron behaviors in crystalline networks at very low temperature [1675].

Alexei Kitaev then had the idea in 1997 to use anyons for quantum calculations, when he was at the Landau Institute for Theoretical Physics in Moscow, several years before joining Microsoft Research [1676, 1677]. He published two foundational papers in 2000 describing the category of fermionic quantum computers and a model of spinless fermions in a 1D superconducting nanowire, *aka* a Kitaev chain [1678–1680]. There are several variations of fermionic quantum computing being investigated, including analog quantum computing with cold atoms [1681, 1682] or with specific superconducting settings like Cooper pair splitters [1683]. Fermionic atoms are isotopes with an odd number of neutrons so that their total nucleus and electron spin is half-integer. Fermionic quantum computing was defined by Sergey B. Bravyi and Alexei Yu. Kitaev in 2000 [1678].

In 2008, Liang Fu and C.L. Kane from the University of Pennsylvania predicted that Majorana bound states (MBS) can appear at the interface between topological insulators and superconductors [1684, 1685].

In 2012, Leo Kouwenhoven then at TU Delft announced the detection of Majorana Zero Modes quasiparticles at TU Delft and later on in 2018 when he was at Microsoft Research in Delft.

Some other advances came out in 2016 from MIT and in 2017, from a group of three American universities UC Irvine, UCLA and Stanford, who said they discovered real Majorana fermions, a claim that was later retracted (see below). In May 2019, American and German researchers from Harvard and Universität Würzburg said they succeeded in creating two-dimensional topological phenomena like Majorana zero modes in phase-controlled Josephson junctions, along with a companion paper from Copenhagen, Microsoft and Purdue [1686, 1687]. Princeton researchers also published in June 2019 the results of their work that led them to observe a Majorana zero mode in a topologically protected edge channel [1688] (Figure 173).

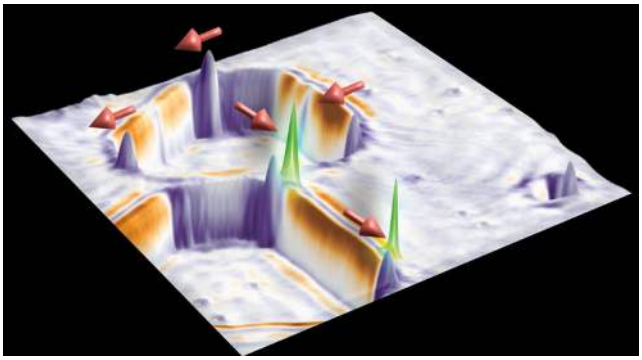

Figure 173: A Majorana Zero mode discovered at Princeton in 2019. Sources: [1688, 1689].

2021 marked the beginning of a crisis winter for Majorana fermions. It started with an expression of concern and a withdrawal of Leo Kouwenhoven's 2018 Nature paper [1690–1692]. In 2022, another paper from Kouwenhoven was retracted [1693]. In a March 2022 Twitter thread Sergey Frolov made an impressive inventory on many other unreliable Majorana research papers with other retracted papers or that should be retracted [1692]. He questioned one paper of Charles M. Marcus published in Science in 2020 [1694], which drove the publication of an editorial expression of concern in 2021, which was finally lifted in August 2025 after a publication of an erratum on the article by its authors [1695]. Leo Kouwenhoven published a perspective on Majorana fermions in which he tells the story [1696].

Another Majorana fermion paper, from researchers in California, Florida and China, and published in Science in 2017, was retracted in 2021 [1697, 1698] with the following comment from the journal editorial board: "*Readers who failed to reproduce the findings requested raw data files from the authors, which they provided. Subsequently, the provenance of the raw data came into question; additionally, an analysis of the raw and published data revealed serious irregularities and discrepancies*".

Sergey Frolov used to work at TU Delft with Leo Kouwenhoven on Majorana fermions and moved in 2012 to the University of Pittsburgh. The withdrawal came after Sergey Frolov and his former Delft colleague Vincent Mourik, now at Forschungszentrum Jülich, unsuccessfully tried to reproduce Kouwenhoven's experiment [1699, 1700]. Leo Kouwenhoven left Microsoft in March 2022. Charlie Marcus from Microsoft Research in Denmark also quit Microsoft late 2021 to return to academic research at the Niels Bohr Institute. Another QuTech team along with researchers from Purdue University (which collaborates with Microsoft) found in 2023 a way to create a two-sites quantum dots based Kitaev chain to engineer Majorana bound states [1701].

Sergey Frolov also co-authored a proposal to braid Majorana bound states using the 4π Majorana-Josephson effect combined with a fluxonium superconducting qubit, the ensemble being branded a braidonium [1702]. He also published in 2022 a deliberately satirical paper showing that, by selecting a handful of traces out of the roughly 4,000 datasets of his own 2012 experiment, one could "discover" a quantized $2e^2/h$ zero-bias peak and a gap closing and re-opening. The supplementary information then dismantles both, the point being to expose how much data selection drives Majorana claims in the literature [1703].

Other researchers in Germany succeeded in integrating a topological insulator into a superconducting qubit in 2022, following on a 2013 proposal from researchers from Caltech and Harvard [1704]. Another 2020 proposal is to couple a Majorana qubit playing the role of a well-protected quantum memory and a superconducting qubit for computation and to implement a SWAP gate between these [1705].

In August 2019, NIST physicists led by Nick Butch announced the accidental discovery of interesting properties of uranium ditelluride (UTe_2). It would be superconducting at about 1.6-1.7 K with the ability to do so via Cooper pairs with identical spins in addition to opposite spins, allowing three types of pairs. This would give it a rare ability to get magnetic flux resistant superconductivity. This material would thus have topological properties in this framework allowing to create topological qubits that are more stable and less subject to decoherence [1706, 1707]. Related work was published by researchers from Johns Hopkins University in 2018 who observed half-quantum flux in the β-Bi_2Pd superconductor, a signature of the spin-triplet pairing that could host Majorana modes [1708]. And the story goes on and on around Majorana fermions that are discovered, believed to be discovered or rediscovered depending on the case. Most of the time, the discoveries deal with very weak experimental signals that can be confused with ambient noise.

1.6.2 Science

The principle of topological quantum computing is based on the notion of anyon which are "quasiparticles" integrated in two-dimensional systems, given that there are Abelian and non-Abelian anyons! Anyons are point-like excitations that exist only in two dimensions, where exchanging two of them multiplies the state by an arbitrary phase (Abelian anyons) or applies a unitary rotation inside a degenerate subspace (non-Abelian anyons), instead of the $+1$ and -1 of bosons and fermions in 3D. This makes it possible to apply some topology principles with sets of successive permutations applied to pairs of anyons that are in proximity in circuits (Figure 175) [1723].

The related algorithms are based on the concepts of topological braid or node organizations ("braids") [1724]. Their representation explains this, with a temporal evolution of the permutations of temporal anyons going from bottom to top, knowing that in other representations, it may go from top to bottom. Topological qubits could also be realized in photonics-based architecture [1725].

The diagram in Figure 176 clarifies this a little. Topological quantum gates require a long sequence of anyonic permutations as with the CNOT gate shown at the bottom of the diagram. They are a sort of quantum error correction code.

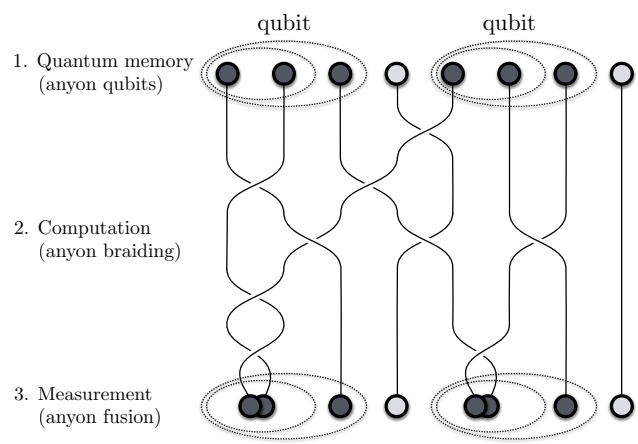

Figure 175: Anyon braiding explained topologically. Source: [1726], 2018.

You need two Majorana fermions to create a single two-level quantum system, *aka* a qubit. With Majorana modes, you implement XX, YY and ZZ two-qubit measurements which are well protected, and a CNOT is assembled from a sequence of such joint measurements combined with single-qubit measurements on an ancilla (Figure 178). But a T gate is not natively protected making it hard to implement FTQC. Some researchers in China still found a workaround, deriving topological $\pi/10$ and $2\pi/5$ phase gates from the braiding of Fibonacci anyons extracted from strongly correlated Majorana edge modes, which together can stand in for the missing $\pi/8$ gate [1712].

topological key takeaways

highlights

- **theoretically very stable qubits**: with a low level of required error correction [1709].
- **long coherence time and gate speed**: enabling the processing of complex and deep algorithms [1710].
- **potential qubits scalability**: built with technologies close to electron spin qubits.
- **simpler qubit drive**: using DC currents and simple microwave pulses, more scalable and less energy consuming.
- other work in the **topological matter field** could be fruitful with no Majorana fermions [1711].

challenges

- topological qubits programming is different and requires an additional software layer.
- hard to build a full universal gate set, as the T gate or Toffoli gate is not natively protected [1712].
- rather few laboratories are involved in this path.
- Microsoft is the only significant vendor, with superconducting nanowire Majorana fermions, but questionable research practices and retracted papers [1693, 1713].
- works at low cryogenic temperatures like superconducting qubits, around 15 mK to 50 mK [1714].
- no Majorana topological qubit has been demonstrated yet [1715].

variations

- **Braidonium**, based on a fluxonium superconducting qubit [1702].
- **uranium ditelluride** qubits (UTe_2), 2D graphene and gold [1707, 1716].
- **alpha ruthenium trichloride** (α-$RuCl_3$) qubits [1717, 1718].
- **Majorana Edge Modes** (MEM) and Majorana Pi Modes (MPM) [1719].
- **other non-Abelian anyons**: Ising anyons, Fibonacci anyons and Jones-Kauffman anyons [1720, 1721].

path to scalability

- **start with making one working qubit**, then two, then a universal gate set along an FTQC staged roadmap [1722].
- **scale control electronics**, preferably cryo-CMOS or SFQ.
- **scale III-V and heterostructures chip manufacturing**.
- **integrated qubit drive and qubits**.

Figure 174: Highlights, challenges, variations and path to scalability of topological qubits. © Olivier Ezratty, 2022-2026.

By the way, let's clarify a little bit the weird vocabulary from this field. What condensed-matter physicists call Majorana fermions are zero-energy bound states that behave as non-Abelian Ising anyons, unlike the genuine Majorana fermion of particle physics which is an ordinary fermion. They are also called Majorana Zero Modes (MZM) or Majorana bound states or even Majorinos. You have also Majorana Edge Modes (MEM) and Majorana Pi Modes (MPM) [1719]. Other non-Abelian anyons exist like Ising anyons [1720], Fibonacci anyons [1721], Jones-Kauffman anyons, and anyons from the non-Abelian gauge groups such as S_3 (a finite non-Abelian group that contains six elements representing the possible permutations of three distinct items) [1727].

Majorana fermions are developed in various materials and heterostructures which are hard to differentiate at this point:

- On the surface of superconducting nanowires, particularly in Denmark and with Microsoft [1694, 1728].
- In heterostructures with different magnetic materials in the USA and China [1729–1731].
- On Dirac–Weyl semimetals [1732].
- On gold, mostly in the USA [1733, 1734].
- In 2D graphene, in Spain and France [1716].
- With α-$RuCl_3$ (alpha ruthenium trichloride) in Japan, which is a potential Kitaev quantum spin liquid [1717, 1718].
- In α-BiPd (alpha-Bismuth Palladium) crystals, in the USA [1735, 1736].
- On $MoTe_2$ (molybdenum ditelluride), also in the USA [1737].
- On superconducting topological crystalline insulator SnTe (tin telluride) [1738].
- In NV centers, as studied in China [1739].
- Even with photons, also investigated in China [1740].

1.6.3 Qubit operations

Let's try to explain how Majorana qubits work on a practical basis, given there are many variations of these.

- **Qubit quantum state** involves a Majorana code also called a Majorana box qubit or Majorana qubit. Correction is partially built in with a Majorana stabilizer code forming the even-fermion-parity ground-state subspace of two parallel Kitaev Majorana chains in their fermionic topological phase. An extension using three nanowires carrying six MZMs at fixed total parity is called the "hexon" Majorana code, and it houses one computational qubit plus ancillary states used to run the measurement-based operations. The proposed circuit in Figure 177 shows superconducting islands containing six MZMs ("hexons") connected together with superconducting topological nanowires, given Microsoft is using four MZMs ("tetrons") [1741].

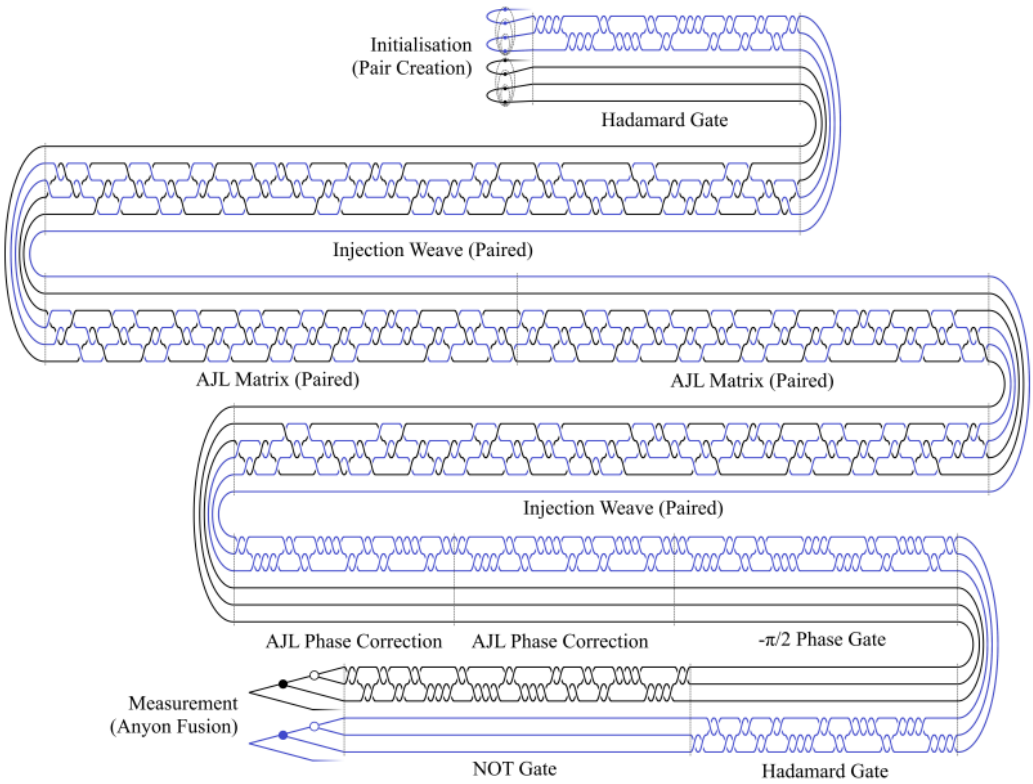

Figure 176: How topological quantum computing is supposed to work to generate gates until the last measurement. Source: [1726], 2018.

- **Single-qubit quantum gates** operations can be driven between the MZMs and semiconducting quantum dots as with the example shown in Figure 177. An H gate can be implemented with an X measurement following by a Z rotation conditioned by the result of the X measurement. In a way, it looks like a form of measurement based quantum computing (MBQC). But this can't work in a NISQ fashion since measurement-based computing requires error correction. In a way, this kind of qubit is bound to be implemented in a FTQC fashion.

- **Two-qubit quantum gates** like a regular CNOT are created with combinations of single Pauli X and Z measurement with XX and ZZ joint measurement between qubits as shown in Figure 178. A T or Toffoli gate in the non-Clifford gates group must be created to achieve universality.

- **Qubit readout** is done to implement any single or two-qubit gate. It uses projective measurement using charge sensing [1743]. It can leverage a cryo-CMOS chip, as with the Gooseberry controller tested by Microsoft with the University of Sydney, which operates at 100 mK next to the qubits and is paired with a general-purpose cryo-compute core running at about 2 K, the pair being designed to drive thousands of qubits [1744]. You can measure only half the qubits at a given time.

- **Error correction**. Majorana have embedded error correction enabling them to potentially reach gate "measurement" fidelities in the 10^{-6} error zone according to Microsoft. Still, error correction codes are required to run all logical gates, and in particular, to implement non-Clifford quantum gates which are not native with Majorana fermions. The planned quantum error correction codes are Floquet codes, a variant of surface codes, and then, qLDPC codes. Other ways to create logical qubits with topological qubits are investigated at Maryland University [1745–1748].

1.6.4 Research

On top of the above-mentioned labs, different physics laboratories are working on topological qubits, notably in the USA, China, Germany [1749], the UK, the Netherlands, Denmark, Australia [1750], Japan [1751, 1752], Finland [1753, 1754], Switzerland [1755], even Saudi Arabia [1756], and also in France.

Maryland [1757, 1758], **Caltech** [1759], **Wisconsin Madison** [1760], **UCSB** [1761], and **Purdue** [1762] Universities also have teams working on topological quantum computing and/or Majorana fermions, the latter two working with Microsoft Research. It is also the case of the Quantum Science Center (QSC) from the DoE **ORNL**, the Air Force Institute of Technology [1763], as well as the **Sandia Labs** [1764, 1765] and

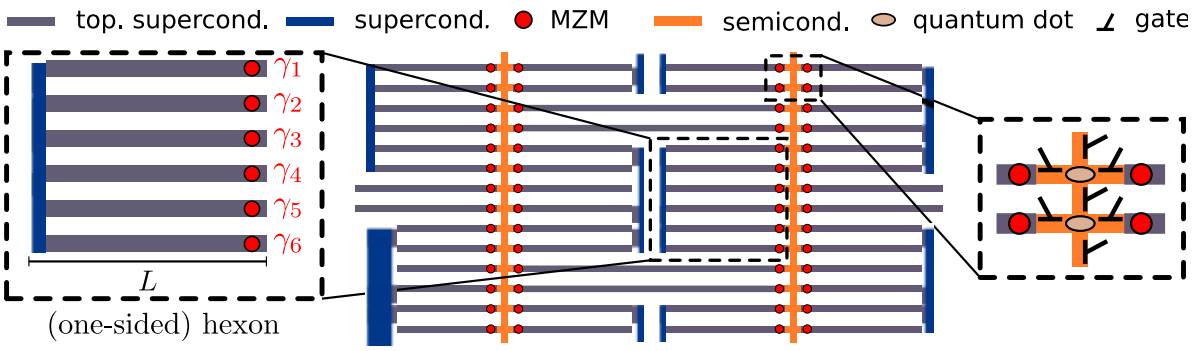

Figure 177: Example of Majorana fermion encoded with 6 MZM connected to topological superconductor nanowires, aka "hexons". Source: [1741]. Added in 2023.

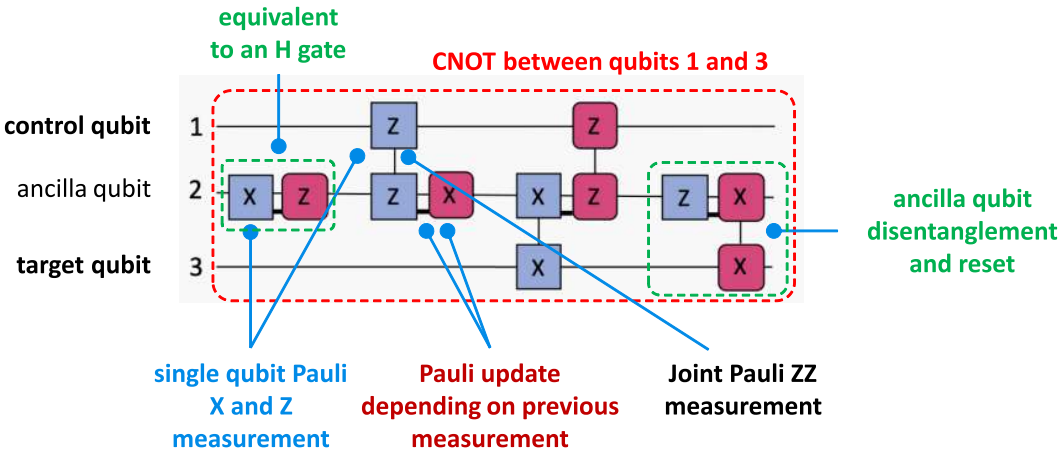

Figure 178: Explanation of the complicated way to implement a CNOT entanglement gate with Majorana fermions. Source: [1742].

AFRL [1766]. The KouBit Lab from the **University of Illinois** and led by Angela Kou also investigates topologically protected superconducting qubits as well as a team led by Javad Shabani at the **New York University**. Researchers from **Cambridge University** are proposing to create NISQ QPUs with topological qubits [1767].

Even IBM is working on Majorana fermions. In 2022, an **IBM Research** team published a paper showing how they could simulate Majorana Zero Modes (MZM), Majorana Pi Modes (MPM) and Majorana braiding on 27-qubit quantum computers [1768]. This type of fundamental research on Majorana based error correction codes was still going on as of 2026 [1769].

A large **Google AI** team did a similar experiment with 47 qubits from its Sycamore processor and simulating Majorana Edge Modes [1061]. A team led by the **Flatiron Institute** emulated MZM on ten ytterbium trapped ions [1770].

Teams in **Finland** and **Russia** also work on topological qubits or effects [1771] as well as in **Sweden** [1772, 1773], **Innsbruck** [1774, 1775] and in **Australia** [1776–1778].

Research on topological qubits still goes on at **TU Delft** with some recent work on the way to stabilize entanglement of topological qubits [1779, 1780]. Leo Kouwenhoven is still involved here [1781].

In **France**, a team at the CEA-IRIG in Grenoble (Julia Meyer, Moïra Hocevar, Edith Bellet-Amalric), Pierre Mallet of CNRS Institut Néel in Grenoble, Hugues Pothier at the CEA in Saclay and Pascal Simon at the LPS in Orsay [1782] do work on Majorana fermions and on various topological matter, particularly on Andreev's states, the linked states and the physics of weak links, different areas that remain to be explored in these lines. Some of these researchers are conducting joint projects with TU Delft. Marko J. Rančić, formerly from TotalEnergies, is also exploring the field by generating MZM out of noisy qubits [1783].

Majorana zero modes (MZMs) were also found by researchers in **China** in 2022 with iron-based superconductors showcasing topological vertices [1784–1788].

We cover in this part only the physical topological qubits like Majorana fermions not the topological error correction codes implemented with other types of qubits like superconducting qubits and trapped ions [1789].

1.6.5 Vendors

Microsoft

USA, 1975

Microsoft Research has investigated topological quantum computing and Majorana fermions for quite a few years. The company is making a bet there, up to saying that "*if they fail, everybody will also fail in quantum computing*". While being a little arrogant and a very risky bet, it would bring lots of strategic advantages if it worked! Indeed, Majorana qubits would be much more reliable and generate fewer errors, with the implication that we could avoid using some of the classical quantum error correction codes that are implemented with other types of qubits [1790–1792].

Beginnings. **Michael Freedman**, who received the Fields Medal in 1986 for his proof of the four-dimensional Poincaré conjecture, joined Microsoft in 1997, coming from the University of California San Diego. He demonstrated with Alexei Kitaev the possibility of implementing quantum computing with a hypothetical particle, the Majorana fermion, conceptualized in 1937 by Ettore Majorana [1793]. This fermion is a strange particle, whose charge and energy are zero and which is its own antiparticle. Freedman and Kitaev were hired by Microsoft Research. Microsoft Quantum Santa Barbara (Station Q), created by Michael Freedman in 2005, is located on the campus of the UCSB (University of California Santa Barbara). They were complemented by **Leo Kouwenhoven**'s team based in Microsoft's Delft Lab in the Netherlands and with **Charles Marcus** from the Niels Bohr Institute who also joined Microsoft Research. They both left Microsoft in 2022 and 2021. Microsoft also collaborates with **Purdue University** in Indiana, where its dedicated research team **Microsoft Quantum Purdue** works on III-V superconductors [1794].

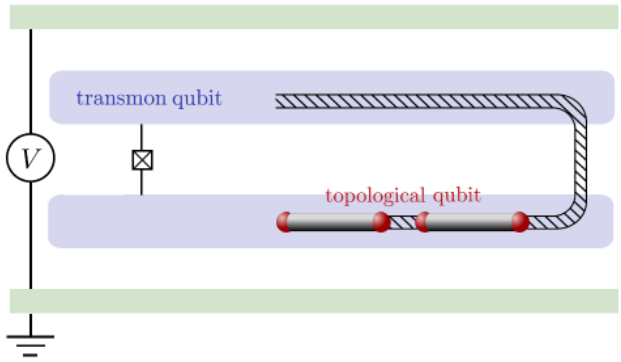

Figure 179: Typical combination of a topological and a superconducting qubit. Source: [1714].

Majorana fermions are strange behaviors of electrons and their spin that are found at both ends of superconducting wires. They operate at very low temperatures, as for superconducting and silicon-based qubits, at about 15-20 mK [1714]. Seen up close, these qubits are sophisticated variants of superconducting qubits (Figure 179). These "topological" mesh associations provide protection against qubit decoherence because the shape of the braids does not matter as long as their topology is stable (Figure 180).

Microsoft announced at the Build conference in May 2018 that they would release their first fermion-based quantum computer from Majorana in 2023 [1795]. After the retraction of Leo Kouwenhoven's 2018 Nature paper in 2021, this planning seemed somewhat compromised.

In 2022, as Leo Kouwenhoven was leaving Microsoft, the company published some new results related to Majorana fermions and scalable quantum computing. It dealt with the observation of a 30 μeV topological gap in indium arsenide-aluminum heterostructures. But no qubit was demonstrated at that stage. The result was a materials and transport characterization claimed to pass the topological gap protocol, with the qubit architecture existing only on paper and in simulation [1796–1798]. Just before, in February 2022, another Microsoft team published a paper related to a quantum error correction code (planar Floquet code) that was suitable for topological qubits and with a threshold in the 1% range [1799]. This is comparable to the circuit-level threshold of the surface code, which also sits between 0.5% and 1%. What matters in practice is the operating point: useful logical error rates require physical error rates about ten times below threshold, hence the sub-0.1% target usually quoted for superconducting qubits.

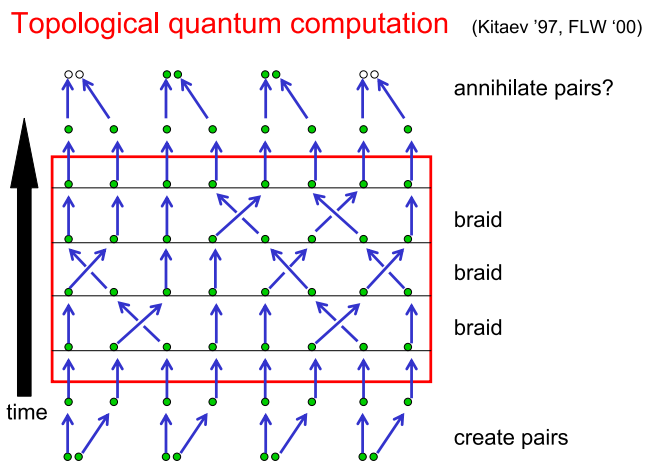

Figure 180: how braiding is sequenced during topological computing. Source: [1800].

Between November 2022 and June 2023, Microsoft upped again the ante with publishing a paper on the discovery of Majorana zero modes (MZM), discussing a lot about the topological gap protocol (TGP) used to detect a topological phase [1802–1805] (Figure 183). Microsoft announced that its Majorana Zero Mode qubits could have fidelities in the 6-nines range, meaning errors around 10^{-6}.

But again and again, the results were contested. This paper was first submitted to PRX Quantum and rejected by their referees. The paper was then submitted

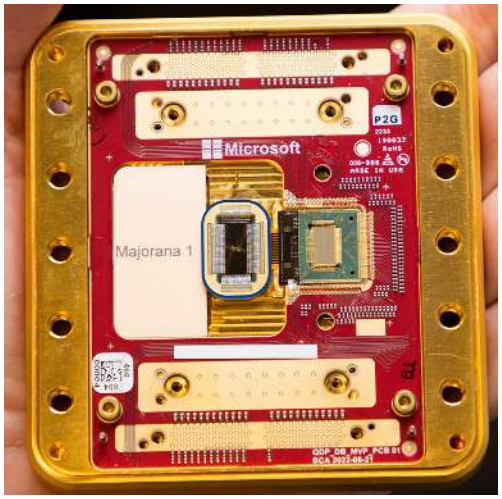

Figure 181: Microsoft's Majorana 1 processor containing their first MZM chip (on the left). The device reports transport and parity measurements rather than a topologically protected computational qubit or any logical-qubit operation, which is why it is described as half a qubit here. and its companion cryo-CMOS control chip (on the right) which seems to contain the (bulky) resonator used to run charge detection on the quantum dot in the half-qubit chip. Source: Microsoft, February 2025.

Figure 182: Microsoft's Majorana-2 processor hosting two qubits (on the left), with its companion cryo-CMOS drive chip (on the right). Comparatively, the MZM chip is much larger while the cryo-CMOS chip has about the sale size. Source: Microsoft, June 2026 [1801].

to PRB with different referees who accepted it although, with some reserves on the lack of experimental data [1806]. Sergey Frolov tweet explained that "*Physical review editors are lying. They manipulated peer review to go around our comments. 1 year ago PRX reached out to @VincentMourik and got a full run down on this paper. It got Rejected. Then PRB took it... But it is the same editors!*". According to that account, the manuscript was rejected by PRX Quantum and was subsequently published in Physical Review B. This review history rests on a single public statement by one of the critics and is not otherwise documented. Another preprint was published in April 2024 on the detection of some MZM in a different circuit design [1807]. In 2026, Sergey Frolov et al. proposed in Science to share experimental data to create a scientifically trustable environment around topological qubits [1713].

First qubits, or so. Then came Microsoft's February 2025 announcement of the realization of the first Majorana-based qubit with a blog post from Chetan Nayak, their chief hardware scientist who has worked in the domain for three decades now [1709, 1808], a blueprint containing a technology roadmap [1722] Figure 184 and the peer-reviewed version of the 2024 paper [1807]. It sparked yet another controversy [1809], fueled by physicists like Vincent Mourik, Sergei Frolov, and Henry Legg who published an arXiv in 2025 and a Nature paper in 2026 to refute Microsoft's claim [1715, 1810] and who was commenting on another Microsoft paper [1802]. Even the referees from the Nature paper were negative. Two out of four rejected the paper and one was conflicted, being the main author of the past retracted 2018 Nature paper. The dispute circles around many questions: did Microsoft really create a topological qubit? Is the TGP that they use to characterize it valid? Do they have a confirmation bias when analyzing their experimental data?

Microsoft did showcase a chip on a chiplet supposed to host a full Majorana-based qubit, a tetron made with 4 MZMs corresponding to the lower left of Figure 184, although their communication was confusing since they inferred that they already had an 8-qubit chip. Microsoft also predicted that (their) useful quantum computers were just years away and would soon support a million physical qubits and thousands of logical qubits. I detailed all this in a long technical post in March 2025 [1811].

The "Majorana 1" is manufactured using III/V techniques (Figure 181). The companion cryo-CMOS chip contains a resonator for the qubit readout and some digital electronic circuitry to drive the whole thing.

It showcases some interconnect wiring between the two chips and connecting the resonator chip to outside electronic components. This chiplet operates at 50 mK. It has a similar size than most quantum chips like the one you have in superconducting qubit quantum computers. You then still need a cryostat with a dilution, control electronics and cabling, including room temperature electronics, which occupies several cubic meters in a dedicated room. Viewed from the outside, a Microsoft quantum computer will look like an IQM or Rigetti QPU, or, more closely, a silicon-qubit system.

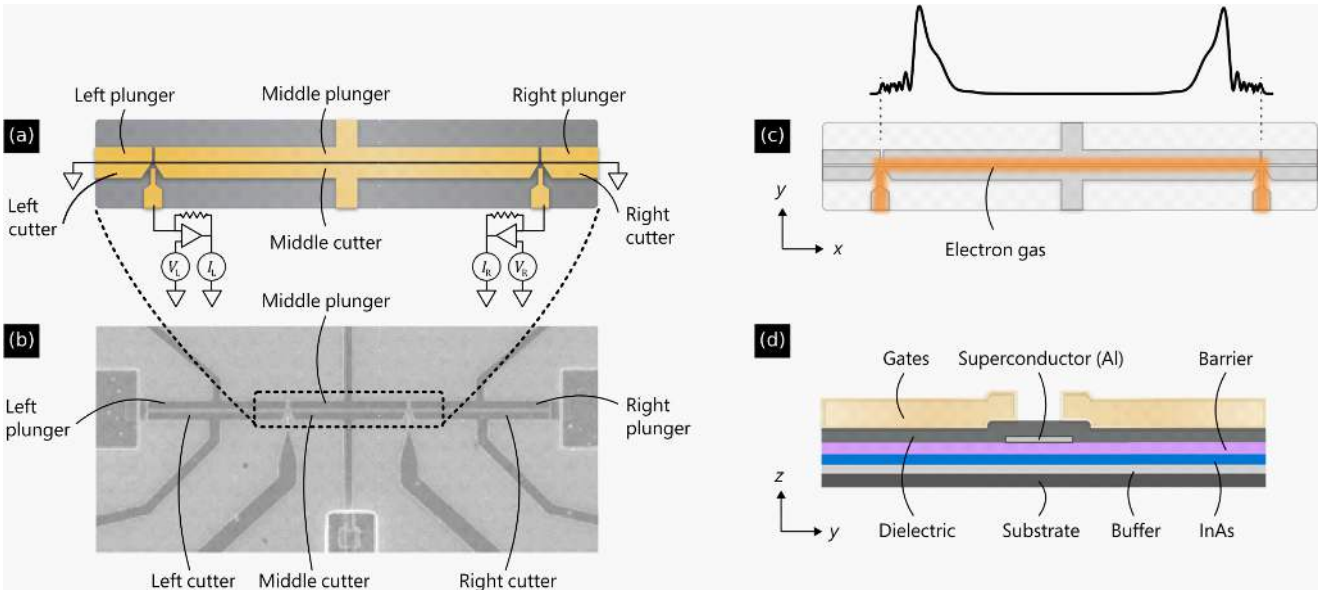

Figure 183: Microsoft's iteration of a MZM, published in 2023. Source: [1802].

Qubits control doesn't need AWGs (arbitrary wave generators). Control relies mostly on digital pulses. The measurement pulse duration seems to have a lower bound of 1 ns, with a planned length of 10 ns, which is in line with the best single qubit gate time with superconducting qubits. Measurement uses an amplifier operating at the quantum limit (a TWPA like the one that are used with superconducting qubits), then a HEMT secondary amplifier operated at 4K (same) and, at last, a room temperature amplifier completes the picture.

A Microsoft topological qubit has a size of $5\,\mu$m $\times$ $3\,\mu$m. They are manufactured with indium, arsenide and aluminum heterostructures, on InP (indium phosphide) III-V wafers. It also uses hafnium, titanium, aluminum and gold for the creation of various gates. Microsoft says that its chip design could accommodate a million qubits, but it doesn't say if this includes the resonator chip. We can also suspect that the resonator chip is built using a more traditional technology, either on silicon or sapphire (aluminum oxide), like with most superconducting qubits and electronic chips.

One looming question for the future is: can III-V manufacturing scale? The prototype Majorana test chips are currently manufactured in Microsoft's own cleanroom in Santa Barbara, California. But some part of the fabrication is also done in Delft as well as in Lyngby near Copenhagen. Most of the traditional III-V commercial products in photonics and RF signals handling have only a few electronic elements, and their tiny chips are glued on silicon chips in so-called heterostructures. Nobody has ever manufactured any III-V chip with thousands of elements, let alone several millions of elements like what Microsoft is planning for the realization of a million-qubit monolithic chiplet. And there are no industry-grade large scale manufacturing plants for this. Also, Microsoft's chip design is highly complex, merging difficulties usually found with manufacturing superconducting qubits (for their MZM nanowires), with silicon qubits (for the quantum dots used in measurement), with cryo-electronics (with their resonators), with cabling at the chip level (which is already incredibly complicated for a single physical qubit). So, there's a huge uncertainty here with scaling this technology and maintaining high manufacturing quality, high yield and low variability across large chips. It will probably need many long years at best.

In July 2025, Microsoft's team published another preprint with X and Z measurement results on their qubit [1812]. It did show that their Z-parity measurements on a single nanowire are stable with 12.4 ms lifetimes, showcasing well-isolated Majorana modes. But their X-parity measurements across two nanowires show stabilities of just 14.5 μs, with 16% operational errors which is far from what is needed [1813]. They still have a lot on their plate to demonstrate functional Majorana qubits! And a third party June 2025 preprint exposed why Majorana fermions were potentially subject to some fundamental detrimental 1/f noise [1814]. All in all, the conclusion is that Microsoft may be on some right track but, at this point in time, they are clearly overselling what they have on their plate. Unfortunately, too many media drank the koolaid [1815, 1816].

On June 2, 2026, at its Build conference, Microsoft presented Majorana 2, its second-generation topological quantum chip [1710, 1801]. The device is a prototype four-tetron unit cell for a larger array, with neighboring tetrons coupled through shared quantum dots, each tetron carrying four MZMs and encoding one qubit. Beyond replacing aluminum by lead, Microsoft also moved from InP to a GaSb substrate and to a composite InAs/InAsSb quantum well, which they say more than doubles the topological gap. They report a 1,000-fold improvement in parity stability, with a mean lifetime of

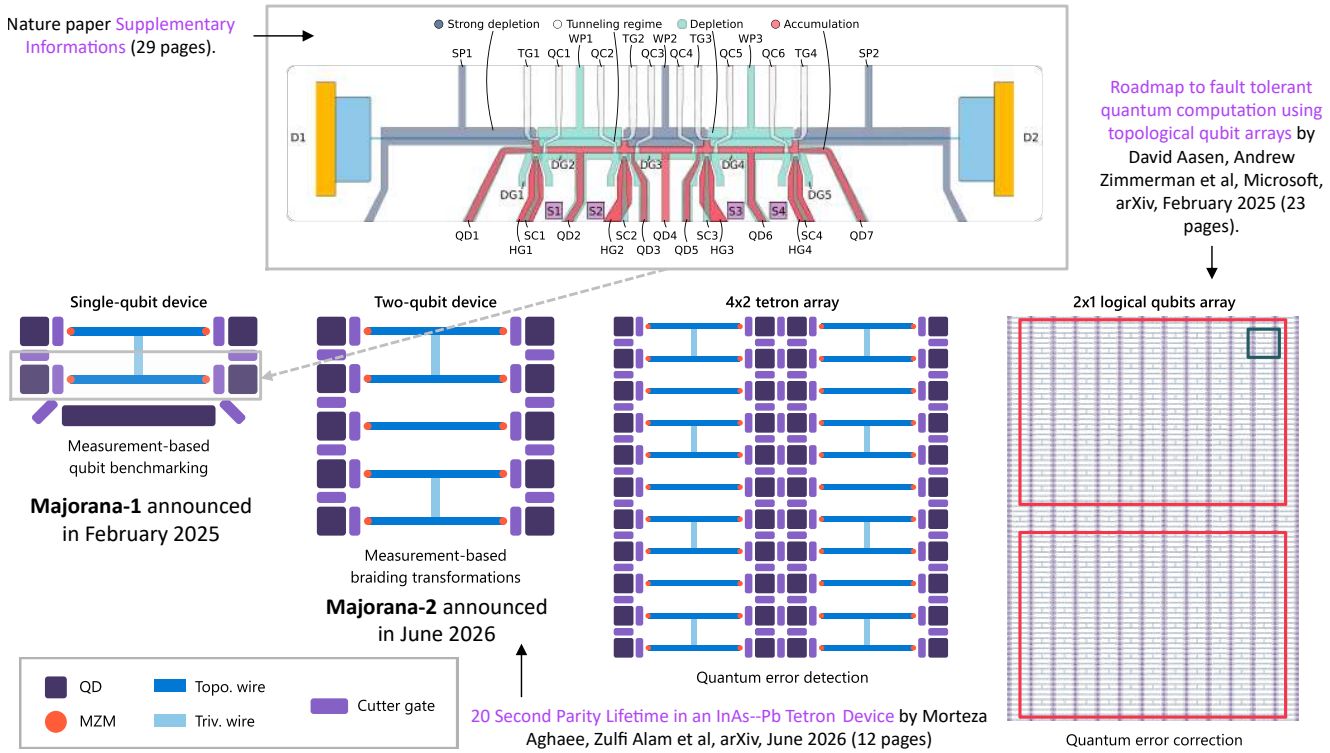

Figure 184: Microsoft first Majorana qubits are made with four MZMs, with a group of two MZMs represented at the top. Microsoft's 2025 roadmap planned to create a first 2-qubit chip made with 10 MZMs to test braiding operations, then an 8-qubit array to test error correction, then a much larger chip with full-fledged error correction containing 371 physical qubits and two logical qubits of 13×13 qubits assembled with a distance 7 surface code. Much later, a 1 million qubit chip will deliver practical computing capabilities. The Majorana-2 device presented in June 2026 is a step toward this two-qubit milestone, though the published measurements were performed on a single tetron of a four-tetron unit cell. Sources: [1807] supplemental materials and [1722], and [1710, 1801] for the Majorana 2 milestone.

20 seconds and some events lasting up to a minute. The caveat is that the rf spectroscopy and the 20 s lifetime were measured on a single nanowire of one grounded tetron, not on the unit cell operated as a multi-qubit processor. The chip was manufactured in Microsoft Lyngby's cleanroom in Denmark, North of Copenhagen. The material switch was chosen with the help of Microsoft Discovery's agentic AI. Microsoft said it expected to create a scalable FTQC computer by 2029, half the 2033 horizon it was quoting a year earlier, which is quite ambitious.

Software. Microsoft obviously also invested on software development, first with its Liquid platform, then with F# for scripting and with the Q# language used for quantum programming, launched at the end of 2017. One of the contributors to these efforts is researcher **Krysta Svore** from Columbia University. In 2018, Microsoft recruited a certain **Helmut Katzgraber**, one of the apostles of D-Wave quantum annealing and MBQC (measurement-based quantum computers) [1817]. He now works at AWS.

Since 2023, DARPA is funding Microsoft's research on Majorana fermion large scale quantum computing as part of its Underexplored Systems for Utility-Scale Quantum Computing (US2QC) program, selected alongside Atom Computing and PsiQuantum. Microsoft moved on to the second phase at the end of 2023 [1818], and in February 2025 it was selected, with PsiQuantum, for the third and final Validation and Co-Design phase, US2QC having been folded into DARPA's broader Quantum Benchmarking Initiative.

Quoherent

USA, 2021, $6.2M

Quoherent wants to create a portable quantum computer using topological insulators, and operating at room temperature.

Its three co-founders are Roberto DiSalvo (CEO), Alton Reich (COO) and David Carroll (CTO), the latter a quantum materials physicist and the Director of the Center for Nanotechnology and Molecular Materials at Wake Forest University in North Carolina, where the underlying research was conducted. The startup has not released any public roadmap.

Nokia

Finland-USA, 1871

Nokia's Bell Labs in the USA, located in Murray Hill, New Jersey, also works on the design of topological qubits at the fundamental research level, in Robert Willett's team [1819]. Willett participated in the discovery of the 5/2 fractional quantum Hall (FQH) state [1820]

and in the first experimental signatures of a non-Abelian state in 2010 [1821], then in 2023 in the interferometric demonstration of the non-Abelian braiding statistics of charge-$e/4$ quasiparticles at filling factors 5/2 and 7/2 [1711]. These are Ising-type anyons, which are not universal on their own, and not the Fibonacci anyons that would be expected at 12/5.

They are working on ultra-pure gallium arsenide quantum wells using the Fractional Quantum Hall Effect, and operating at <100 mK and under magnetic fields over 1 tesla. It manipulates fractional electrical charges in a 2D electron liquid. The components are manufactured using MBE (Molecular Beam Epitaxy) [1822].

Nokia also supports Oxford University's Quopal initiative on the use of quantum in machine learning. Nokia likes to remind us that Grover and Shor's algorithms were discovered by their creators when they worked at the Bell Labs.

Nokia also develops quantum cryptography technologies, at least at the level of its transport on optical fibers, as demonstrated by a partnership with SK Telecom of 2017.

There is even a private research company, **Quantum Gravity Research** (2009, USA) with an overarching goal to create a unified physics theory encompassing gravity and quantum physics that also undertakes research in topological computing [1823].

The organization created by Klee Irwin employs about 20 researchers like Fang Fang, Raymond Aschheim, Marcelo Amaral, Dugan Hammock, Richard Clawson and Michel Planat. They envision "*a specific substructure of spacetime at the smallest scale, so that in this view physical reality is like a mosaic tiling language of Planck scale, 3-dimensional, tetrahedron-shaped pixels*". Let's say it is quite difficult to fact-check these sorts of claims and their practicality!

Quantum Brain (2024, South Korea) is a weird startup that wants to create a topological quantum computer with getting inspirations from some understanding on the way human brains work and using Qransistors to minimize qubit errors using an unspecified topological quantum material. The word Qransistor is not even Googleable and the company has no visible founder! It may be automatically generated by ChatGPT!

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This **Topological qubits** subsection contains 155 bibliographical references and notes containing at least 2,157 pages.

1.7 Trapped ions qubits

Trapped ions are atomic ions confined by electromagnetic fields in ultra-high vacuum. The species used in quantum computing are most often singly ionized alkaline-earth elements such as Be^+, Mg^+, Ca^+, Sr^+ and Ba^+, and the lanthanide Yb^+, with less-common historical work on group-12 ions such as Cd^+ and Hg^+ [1824, 1825].

1.7.1 History

Before the very notion of a qubit even existed, scientists developed electromagnetic traps for charged particles. **Wolfgang Paul** developed radio-frequency quadrupole mass filters and ion traps in the 1950s, with the first three-dimensional Paul traps realized around 1954-1955. He received the Nobel Prize in Physics in 1989. The **Penning trap** combines a static electric quadrupole field with a static magnetic field and grew from Frans Penning's magnetron work and Hans Dehmelt's precision-trapping developments. Dehmelt built a high-vacuum magnetron/Penning trap in 1959, while the first isolated single electron in such a trap was achieved in 1973.

In the USA, **David Wineland** and collaborators pioneered laser cooling of trapped ions. In 1989, Fred Diedrich, John C. Bergquist, Wayne M. Itano and Wineland used resolved-sideband cooling to prepare a single $^{198}Hg^+$ ion in its motional ground state with about 95% probability [1826]. Wineland received the Nobel Prize in Physics in 2012 along with Serge Haroche.

Peter Zoller and **Juan Ignacio Cirac** from the University of Innsbruck in Austria proposed in 1995 a blueprint to create a gate-based quantum processor with a linear trap of ions controlled by laser beams [1827, 1828]. Along with **Rainer Blatt**, they initiated a long-lasting experience in the field at Innsbruck, which led to the creation of the startup **AQT** in 2017.

1.7.2 Science

Here are some specifics of trapped ions qubits…(Figure 187).

Why ions? Ions of a given isotope are intrinsically identical, which removes the fabrication-induced qubit-frequency dispersion found in many solid-state modalities. Device variability remains in the trapping fields, stray electric and magnetic fields, lasers, microwave and RF control, motional modes and readout. Qubits are encoded in two selected long-lived internal states, typically Zeeman or hyperfine sublevels of the electronic ground state or a metastable optical state. Separate short-lived cycling transitions are generally used for Doppler cooling and fluorescence readout. Mixed-species ion crystals can combine complementary properties, for example one species for computation and another for sympathetic cooling or transport [1829, 1830].

Long coherence time. Trapped-ion coherence depends mainly on the qubit encoding and magnetic-noise protection. As a high-fidelity laboratory benchmark, a $^{43}Ca^+$ hyperfine clock qubit showed $T_2 \approx 70$ s with single-qubit gate times from 4.4 to 35 μs, corresponding to a coherence-to-gate-time ratio of roughly 2×10^6 to 1.6×10^7 [1831]. Cross-platform ratios should be compared with caution since coherence definitions, gate types and operating points differ a lot.

Qubit fidelities. Trapped ions have reached exceptionally low single-qubit gate errors. Smith et al. reported a minimum error per Clifford of $1.5(4) \times 10^{-7}$ in a $^{43}Ca^+$ clock qubit, corresponding nominally to 99.999985% Clifford fidelity, in a paper published in 2025 [1831] (Figure 185 and Figure 186). Two-qubit fidelities above 99.9% have also been demonstrated. For example, Quantinuum's 98-qubit Helios processor reported an average two-qubit infidelity of 7.9×10^{-4}, or about 99.921% fidelity [119]. These figures are not directly interchangeable because randomized-benchmarking, gate-set and SPAM metrics probe different error channels.

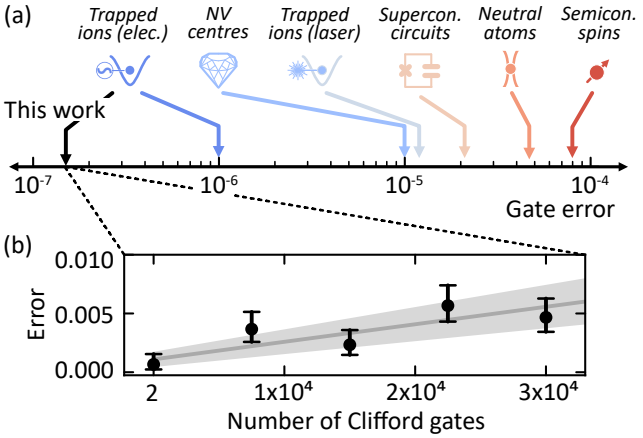
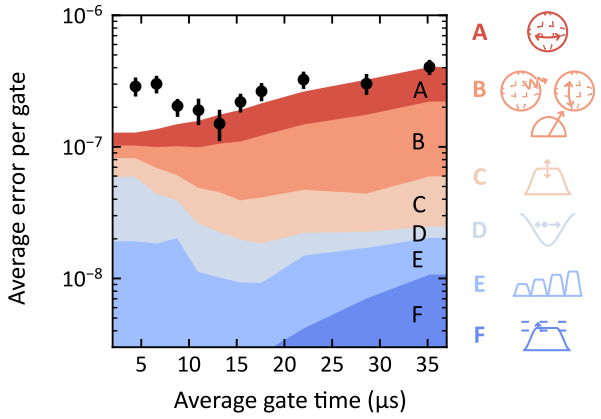


Figure 185: The record single-qubit gate error reported in 2025, compared with representative laboratory results for other qubit modalities. Source: [1831].

SPAM measures the combined errors of state preparation and measurement. IonQ reported 99.96% SPAM fidelity with barium ions in 2022. Quantinuum demonstrated a $^{137}Ba^+$ SPAM infidelity of $(9.0 \pm 1.3) \times 10^{-5}$, corresponding to a fidelity of $99.9910 \pm 0.0013\%$, in a peer-reviewed experiment [1832].

Where are the residual errors coming from? The most frequently mentioned sources are control voltage variability in the case of microwave qubit drive, laser frequency, intensity noise, beam pointing instability and optical waveguides crosstalk for qubit laser drive [28, 29], optical tweezers imprecision [1833], and ions heating.

There are also magnetic-field fluctuations that generate phase noise and are mitigated with shielding, field stabilization, clock-state operation or dynamical decoupling. Additional error sources include collisions and recoil from residual-gas molecules, off-resonant excitation,



Error source	Error ($/10^{-7}$)
A. Decoherence	0.64(7)
B. Leakage, bit-flip and time-dependent measurement	0.62(7)
C. Fast amplitude noise	0.23(2)
D. Harmonic motion	0.13(2)
E. Slow amplitude drift	0.09(7)
ac Zeeman shift calibration	0.03(2)
F. Amplitude resolution	0.015
Excitation of spectator states	<0.01
Inter-pulse Zeeman shift ramping	<0.01
Non-rotating-wave dynamics	<0.001
Expected error per gate	1.7(1)
Measured error per gate	1.5(4)

Figure 186: A decomposition of the error sources for trapped-ion single-qubit gates by researchers from the Universities of Oxford and Osaka. Source: [1831].

spontaneous emission and imperfect state preparation or readout.

Connectivity. Within a linear chain or interaction zone, shared collective motional modes can mediate entangling gates between arbitrary selected ion pairs, giving effective all-to-all connectivity without SWAP routing [1834]. This is a major advantage at modest scale, but the control problem becomes harder as the number of ions and motional modes grows. Gate time and fidelity then depend on the mode spectrum, laser or microwave power, pulse shaping, heating and spectator-mode errors rather than obeying a universal monotonic law. QCCD architectures therefore use smaller interaction zones connected by ion shuttling. Rydberg-mediated ion gates provide another route that can reduce reliance on collective phonon buses, at the cost of demanding UV/VUV control and strong sensitivity of Rydberg states to electric fields.

Interconnect. Trapped ions offer a natural optical interface for modular architectures, but efficient remote entanglement remains experimentally demanding. A 2023 experiment entangled two $^{40}Ca^+$ ions separated by 230 m through 520(2) m of optical fiber with Bell-state fidelity up to 88% and success probability 4×10^{-5} [66]. More recent architecture studies project that remote Bell-pair fidelities around 99.9% could be feasible with improved interfaces and protocols, but this is a target rather than a demonstrated inter-processor two-qubit gate fidelity [105].

Calibration. Ions of the same isotope have identical intrinsic spectra, which removes fabrication-induced qubit-to-qubit parameter spread. The processor still requires substantial calibration of micromotion compensation, secular-mode frequencies, stray electric fields, magnetic fields, laser frequency, phase and intensity, microwave amplitudes, optical addressing, readout thresholds and shuttling waveforms. Drift-tracking and automated calibration therefore remain active research topics [30, 1843, 1844].

Ion variations. There are five main variations of trapped ions being used, depending on the energy transitions applied to manage the two states of a qubit. Each of these modes correspond to different transition frequencies:

- **Zeeman qubits** encode information in magnetic sublevels, typically with splittings in the MHz range. Their transition frequencies are generally first-order sensitive to magnetic-field noise, although high fidelity is can be obtained with stabilization and dynamical decoupling [1845]. Raman-based control of these qubits is also possible [1846].
- **Hyperfine structure qubits** use states split by the interaction between the nuclear spin and the electronic angular momentum, with transition frequencies commonly in the GHz range and control by microwaves or Raman transitions [1847]. Hyperfine structure requires a nucleus with non-zero spin. Even-even nuclei generally have nuclear spin $I = 0$, while odd-mass isotopes often have $I \neq 0$. Thus $^{40}Ca^+$, with 20 protons and 20 neutrons, has $I = 0$ and is commonly used as an optical qubit, whereas $^{43}Ca^+$, with 20 protons and 23 neutrons, has $I = 7/2$ and supports hyperfine clock-qubit encodings. Quantinuum uses hyperfine qubits with laser-driven gates, while IonQ/Oxford Ionics and Universal Quantum also exploit microwave control schemes [1848]. $^{89}Y^+$ has also been proposed as a two-valence-electron trapped-ion qubit [1849].
- **Fine structure qubits** use submillimeter waves of a few THz. These are exotic qubits not used in the commercial world.
- **Optical qubits** use photons of a few hundred THz. AQT is using this type of qubits.
- **Rydberg-ion schemes** transiently excite an ion to a highly excited electronic state to generate strong, controllable interactions. The required wavelengths depend on ion species and excitation path. Experiments include direct VUV excitation near 122 nm in

trapped ions qubits key takeaways

highlights

- **two-qubit gate fidelities above 99.9%** have been demonstrated on trapped-ion platforms, including Quantinuum Helios and Oxford Ionics lineage systems [119, 121].
- **98-qubit gate-based processor** with Quantinuum Helios in 2025 [119]. Larger ion crystals for analog quantum simulation.
- **logical states and logical operations** have crossed selected break-even benchmarks, including logical magic-state and error-corrected demonstrations [120, 1835].
- **high coherence-to-gate-time ratio**, reaching above 10^6 in state-of-the-art single-qubit experiments, could enable larger NISQ circuits [1831].
- **low qubits variability** given the ions are all the same, but variability still exists at the control level (lasers, ion traps).
- **effective all-to-all connectivity within an ion chain or interaction zone**, reducing SWAP overhead [119, 1834].
- **room-temperature or cryogenic operation**: cryogenic traps around 4–20 K can reduce anomalous heating and improve vacuum, but is not intrinsically required [1831, 1836].
- **photonic interconnect** is a natural modular scaling route because trapped ions can interface with photons, although remote-entanglement rates and fidelities remain well below local gate performance [66, 105].

challenges

- **unproven scalability beyond roughly 100 high-fidelity gate-based physical qubits** in a single processor, despite larger analog ion crystals, with candidate routes including QCCD shuttling, 2D architectures, photonic interconnects and micro-Penning traps [25, 26, 119].
- **slow computing** due to long quantum gate times and ions shuttling, which may be problematic for deep algorithms in a FTQC regime despite better many-to-many connectivity at small scale [23].
- **motional-mode crowding and control complexity** increase as interaction zones grow, which can lengthen entangling gates or reduce their fidelity unless pulse design and architecture are adapted [24].
- **global connectivity is now demonstrated at 98 qubits**, but scaling the quality, parallelism and calibration of such connectivity remains challenging [119].
- **control signals variability** across microwave, laser and RF drives [28, 29].
- **anomalous motional heating** remains incompletely understood microscopically, but is substantially mitigated by surface treatment, trap design, larger ion-electrode distance and often cryogenic operation [27, 1837].
- **laser phase noise** [30].

variations

- **microwave, RF and magnetic-gradient control** can replace some laser-driven qubit operations [59, 60].
- **connectivity**: many-to-many within zones and ions shuttling between zones [58, 61].
- **dual species** like ytterbium + barium for computing and cooling [62].
- **Rydberg-ion interactions** can reduce reliance on collective motional modes for entangling operations, while introducing UV/VUV laser, lifetime, Stark-shift and electric-field-sensitivity challenges [63, 64].
- **hybrid** neutral atoms-ions platforms [1838, 1839].

path to scalability

- **2D QCCD** and ions shuttling [67, 1840].
- **QCCD tiling** as pursued by Universal Quantum [106].
- **multi modules** ion traps with intermodule ions shuttling [62].
- **multi-layer ion traps** to enable long-range microwave based entanglement [68, 1841, 1842].
- **photonic interconnect** to entangle qubits from different QPUs [65, 66].

Figure 187: Trapped ions qubits highlights, challenges, variations and path to scalability. Olivier Ezratty, 2022-2025.

Ca^+ and multi-photon UV excitation schemes in Sr^+ and other species. Rydberg levels are generally auxiliary interaction states rather than the two long-lived computational basis states themselves. Crystal Quantum Computing is pursuing Rydberg-mediated $^{88}Sr^+$ gates, while academic work includes the groups of Markus Hennrich [63] and Ferdinand Schmidt-Kaler [1850].

Clock qubits use transitions whose frequency is first-order insensitive to magnetic-field fluctuations at a chosen operating point, meaning $d\nu/dB = 0$ locally. This suppresses, but does not eliminate, magnetic dephasing because second-order Zeeman and other shifts remain [1845]. Zero-field clock states, for example selecting $m_F = 0$ hyperfine states in $^{171}Yb^+$ or $^{133}Ba^+$, are first-order insensitive around their operating point. First-order field-insensitive (FOFI) transitions such as those used in $^{43}Ca^+$ or $^9Be^+$ operate at a non-zero bias field where the transition-frequency curve has an extremum. For the commonly used $^{43}Ca^+$ clock transition this occurs near 14.6 mT. The FOFI values are indicated in Table 6.

Figure 188 summarizes these variants using ion energy levels and transitions. The left panel shows a generic atomic level structure with transitions used for qubit control, state preparation and readout. Such diagrams of atomic electronic energy levels and allowed transitions are called Grotrian diagrams. The middle and right panels illustrate different choices of the $|0\rangle$ and $|1\rangle$ qubit states.

The energy separation between the two chosen computational states determines the resonant qubit-control frequency, ranging from MHz Zeeman splittings to GHz hyperfine splittings and hundreds of THz for optical qubits. Rydberg excitation is different: it addresses a high-lying auxiliary electronic state, often in the UV or VUV, rather than simply extending the computational-state splitting.

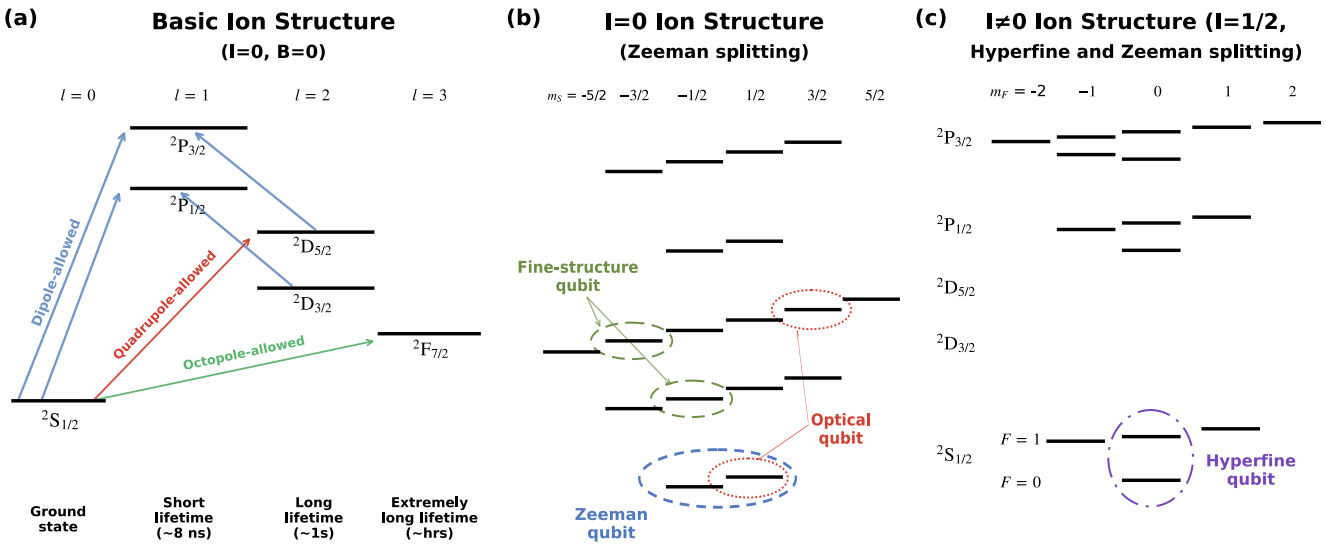


Figure 188: Various types of trapped ions and their respective energy transitions. Source: [1827].

The spatial confinement of trapped ions is mainly implemented with two electromagnetic trap families, Paul and Penning traps, while newer proposals add optical tweezers for local ion positioning and reconfiguration [1851]:

- With a **static magnetic field** and a **static electric quadrupole field**: these are Penning traps. Their underlying principle predates 1959, while Dehmelt's 1959 experiments established high-vacuum magnetron/Penning trapping for precision charged-particle control. Modern micro-Penning approaches are being developed by Jonathan Home's team at ETH Zurich and Zuriq for scalable 2D ion arrays [26, 1852, 1853].

- With a **time-varying radio-frequency electric field**: these are Paul traps named after Wolfgang Paul. They can be implemented as three-dimensional or linear traps and as microfabricated surface-electrode traps [67]. Segmented surface traps are widely used for QCCD architectures, including Quantinuum and Oxford Ionics, while other vendors use different linear RF geometries. Proposals also exist for more complex three-dimensional RF trap structures [1854].

- With using **light tweezers** as proposed by Peter Zoller and Ignacio Cirac et al. in 2026 [1855]. The technique proposed with Ba^+ ions is similar to atom shuttling used with cold atoms since 2022. It uses a storage zone and a gate zone where entangling gates are implemented as well as sympathetic cooling (Figure 189).

These traps use static and radio-frequency electrode potentials for confinement and transport. Lasers are then used, depending on the architecture, for photoionization, Doppler cooling, resolved-sideband or Raman-sideband cooling, qubit initialization, coherent gates and fluorescence readout [1856]. The relevant phonons are quanta of the collective normal modes of ion motion, not shock waves propagating from ion to ion. In the Lamb-Dicke regime, the ion's motional excursion projected along the laser wave vector is small, conventionally $\eta\sqrt{2\bar{n}+1} \ll 1$, which allows well-resolved carrier and motional-sideband control.

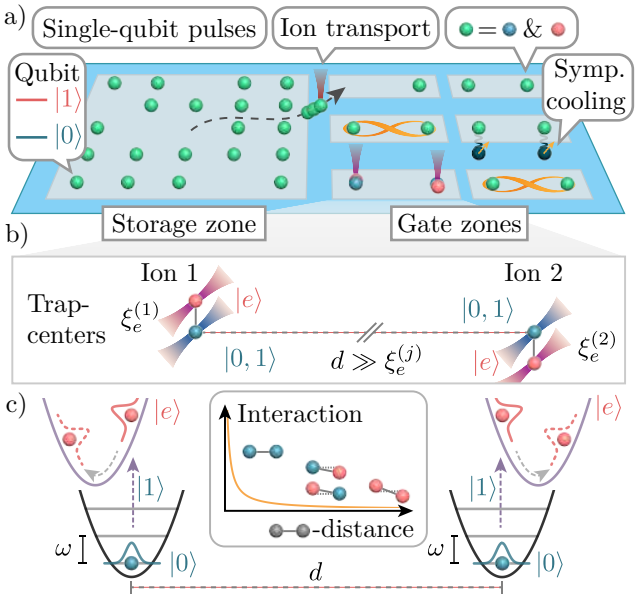


Figure 189: Ions could be positioned using light tweezers like with cold atoms as proposed in 2026. Entangling gates would be implemented in a dedicated gate zone. Single-qubit gates could be implemented in both the storage and the gate zones. Source: [1855].

Laser beams used to cool ions, handle readout and quantum gates can be conveyed using waveguides in 3D PIC (photonic integrated circuits) ion traps as described in [1857–1859] and in Figure 226. The ions are usually aligned in rows and separated by about 2 to 5 μm as shown in Figure 192 but other settings are proposed

ion	atomic mass (amu)	nuclear spin	transitions $\lambda_{1/2}$, $\lambda_{3/2}$, λ_D (nm)	decay rate γ_D (s^{-1})	fine structure $\omega_F/2\pi$ (THz)	qubits type	FOFI B_0 (mT)	qubit gates
Be^+	9	3/2	313, 313, N.A.	N.A.	0.198	H	11.94	R, M
Mg^+	25	5/2	280, 280, N.A.	N.A.	2.75	H	10.9	R, M
	24	0	"	"	"	*		R
Ca^+	40	0	397, 393, 729	0.855	6.68	Z, F, O		R, O
	43	7/2	"	"	"	H, O	14.61	R, M
Sr^+	87	9/2	422, 408, 674	2.90	24.0			
	88	0	"	"	"	O		O, R
Cd^+	111	1/2	226, 214, N.A.	N.A.	74.4	H	Clock	R
	112, 114	0	"	"	"	*		R
Ba^+	133†	1/2	493‡, 455, 1762	0.0286	50.7	H, O	Clock	
	137	3/2	"	"	"	H, O	Clock	
	138	0	"	"	"	O		R
Yb^+	171	1/2	369‡, 329, 411	139	99.8	H	Clock	R, M
	172, 174	0	"	"	"	O		
Y^+	89	1/2	421, N.A., N.A.	N.A.	N.A.	H, O	Clock	R, M

Table 6: Properties of ions of interest for quantum computing. $\lambda_{1/2}$, $\lambda_{3/2}$, λ_D refer to the wavelengths of the transitions from the ground state to the $P_{1/2}$, $P_{3/2}$, and (if present) $D_{5/2}$ levels with decay rates γ_D. $\omega_F/2\pi$: fine-structure splitting frequency of the ion's lowest excited state with ω_F being the angular frequency of the energy difference between the $P_{1/2}$ and $P_{3/2}$ excited energy levels. The subscript "F" stands for "Fine structure". Qubit types: Z (Zeeman), H (hyperfine), F (Fine structure), and O (optical). FOFI (first-order field-insensitive): transitions that have been used are indicated in the FOFI column with the required magnetic field. "Clock" indicates nominally zero-field clock-state operation. Gate types: R (Raman), O (Optical), M (Magnetic [AC or static gradient]). * these isotopes have no good method of state discrimination; they have been used for sympathetic cooling, essentially as Zeeman qubits with no state detection. †: this isotope of barium is radioactive, with a half life of 10.5 y. ‡Light at 532 nm (355 nm) from a doubled (tripled) YAG laser has been used to drive Raman transitions in Ba^+ (Yb^+). Modified using table II from [1827] and added yttrium based on [1849].

in 2D fashion, like what is planned by Quantinuum, beyond their racetrack 2023 configuration.

One key variation of the Paul trap is the Quantum Charge-Coupled Device (QCCD). It distributes ions over spatially distinct storage, interaction, cooling and measurement zones on a segmented trap, with local laser and/or microwave operations and ion transport between zones [58]. The number of ions per zone is architecture-dependent rather than fixed to 4–12. In microfabricated surface traps, the ion-electrode distance is commonly of order a few tens to roughly 100 μm, depending on the device.

The technique is used by many vendors like Quantinuum [61], Oxford Ionics (IonQ since June 2025) and Universal Quantum, one challenge being to direct laser light in the ion [1860].

A variation of the technique moves around ions between adjacent ion traps, as studied by Universal Quantum. It seems possible to implement this type of ion shuttling with good operation fidelities. In 2024, that team transported ions from one QCCD circuit to the other in 0.4 ms and with a fidelity of 99.999993%, using ^{171}Yb+ ions for computing and ^{138}Ba+ for transfer [62]. All of this requires some specific circuit compiling optimizations [1861–1863].

Cryogenics. Trapped-ion processors can operate with room-temperature or cryogenic traps. The ions' internal and motional degrees of freedom are cooled by laser techniques, not by the chamber temperature. Doppler cooling typically brings the motion to the mK regime, while resolved-sideband or Raman-sideband cooling can approach the motional ground state. Cryogenic traps, often operated around 4–20 K, can reduce anomalous electric-field heating, improve vacuum through cryopumping and simplify some thermal-management constraints, but they are an architectural choice rather than an intrinsic requirement [1831, 1836, 1864].

At last, some ion chips now include integrated detectors like SNSPDs (superconducting nanowire single-photon detectors) which are cooled at 4K. Researchers from the

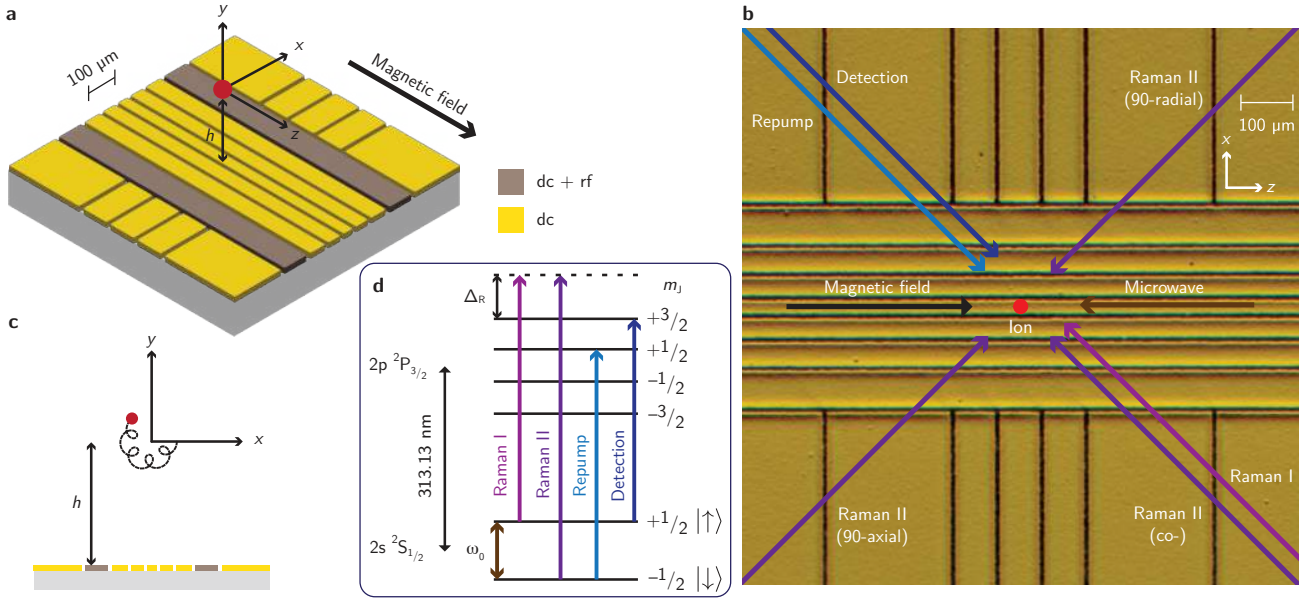


Figure 190: Ions microwave drive combining a global magnetic gradient field and a local microwave drive. Source: ETH Zurich [1853].

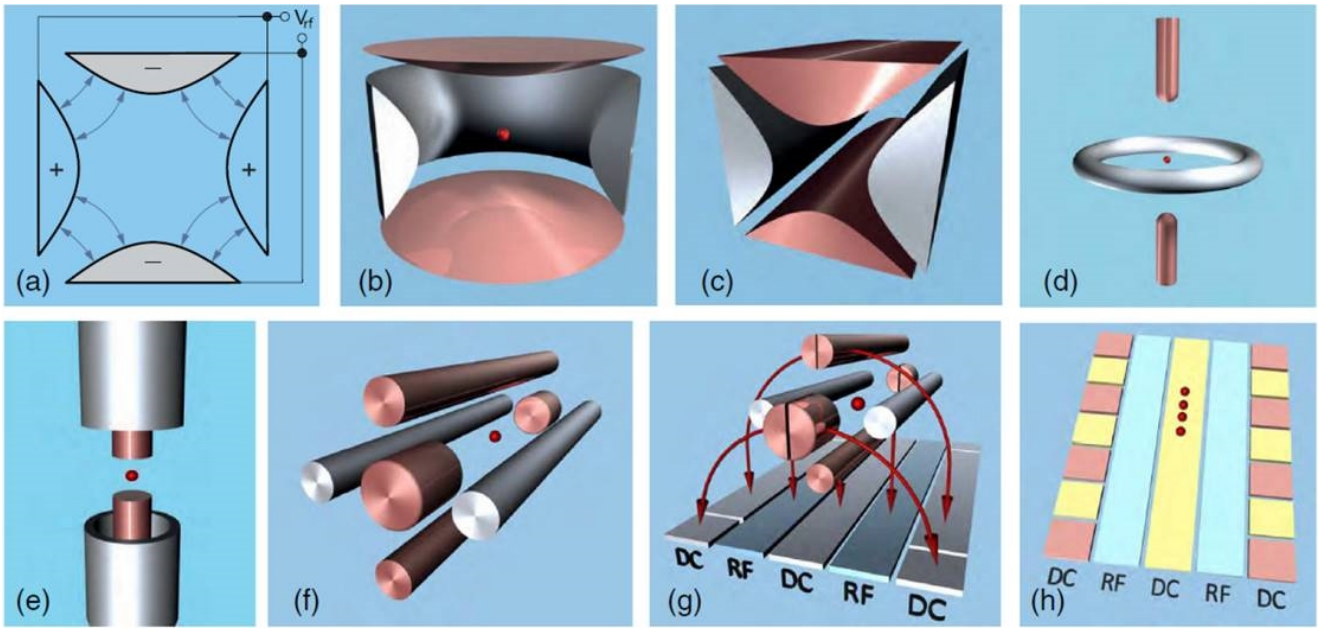


Figure 191: Various ways to trap ions. RF Paul trap geometries with (a) RF trapping basic concept with quadrupolar fields oscillating at an RF frequency produced by parabolic electrodes. (b) The simplest cylindrically symmetric version of the basic RF trap. (c) The simplest translationally symmetric version of the basic RF trap. (d,e) Topologically equivalent deformations of the geometry shown in (b). (f) Topologically equivalent deformations of the geometry shown in (c) with additional endcap electrodes added to form a four-rod, linear trap. (g) The four-rod trap in (f) may be deformed such that all electrodes reside in a single plane, forming a linear "surface-electrode trap", which is used in most QCCD ion traps nowadays (h) A subset of the electrodes in a linear trap [a surface-electrode trap is depicted here, but segmentation may be applied to other linear trap geometries, such as that shown in (f) may be segmented to allow trapping in multiple zones, along the axial direction. Source: [1827].

University of Innsbruck and from ETH Zurich are thinking about making the trapped ion technology "portable", using compact cryogenics and requiring more compact lasers [1865]. They are part of the EU-funded **PIEDMONS** project (E2020). It also involves Infineon Austria [1866].

Trapped ions or ion traps? An ion is a multilevel atomic system. A qubit is defined by selecting two long-lived internal states of that ion as a computational subspace. The ion trap is the electromagnetic structure that confines and transports the ions. Thus "trapped-

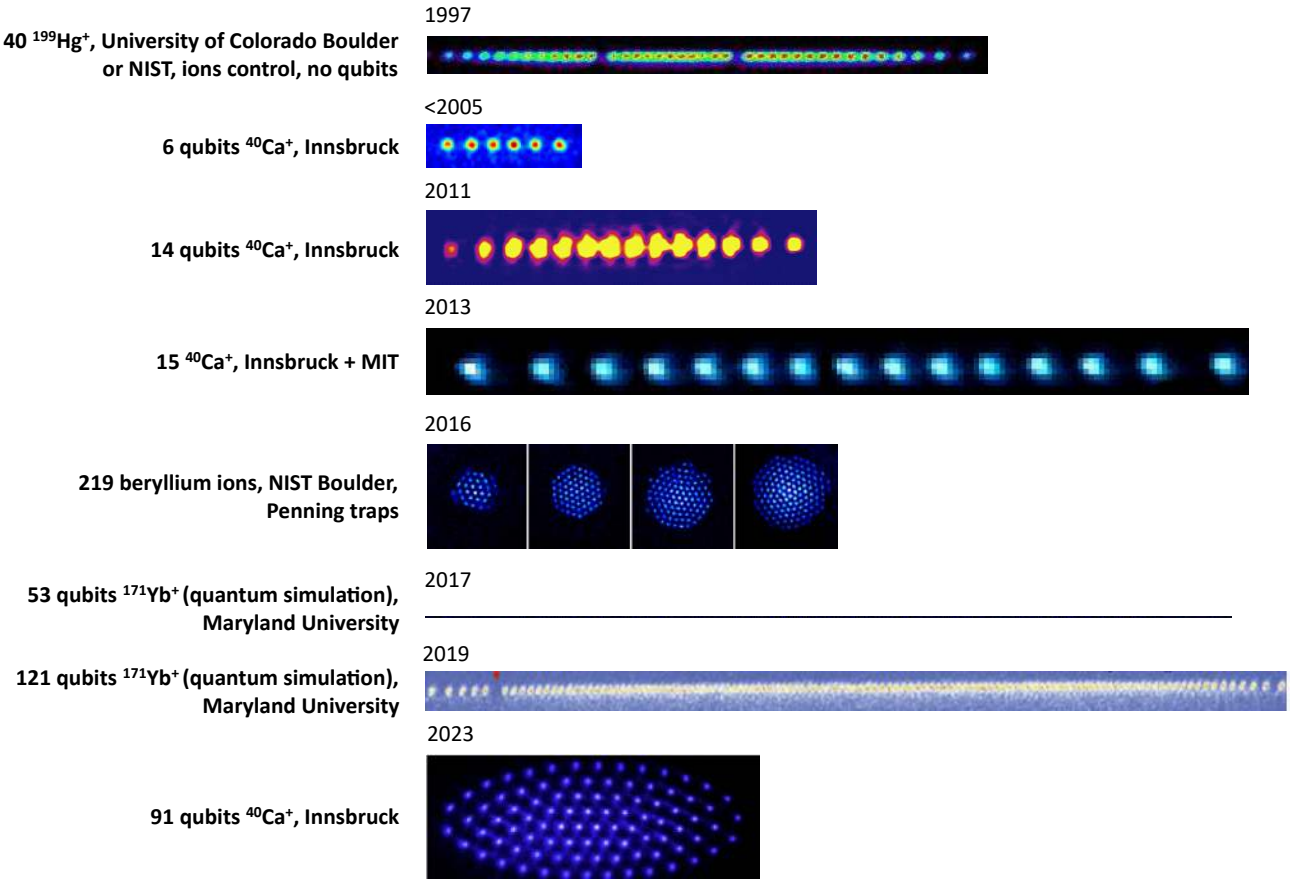


Figure 192: Selected trapped-ion experiments over time. Early systems used Penning or Paul traps, while current traps are built with QCCD circuits, enabling ions shuttling in 1D or 2D. Compilation: Olivier Ezratty. 2020-2023.

ion qubit" describes the information carrier, while "ion trap" describes the trapping hardware.

Ions applications. Trapped ions have at least two other use cases: quantum memories, and their integration in quantum repeaters for secure quantum telecommunications, including quantum keys distribution [1867]. This involves interactions between trapped ions and photons, using cavities.

Scale-in. As of September 2026, Quantinuum Helios provides a 98-qubit fully programmable gate-based trapped-ion processor [119]. Much larger crystals have been controlled for analog quantum simulation, including 512 trapped $^{171}Yb^+$ ions and site-resolved measurements on 300 of them [1868]. Scaling digital processors is limited by several coupled effects, including motional-mode crowding, laser or microwave control complexity, shuttling overhead, crosstalk and anomalous electric-field heating. The latter often increases strongly as the ion-electrode distance is reduced, with an empirical distance exponent that varies by device and is not universally d^{-4} [1837]. Micro-Penning arrays remove the RF trapping drive and are one alternative being pursued by ETH Zurich and Zuriq [26].

Wiring a QCCD circuit is also a scaling challenge because segmented traps require many independently controlled DC electrodes, often with dedicated DAC channels, in addition to RF trapping, microwave and optical-routing hardware [1869]. The number of control electrodes is not simply one wire per qubit. Multiplexing and local integrated electronics can reduce the off-chip wiring burden, as proposed by RIKEN researchers in 2025 [1870].

Another possibility is the use of ion shuttling between zones and neighboring trap modules [1873, 1874]. A 2017 blueprint proposed microwave gates, magnetic-field gradients, silicon trap circuits, X-junctions and integrated control electronics for a very large fault-tolerant machine [25]. Its resource and footprint estimates were tied to the error-correction assumptions available at that time. Modern QCCD performance depends on code choice, physical error model, routing, parallelism and decoding, not only on physical-qubit count. Ion shuttling therefore requires architecture-aware circuit compilation [1840, 1875, 1876], with recent work also exploring machine-learning-assisted optimization [1877].

Quantinuum's future 2D architecture and several other vendor roadmaps follow related multi-zone approaches. The route is credible, but wall-clock speed, transport parallelism, calibration and thermal management remain important scaling constraints.

Scale-out. Beyond a single QCCD chip, two main approaches are photonic entanglement between modules

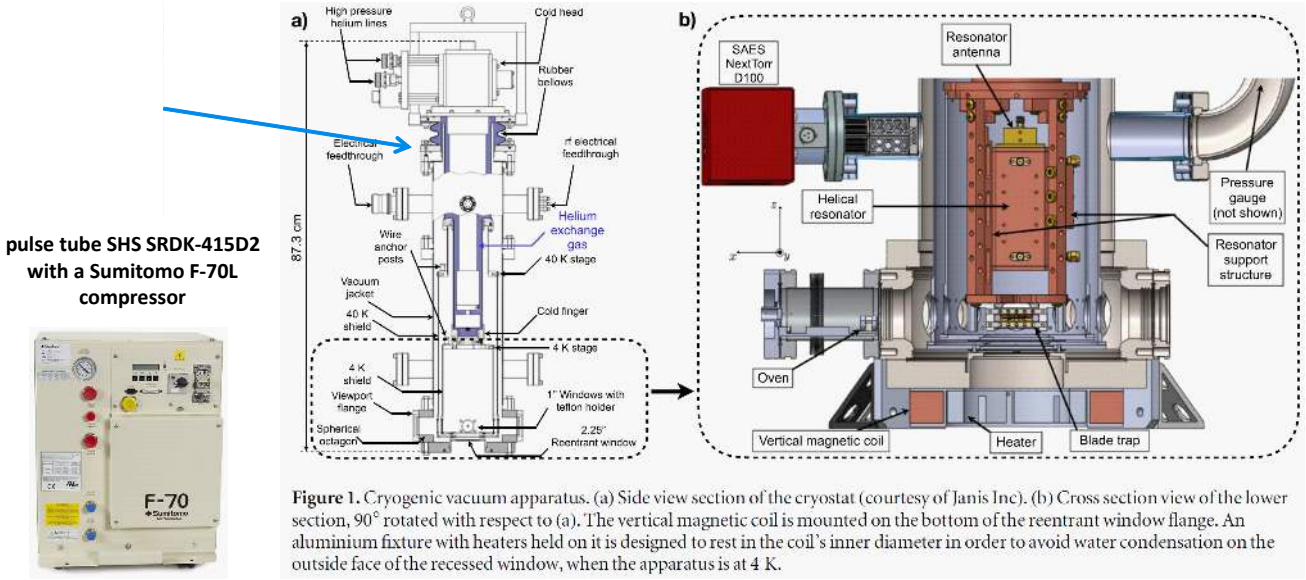


Figure 193: The 4K cryostat used a while ago by Christopher Monroe's team at the University of Maryland to trap more than a hundred ytterbium ions. It operated a 4.2K SHS pulse tube and a Sumitomo compressor. Source: [1871, 1872].

and direct ion transport between adjacent traps. In a 2023 experiment, two $^{40}Ca^+$ ions separated by 230 m were entangled through 520(2) m of optical fiber with Bell-state fidelity up to 88% and a per-attempt success probability of 4×10^{-5} [66]. Other experiments report different probabilities because collection efficiency, protocol structure, fiber loss and repetition rate differ, so no single value such as 2.18×10^{-4} represents a universal remote-entanglement limit. Extending such links from demonstrations to fault-tolerant distributed computing still requires major improvements in rate, fidelity, memory lifetime and networking protocols.

Qudits. A complementary route is to encode a d-level qudit in several internal levels of one ion, increasing Hilbert-space dimension without increasing the number of particles. A $^{137}Ba^+$ experiment demonstrated control and single-shot readout of 13 computational levels with unheralded SPAM fidelity around 91.7%, and 12-level readout with one error-detection step at about 98.97% [1878]. This can reduce carrier count for some algorithms, but calibration, control and error correction generally become more complex as d grows. Multiple qubits can also be encoded in one ion [1879].

Error correction. High physical gate fidelity and flexible connectivity can reduce routing overhead for quantum error correction, especially for codes that benefit from non-local parity checks such as some qLDPC constructions. They do not generically guarantee a lower total QEC overhead, which also depends on leakage, correlated errors, measurement fidelity, cycle time and code architecture. Slower physical gates relax the absolute latency required of a real-time decoder per syndrome round, but they also reduce logical throughput and leave qubits exposed to noise for longer wall-clock times. Trapped-ion roadmaps therefore trade physical fidelity and connectivity against cycle speed and transport overhead. Qudit and bosonic encodings provide additional academic routes to reducing hardware overhead [1880].

Quantum simulations can also be implemented with trapped ions [1881, 1882]. Quantum simulations using trapped ions have been proposed for the simulation of strongly correlated many-body dynamics, of linear vibronic coupling models (LVCMs) [1883] and molecular dynamics with coupling ion qudits manifold with their nuclear vibrational degree of freedom [1884]. It has also been used for simulating interacting nucleons and pions [1885].

In 2023 and 2024, a Tsinghua University team in China demonstrated stable control of a 512-ion $^{171}Yb^+$ two-dimensional Wigner crystal in a monolithic three-dimensional Paul trap. They sideband-cooled transverse modes and implemented long-range Ising-model quantum simulation with tunable couplings on up to 300 individually resolved ions, using a 411 nm laser [1868] (Figure 194). The ions were read out with site-resolved single-shot fluorescence imaging on a CMOS camera. "Single-shot" describes obtaining the state estimate from one measurement exposure and is independent of whether the measurement is quantum non-demolition. The platform is a large-scale analog quantum simulator and is not yet a 512-qubit universal gate-based QPU. But in September 2026, using the same platform, they proposed a frequency-multiplexing scheme for implementing parallel entangling gates their 2D-ion setup and to implement on it some quantum LDPC error correction codes [1886].

In 2026, Peter Zoller et al. proposed a framework for bounded-error quantum simulation, in other words a model to predict and certify simulation errors in trapped-ion experiments. The model was validated by comparing a digital simulation with a 51-ion one-dimensional system [1887].

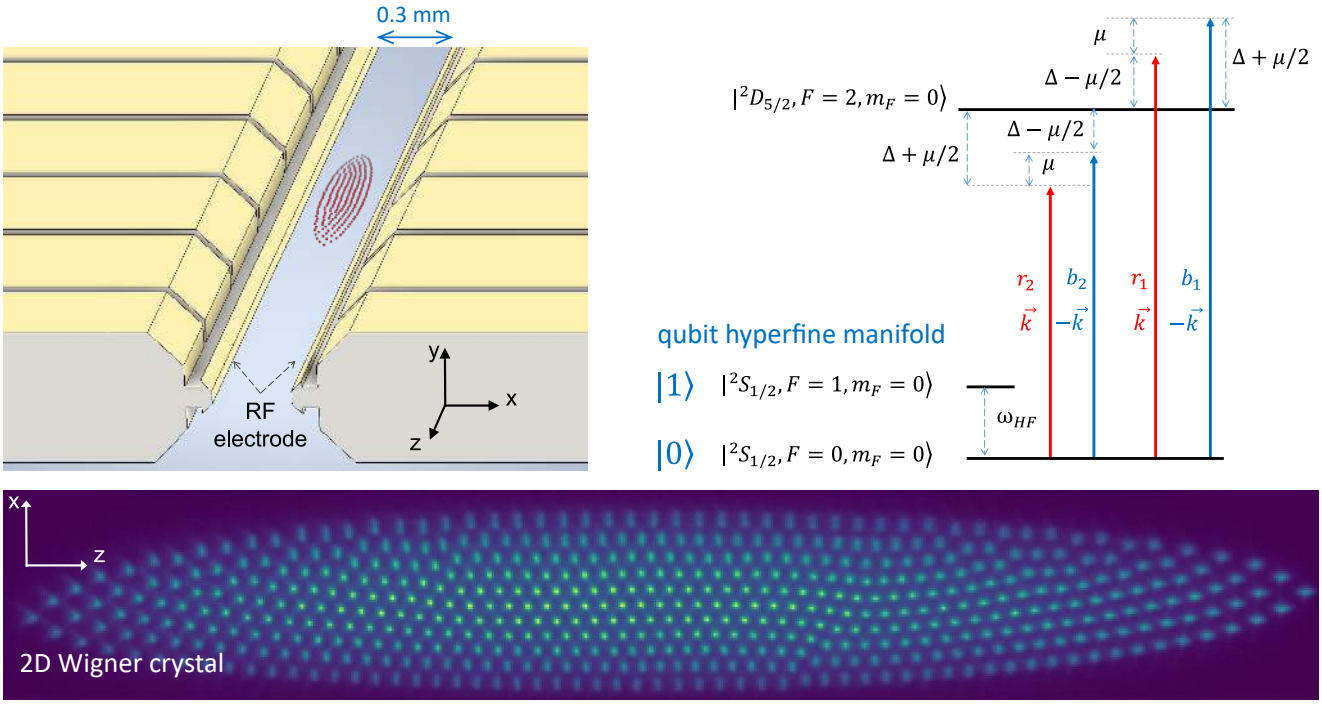


Figure 194: The 2D Wigner crystal with an elliptical shape used to control 512 ions between RF electrodes. Source: [1868].

Other trapped-ion implementation variations include hybrid digital-analog QPUs for optimization problems [1888] and encoding information in quantized mechanical modes to form Gottesman-Kitaev-Preskill states. GKP states are bosonic quantum-error-correcting encodings, not self-correcting logical qubits. A trapped-ion experiment demonstrated a universal logical gate set on GKP-encoded motional modes in 2025 [1889].

Hybrid cold-atoms and ions simulations are also investigated, by Ferdinand Schmidt-Kaler from Johannes Gutenberg-Universität Mainz in Germany [1890]. It is based on an ion trap circuit associated with a mirror magneto-optical trap (mMOT) which is positioned back-to-back to the ion-trap [1838]. What is it made for? Mainly, to simulate solid state physics phenomena.

1.7.3 Qubit operations

The general operating principles of trapped-ion qubits are as follows:

- **Preparation**. Neutral atoms can be produced from an oven or by laser ablation, photoionized, loaded into the trap and laser-cooled [1891]. Doppler cooling reduces the initial motional temperature, while resolved-sideband or Raman-sideband cooling can bring selected motional modes close to their ground state. In sympathetic cooling, a co-trapped coolant ion, often of another species, is directly laser-cooled and removes motional energy from computational ions through their Coulomb-coupled normal modes. Optical pumping prepares the chosen $|0\rangle$ internal state. The experiment operates in ultra-high vacuum, with either room-temperature or cryogenic trapping hardware depending on the architecture.
- **Qubit quantum state** is encoded in two selected long-lived internal states of a multilevel trapped ion, controlled by microwave, RF, Raman or direct optical transitions depending on the encoding.
- **Single-qubit quantum gates** are driven by resonant microwave or RF magnetic fields, Raman laser pairs or direct optical transitions, depending on the qubit type. High-fidelity trapped-ion single-qubit gates are commonly in the few-μs to few-tens-of-μs range. For example, the 2025 $^{43}Ca^+$ fidelity record used gate times from 4.4 to 35 μs [1831]. Ultrafast nanosecond-scale demonstrations exist, but they are not representative of current highest-fidelity processor operation.
- **Two-qubit quantum gates** most commonly exploit shared collective motional modes of an ion chain as a quantum bus. These modes are normal modes of the Coulomb-coupled crystal rather than vibrations propagating sequentially from one ion to the next. A standard implementation is the Mølmer-Sørensen (MS) gate, where bichromatic optical or microwave fields create a state-dependent force and transiently couple the internal states to collective motion. The ideal gate trajectory returns the motion to its initial phase-space point, so exact motional-ground-state occupation is not a fundamental requirement, although low and well-controlled phonon occupation helps high fidelity. Gate times span roughly tens of microseconds to about a millisecond across architectures [23]. Error scaling with ion number is architecture- and pulse-dependent. Expressions such as $\sim (T/T_2)N^\alpha$

Figure 195: Image sensor for trapped-ion-qubit readout from Oxford Instrument, the Andor iXon Ultra 888 UVB.

Figure 196: An image sensor from Hamamatsu, the H10682-210 PMT.

with $1 \leq \alpha \leq 2$ describe particular models rather than a universal trapped-ion gate law [24, 1892, 1893]. Scalable-control proposals use combinations of static DC electrode potentials, RF trapping fields, near-field microwaves [59, 60, 1894], integrated photonics [1895] and piezo-optomechanical circuits [1896].

High-fidelity motional-mode gates have traditionally used near-ground-state cooling because thermal occupation and mode-frequency fluctuations can increase residual spin-motion entanglement. Resolved-sideband cooling removes motional quanta one by one and sympathetic cooling transfers motional energy to a co-trapped coolant ion. Ground-state cooling is not a fundamental requirement for every high-fidelity gate. Motion-robust pulse shaping and alternative gate protocols can substantially relax this requirement. Cooling and transport scheduling can also be optimized at the compiler level [1897, 1898].

- **Qubit readout** usually uses state-dependent fluorescence after resonant laser excitation. The emitted photons can be detected with PMTs or PMT arrays, EMCCD/CCD/CMOS cameras, or trap-integrated superconducting nanowire single-photon detectors (SNSPDs) [139, 1899]. Camera-based readout can use machine-learning classifiers for fast state discrimination [1900].

  State-dependent fluorescence maps one computational basis state to a bright cycling transition and the other to a dark state. Whether $|0\rangle$ or $|1\rangle$ is defined as the bright state is an encoding convention. Qubit readout can also use NbTiN SNSPDs integrated into surface-electrode RF traps [1901]. Selective per-qubit readout is important for quantum error correction and feed-forward algorithms and can use individually addressed laser beams with AODs [1902, 1903], EOMs, integrated waveguides, temporal multiplexing, dedicated measurement zones or ancilla ions [1904]. Mid-circuit measurement and reset (MCMR) has also been demonstrated [1905, 1906].

1.7.4 Setup

A typical trapped-ion setup contains an ultra-high-vacuum chamber with an ion trap, optical access and imaging hardware. Neutral atoms are supplied from an oven or laser-ablation source and photoionized before trapping. Some architectures use a MOT-assisted source. The trap package may operate at room temperature or be cryogenic, commonly in the 4–20 K range when cryogenic operation is chosen.

Ions are confined and transported with static electrode voltages and RF trapping fields, while microwave/RF and optical fields implement state control depending on the architecture. State-dependent fluorescence is detected with cameras, PMTs or integrated photon detectors. A complete system also includes lasers, timing and control electronics, RF/microwave sources, vacuum equipment and classical compute servers. Compact implementations can fit in a few equipment racks [164] (Figure 198).

1.7.5 Research

About a hundred research teams around the world are working on trapped ion qubits in almost every country working on quantum technologies (Australia, Austria, Canada, China, Denmark, Finland, France, Germany, India, Israel, Japan, the Netherlands, Singapore, Switzerland, UK, USA, South Korea) (see an inventory in [1907]).

Rainer Blatt from the University of Innsbruck is one of the pioneers in this field. He created a register of 14 addressable qubits in 2011 and increased it to 20 addressable and individually controllable qubits in 2018, using calcium ions.

Rainer Blatt then cofounded **Alpine Quantum Technologies** (2017, Austria) where he characterized up to 10 high-quality trapped-ion qubits [1908]. In 2021, his team also demonstrated the use of trapped ions to cre-

ate qudits with 3, 5 and 7 levels, potentially opening the path for more powerful trapped ion based quantum computing [1909].

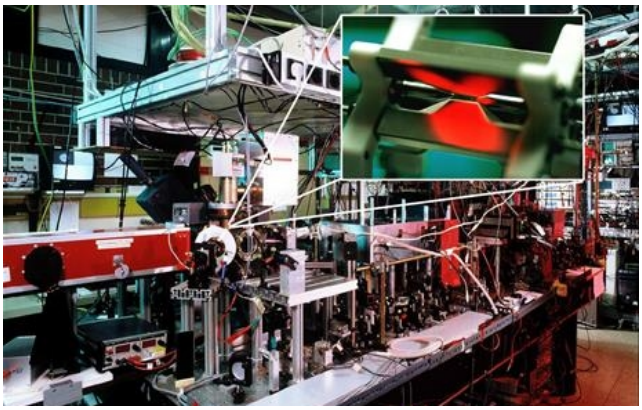


Figure 197: Rainer Blatt's lab in Innsbruck.

Quantum simulation using trapped ions, and an Ising model as with the D-Wave, is also investigated by some laboratories such as at **ETH Zurich** in Jonathan P. Home's Trapped Ions Quantum Information Group (TIQG)**,** the **University of Maryland**, elsewhere in the USA [1910–1912] and also in China [1913].

In May 2020, Wesley Campbell's **UCLA** team associated with UNSW announced that they had stabilized barium ions ($^{133}Ba^+$) to build quality qubits in a linear trap [1914]. In 2024, the same team reached single qubit fidelities of 99.997% [1915].

Let's also mention the **IQOQI** (Austria, see Rainer Blatt, one of their laboratories, Figure 197) and the **IQST** (Germany), and their calcium based 20-qubit prototype, who coauthored [1916]. Then, the Ion Quantum Technology Group from the **University of Sussex** (UK) that is run by Winfried Hensinger and its 10 qubits prototype, proposing an architecture design to scale up to 1,000 qubits through a cluster of quantum processors [1917, 1918]. The group led to the creation of the startup **Universal Quantum** (2019, UK).

In March 2021, the DoE **Sandia Labs** launched QSCOUT (Quantum Scientific Computing Open User Testbed), a cloud-accessible trapped-ion testbed for selected research users [1919]. Its initial processor used $^{171}Yb^+$ ions and the Jaqal ("Just Another Quantum Assembly Language") low-level instruction language. The earlier 2021 roadmap anticipated expansion beyond the initial three-qubit configuration, so those numbers should be treated as historical targets rather than a current system specification.

In August 2023, Sandia Labs introduced an ion trap capable of controlling up to 200 ions [1920].

The **MIT Lincoln Labs** works on integrated silicon photonics for the manipulation of ions [1921].

Also in the USA, a Georgia Tech Research Institute team led by Creston Herold and collaborators has developed a compact permanent-magnet Penning-trap platform. In 2024, they demonstrated individual addressing and parallel fluorescence readout in a rigidly rotating planar crystal of $^{40}Ca^+$ ions using a metastable $D_{5/2}$ qubit manifold [1922]. The experiment used a permanent magnetic field rather than RF confinement and completed the basic control operations needed for programmable quantum simulation on this Penning-trap platform.

The European Flagship includes the **AQTION** project, which is led by the University of Innsbruck and has a budget of €9.57M. The objective is to reach 50 operational qubits to prepare for the next phase, beyond 100 qubits, by adopting a distributed architecture with photonic links. Alpine Quantum Technologies (AQT), the University of Oxford, ETH Zurich, Fraunhofer IOF and Atos are participating. Atos works on the solution software stacks and applications.

In **Israel**, a team of researchers from the Weizmann Institute led by Roee Ozeri announced in 2022 the creation of the first local quantum computer using 5 strontium ions [1923]. They plan to reach 64 qubits someday. It led to the creation of the startup Quantum Art in 2022.

In **Singapore**, Manas Mukherjee at CQT/NUS leads work on ion trapping for quantum computing and metrology. NTU researchers have developed electro-optical modules that combine planar ion-trap electrodes with silicon photonics and in-trap photodetection concepts compatible with wafer-scale fabrication [1924, 1925]. Related work with A*STAR, NTU and Université Paris Cité has explored glass-wafer and integrated-photonics approaches for Sr^+ ion platforms.

In **Russia**, the Russian Quantum Center, the P.N. Lebedev Physical Institute and collaborators developed a trapped-ion qudit processor based on $^{171}Yb^+$ ions. The peer-reviewed 2025 system uses eight individually controllable four-level qudits, or ququarts. Its computational Hilbert-space dimension is $4^8 = 2^{16}$, hence the statement that it is computationally equivalent in dimension to a 16-qubit register [1926]. This does not mean that four ions with four levels are equivalent to 16 qubits. The platform uses a three-dimensional linear Paul trap and 435 nm electric-quadrupole transitions for qudit encoding. The same research program has demonstrated basic algorithms and molecular simulations on the multiqudit register.

In **South Korea**, half a dozen research teams work in the field of trapped ions, including Taehyun Kim's team which proposed some optimization of quantum error correction [1927] and to improve the manufacturing of silicon-based ion traps [1928], and Joonsuk Huh's team which works on dual-rail encoding by two vibrational modes sharing a single phonon [1929, 1930].

In **China**, research teams are working on gate improvements and crosstalk mitigation [1931–1933], hybrid electron and nuclear spins [1934], error mitigation [1935] and quantum simulation. In 2026, Kihwan Kim's team reported coherence beyond ten hours for a decoherence-free encoded clock qubit formed from pairs of $^{171}Yb^+$

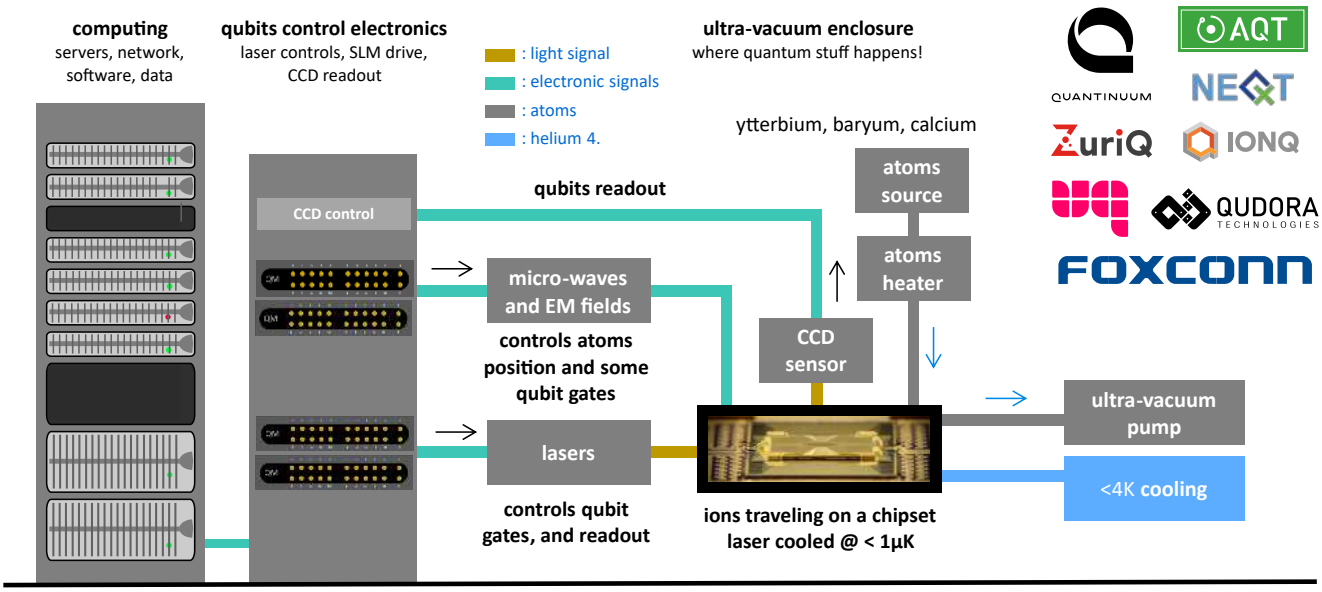


Figure 198: Generic architecture of a trapped ion quantum computer which can fit into a 2-rack system, but is usually a little larger. Olivier Ezratty, 2022-September 2026.

ions, sympathetically cooled with $^{138}Ba^+$ ions, with a fitted coherence time of about 3.77×10^4 s [154]. This is an encoded two-ion coherence result, not the T_2 of an arbitrary individual trapped-ion qubit.

1.7.6 Vendors

See two tables comparing the key technical differences between these vendors in Table 8 and Table 9 at the end of this part.

IonQ

USA, 2016, $4,093M

IonQ is a spin-off from the University of Maryland specialized in the design of universal quantum computers based on ytterbium trapped ions, and later, barium ions.

Company. IonQ was co-founded by Christopher Monroe, professor at the University of Maryland, who was their Chief Scientist until October 2023 when he left the company. Peter Chapman was their President and CEO between 2019 and April 2024 when Harry You became the Lead Director of the company, while Peter Chapman became the company chairman. One can remember that Chapman declared emphatically in 2023 that reaching 64 qubits in 2024 would be a "ChatGPT moment". This was highly questionable given the narrow scope of applications that could bring some sort of quantum advantage at this level. In February 2025, Niccolo de Masi became the CEO of the company. These are all "businessmen", having gone through many companies and different businesses. IonQ's investors include Google Ventures, Amazon, Samsung Ventures, Microsoft, Lockheed Martin, Bosch and HPE. In June 2020, they created an advisory board including David Wineland, Umesh Vazirani, Margaret Williams (ex-Cray) and Kenneth Brown (Duke University). IonQ's story exemplifies the good, the bad and the ugly of this industry with over-promises on QPU roadmaps, a SPAC and IPO, a spree of acquisitions outside the quantum computing realm, and the acquisition of Oxford Ionics, a UK competitor which had presented a more concrete scaling roadmap than IonQ's at that time, plus Skywater's acquisition in the chip manufacturing space. For the sake of History, this text will describe IonQ's initial architecture before explaining why Oxford Ionics had a much better proposal for scalability towards utility-grade FTQC.

IonQ's IPO journey started in March 2021 when it announced a new round of funding with a SPAC merger with the dMY Technology Group III fund. The initial funding was made of $350M coming from investors including Hyundai, Kia Corporation and Breakthrough Energy Ventures, and an additional $300M coming from dMY and an IPO that was finalized in October 2021. In March 2025, IonQ raised about $360 million through an equity offering program of 16 million shares of common stock. Their revenue was growing well in 2023, 2024 and 2025 (Figure 199), mostly coming from DARPA and AFRL projects, and with the Quantum Basel QPU sale in 2024. In August 2025, Amazon disclosed that it had invested $36.7M in IonQ during the year of 2024.

In January 2023, IonQ announced the opening of an R&D, production and new data center site in Bothell, Washington state, near Seattle with an area of 5,785 m^2 to be extended to a total of 9,345 m^2 as announced in February 2024 [1936]. It is an addition to their data center in Maryland. They prepared for higher-volume QPU production in anticipation of increased demand [1936]. They also formally opened an R&D lab and semiconductor testing facility in Boulder Colorado in May 2026, which made sense given Oxford Ionics had already

established its US R&D there before their acquisition by IonQ.

When Willow was formally introduced by Google in December 2024, it drove all quantum companies stocks to unprecedented levels, with IonQ's market capitalization reaching $19B (as of September 2025). It enabled IonQ to launch many acquisitions with Qubitekk (December 2024), ID Quantique (February 2025), Lightsynq (May 2025), Capella Space (May 2025) that we describe in the communications and cryptography vendors pages, Vector Atomic in quantum sensing (September 2025), Skyloom in optical communications with satellite, Skywater and Seed Innovations, an AI service company (all three in January 2026). Its apex was Oxford Ionics's acquisition, announced in June 2025, for $1B in stock swaps and $10M in cash. As a result of all their acquisitions, they had a staff of 1,100 people as of November 2025, making them probably the largest quantum technologies company in the world.

Look at the contrast, which is commonplace for traded company in this sector, between their forecast from 2021 when their did their SPAC IPO (Figure 199).

Technology. IonQ's initial trapped ion architecture became entirely moot with the acquisition of Oxford Ionics in 2025. It is a first example of a radical pivot in the quantum computing hardware vendor space. It used a single 1D array of ions of variable length which are controlled by lasers for both cooling, quantum gates and readout and with a small circuit fitting in a tiny vacuum chamber. It enabled all-to-all connectivity between ions (Figure 202 and Figure 200), although being practically limited to the number of physical qubits in a single QPU. As with all trapped ions QPUs, this is achieved at the expense of relatively slow gates in comparison with superconducting and silicon qubits QPUs.

The scalability of IonQ's trapped ions has been challenged by their failed promises. Early 2018, they announced a record of 53 coherent and entangled qubits, but these were used for quantum simulation and not with gate-based computing. At the end of 2018, they said they had reached 79 qubits associated with 160 storage qubits [1937]. It never became a product. In 2019, they had 11 characterized qubits [1938]. In October 2020, IonQ announced that it had created the world's most powerful quantum computer with 32 qubits and a quantum volume of 4,000,000 but it took over a year and a half for this system to become live and tested [1939] and made available on Amazon Braket, Microsoft Azure Quantum and Google cloud. They claimed to handle error correction codes with 13 (and sometimes, 16) physical qubits per logical qubits.

Barium. In December 2021, after they had finalized their SPAC and IPO, IonQ announced a transition from ytterbium toward barium ions, in particular $^{133}Ba^{+}$. Barium offers useful visible and near-infrared optical transitions, reducing reliance on ultraviolet optics and potentially easing the integration of photonic components. This does not mean that all control and interconnect optics can directly use standard silicon photonics. They also secured the provisioning of ^{133}Ba with a partnership with **DoE's PNNL** (Pacific Northwest National Laboratory) in February 2022. Oxford Ionics has published results with both barium and calcium ions. IonQ published research in 2025 on mixed-species two-qubit gates involving calcium, barium and strontium [1942]. It remains unclear which ion species will dominate the post-acquisition Oxford Ionics roadmap.

Gates. In February 2022, IonQ and Duke University presented a method for implementing multi-qubit interactions using spin-dependent squeezing [1943]. Such native many-body interactions can reduce circuit depth for operations including Toffoli-like gates and can be useful for quantum simulation, optimization and error-correction circuits. A native three-qubit gate does not by itself constitute a fault-tolerant universal gate set, which additionally requires an encoded architecture and fault-tolerant implementations of a universal logical gate set.

In November 2022, they announced a new generation trapped ions control chip, with multilayered glass traps and better routing of driving signals. Their record two-qubit gate fidelity as of 2023 was 99.99% with 7 ions, obtained in a non-commercial lab setting and using XX gates [1944]. They then reached this fidelity with barium ions on an unspecified development platform in 2024 [1945]. In July 2024, IonQ announced the goal to improve two-qubit gate fidelities above 99.9% in 2025 and 99.999% by the end of 2025, using logical qubits. It reaffirmed its focus on connecting multiple QPUs using photonic interconnects. In 2025, IonQ published a preprint on some work related to spin-photon interfaces realized with SiV centers chips but without describing the 'last-mile' problem of connecting these photons and ions for remote entanglement sharing [1946]. This was however extended to an experiment of a GHZ state across three quantum memories in 2026 [1947].

Past roadmaps. In December 2020, IonQ unveiled a 5-year roadmap with plans to use rack-mounted modular quantum computers small enough to be networked together in a datacenter by 2023. 2023-2024 was supposed to be the year of quantum machine learning inflection point and 2025-2026 for materials and faster optimizations. IonQ adopted a new benchmark metric of their own: algorithmic qubits, using $\log_2$ of IBM's quantum volume and a different computing mode that we cover in the benchmarking section of this book, using a set of QED-C benchmarks, which was later debunked by Quantinuum in a scathing post [1948].

IonQ's algorithmic-qubit metric (#AQ) is an application-oriented system benchmark, not a count of physical or logical qubits. Roughly, #AQ= N means that a prescribed suite of benchmark circuits with widths up to N and two-qubit-gate depths up to approximately N^2 passes a fidelity threshold after compilation and any allowed mitigation.

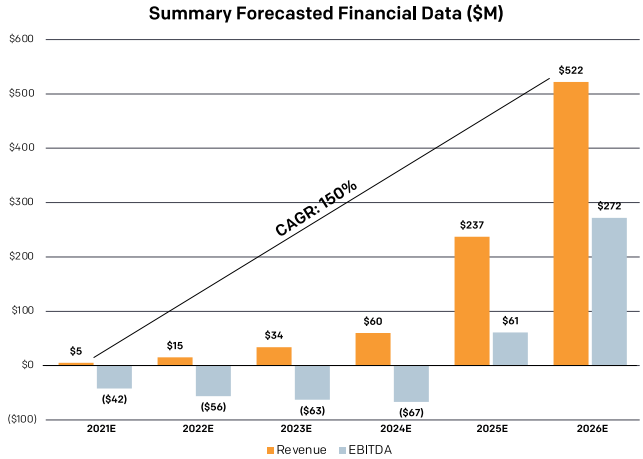


Figure 199: IonQ forecast in their investor deck from 2021 showing an exponential revenue growth starting in 2025. Their actual revenue in 2025 was $130M, off the $237M forecast, and only thanks to a flurry of acquisitions. Source: IonQ Investor Presentation, March 2021 [1940].

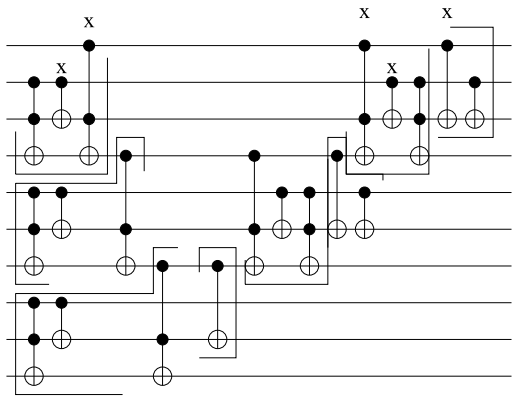


Figure 200: How the good connectivity of trapped ions can reduce routing overhead compared with nearest-neighbor architectures, as illustrated by the circuit in Figure 202. This advantage is not intrinsically limited to fewer than 50 qubits: Quantinuum demonstrated effective all-to-all connectivity on its 98-qubit Helios QCCD processor in 2026 [119]. Source of the circuit comparison: [1941].

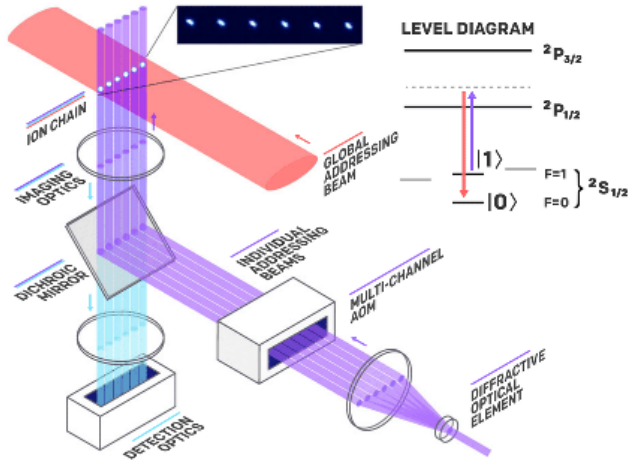


Figure 201: How IonQ was driving its ions in its 1D not scalable trap. Source: IonQ web site.

Their 32 qubits QPU reached 22 algorithmic qubits with plans to reach 29 algorithm qubits by 2023, 64 by 2025 with the Tempo system using a 16:1 error-correction encoding (meaning: 16 physical qubits per logical qubits [1949]) and gate-times of 300 μs. They plan to later rely on a 32:1 ratio. The 29 algorithmic qubits milestone was achieved in 2023 with their 32-qubit Forte system [144], which was to expand to 35 algorithmic qubits in 2024 with Forte Enterprise (and 0.4% announced two-qubit error rates). The 64-qubit milestone was reached in September 2025.

They also reached 29 algorithmic qubits, measured with their application-oriented #AQ benchmark and not a physical- or logical-qubit count, on a prototype 29-qubit system using barium instead of ytterbium in October 2023. They got 35 and 36 algorithmic qubits in January 2024 with their Forte QPU [144]. They expected to scale beyond 64 and reach a broad quantum advantage with 256 then 1,024 algorithmic qubits by 2026 and 2028. The caveat is that this required scaling-out their QPU with interconnecting several units of 64 qubits through photonic links in a distributed computing manner. Something that has not been tested yet beyond one-to-one qubit connectivity [65, 1951–1953]. It led IonQ to acquire in 2023 the assets from **Entangled Networks** (Toronto) which was creating a QPU interconnect hardware and software solution and to acquire **Qubitekk** in 2024, a supplier of photon and entangled photon sources for second generation QKD deployments [1954].

IonQ announced in August 2021 their Reconfigurable Multicore Quantum Architecture (RMQA) detailing how they would create 64 ions chips. It would assemble 4 chains or lines of 16 ions, 12 being usable as qubits and the 4 remaining for cooling, in a single chip manufactured on a glass support (Evaporated Glass Traps) replacing their previous silicon-based platform built by Sandia Labs and Honeywell. These chunks of 16 ions can be moved around, paired and entangled, to create dynamic 32 ions units. IonQ stated that this architecture could scale-up and support even more blocks of 16 ions. They were also working on the stabilization of two-qubit gates control, using some randomized benchmarking technique [1955].

FTQC roadmap. With the acquisition of Oxford Ionics in June 2025, IonQ entirely updated its roadmap [1956], with showcasing ambitious physical and logical qubit numbers, based on the scalable platform from Oxford Ionics (Figure 206). These goals remain ambitious given Oxford Ionics current experimental ion traps supported only 10 qubits as of 2025 (Figure 207). The OI

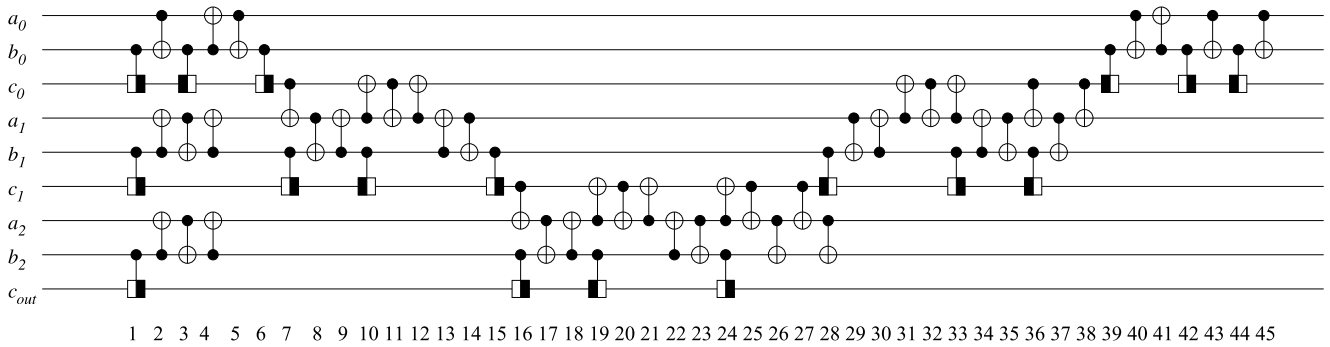


Figure 202: A 3-bit addition done with a QPU having limited nearest-neighbor qubit connectivity, in contrast with a version of the circuit for all-to-all connectivity in Figure 200. Source: [1941].

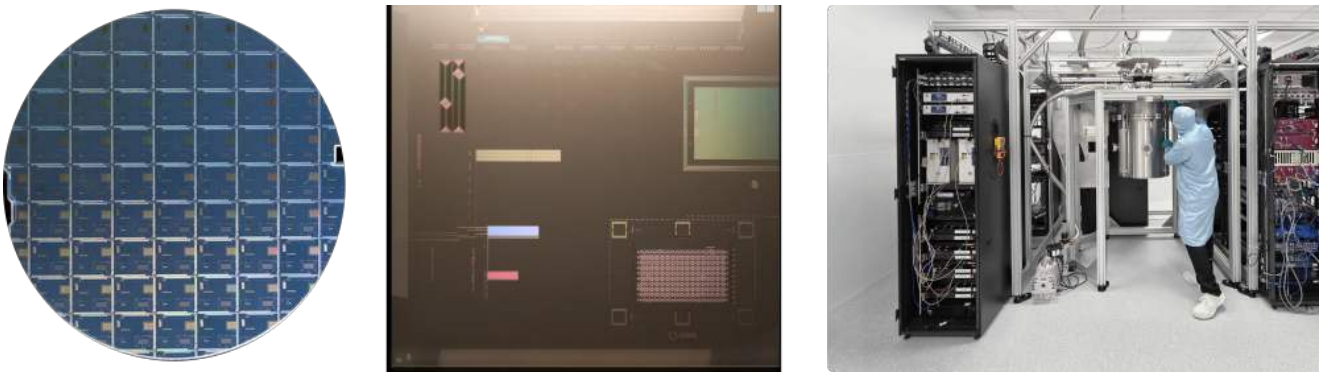


Figure 203: IonQ 256-qubit Superion system to be commercially available in 2027 with chips manufactured at Skywater. Source: [1950].

team achieved 99.99% two-qubit fidelities in September 2025 on an experimental two-qubit chip. The roadmap assumes that this fidelity can be maintained at larger scale, starting with the 256-qubit Superion system to be delivered in 2027 Figure 203.

IonQ hired Nicolas Delfosse from Microsoft in 2023. There, he proposed many improvements in the domain, which were initially customized for the IonQ 1D ion trap architecture [1957]. In July 2024, IonQ introduced a quantum error correction scheme for Clifford gates (the easiest ones to correct…) that need only three physical qubits per logical qubits. It sits in between QEM and QEC and extends the potential capability of NISQ applications [1958]. Late 2025, Delfosse et al. published a preprint proposing a solution to circumvent atom losses in ion chains [1959]. IonQ ended up publishing a detailed 110-page FTQC blueprint in April 2026 with the walking cat architecture [170] (Figure 204). It shows how IonQ will implement QEC and FTQC, down to the hardware level. The qLDPC -based walking cats are error correction probes that are continuously generated and are shuttled in the chip QCCD grid to perform gate operations or measurements on logical qubits. The blueprint provides some resource estimates for some quantum circuits. They exhibit the capability to support 110 logical qubits executing about one million T gates per day using 2,514 physical qubits and a single T factory, or 10.5M T gates per day with 220 logical qubits, 10 T factories, and 7,559 physical qubits. With 10,000 physical qubits, they estimate they can run some 100-sites quantum Hamiltonian simulation of a Heisenberg model in one month (and this is supposed to be classically intractable), and break a small RSA-40 key in 53 hours and 13,264 physical qubits, which is very slow. On a laptop, it takes less than a millisecond! They were carefully not estimating the time and resources to break an RSA-2048 key. The slow QEC/FTQC operations are mainly due to ion transport which last about 10 ms, a logical T gate lasting about 86 ms or 200 ms depending on the method, and a physical qubit measurement 200 μs. A logical CNOT is implemented in the compiler with Pauli frame tracking within a memory block, and physically between memory blocks with a computing time of 34 to 49 ms. It is computed for distance 9 error correction codes, supporting circuits size of about 10 million (depth $\times$ breadth). In July 2026, the walking cats were completed by a fast transversal logical gates implementation proposal [1960] and in August 2026 by a paper showing that a run time decoder supporting a MegaQuop could run on a simple CPU [1961], confirmed by a September 2026 experimental paper [1962]. Finally, in September, they published a resource estimate for breaking ECC-256 keys, which would need 19,397 physical qubits and 25.7 hours of computing [1963]. IonQ is also working on interconnecting multiple quantum processors using LightSynq vacancies-based technology.

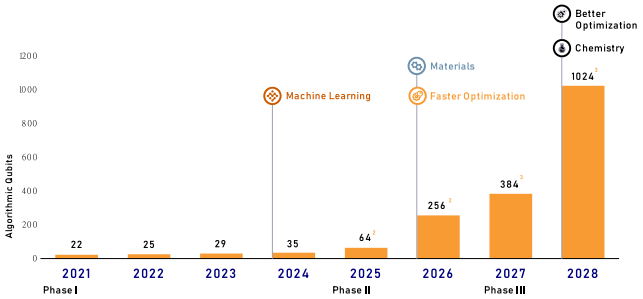


Figure 205: IonQ's qubits roadmap as published in March 2021. They had indeed reached 29 algorithmic qubits in 2023. Source: IonQ Investor Update, 2023.

Updated Technology Roadmap

	2025	2026	2027	2028	2029	2030
~~#AQ~~	~~64~~	~~256~~	~~384~~	~~1,024~~		
Qubits	64	256	10,000	20,000	200,000	2,000,000
Logical Qubits		12	800	1,600	8,000	80,000
Logical Error Rate			<1.00E-7		<1.00E-12	

Figure 206: IonQ's qubits roadmap as updated in June 2025 after they announced the acquisition of Oxford Ionics. Source: IonQ Technology Update, June 2025 [1956].

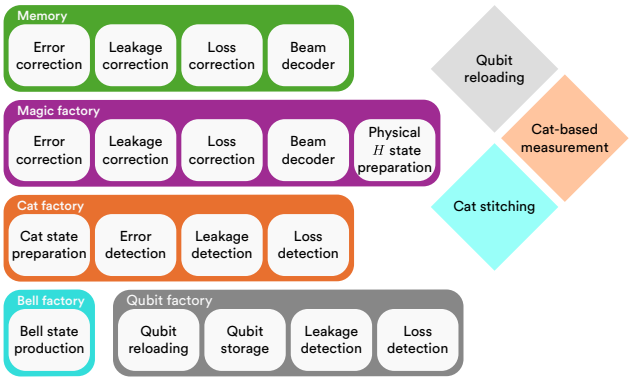


Figure 204: IonQ's QEC/FTQC architecture components presented in their April 2026 walking cats blueprint. Source: [170].

Cryogeny. A team associating IonQ, Duke University in Durham and Infleqtion) published an interesting paper describing the architecture of a trapped ions systems cryostat from Montana Instruments that is optimized to minimize the vibrations coming from the pulse tube. This seems to be one of the figures of merit to ensure the stability of the trapped ions qubits and their control devices like lasers [1964]. The ion traps are cooled at 5K while laser-based cooling using the Doppler effect cool it at an even lower temperature. In 2025, IonQ announced the creation of a miniaturized ion trap vacuum package that could avoid the use of 4K ultra vacuum pump. It doesn't necessarily mean that the ion trap chamber itself could get rid of 4K cryogenics.

Manufacturing. In November 2024, IonQ announced it would work with IMEC (Belgium) to develop and manufacture their photonic integrated circuits (PICs) and ion trap chips and with NKT Photonics lasers. It may be short lived since Oxford Ionics is working with Infineon. But then, with the acquisition of Skywater, IonQ decided to repatriate manufacturing in the USA and even updated its roadmap to save one year (Figure 208). It won't probably happen since the learning curve in ion trap manufacturing is quite long. SkyWater was connected to Infineon, since it acquired Infineon's Austin 200 mm Fab 25 in 2025. Skywater does manufacture a lot of specific semiconductors: superconducting qubit chips (for D-Wave), traditional custom CMOS chips and also photonic chips, which can be useful for IonQ. It also grows IonQ's revenue stream since Skywater made $442M in 2025. As a result, about two thirds of IonQ's revenue will come from this new activity in their portfolio.

Partnerships. In November 2019, **Microsoft** announced the integration of IonQ's quantum accelerator support into its Azure Quantum cloud offering and its Q#, QDK and Visual Studio development tools. All this was made available to developers from late spring 2020. IonQ is also proposed by **Google** in its own cloud offering, on top of **Amazon** AWS Braket. IonQ became in 2021 the only quantum computer vendor available on Amazon, Google, and Microsoft clouds (with 11 qubits, being extended to 32 qubits with the Forte QPU in December 2023). In May 2023, IonQ Aria went online on Amazon Braket with 25 algorithmic qubits. In September 2021, IonQ announced the creation of a joint laboratory with the University of Maryland (UMD), the **Q-Lab**, with $20M funding. Among other things, the lab is tasked with training UMD students on quantum computing. In 2022, they also established business development subsidiaries in Germany and Israel. They announced some new partnership with **Dell** in November 2022 which helped them work with **Aramco**, with **TII** in Abu Dhabi in 2023 as well as with **Bearing Point**. Other partners include HPC cloud computing specialist **Rescale** [1967] (USA) and with **South Carolina Quantum** [1968]. In 2025, they announced various applications-oriented partnerships, one with Einride Partners, an autonomous vehicle fleet operator, to develop quantum computing applications for optimizing autonomous and electric freight fleet operations [1969]. Another with Toyota Tsusho Corporation, to distribute its quantum computing and networking technologies in Japan and a MOU with G-QuAT (Global Research and Development Center for Business by Quantum-AI Technology from AIST). Yet another with Busan Metropolitan City in South Korea, and then in March 2026 with Korea Institute of Science and Technology (KISTI) which acquired a 100-qubit Tempo quantum system in December 2025 which doesn't exist and will probably be converted in a 256-qubit Oxford Ionics generation system. Starting in April 2026, IonQ also part-

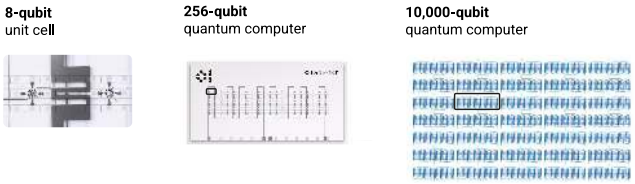


Figure 207: IonQ's roadmap entirely changed with the acquisition of Oxford Ionics, switching from the nebulous algorithmic qubits to real physical and logical qubits. But, as usual, scaling these ion traps will require more time than planned, particularly given the ambitious goal to sustain 99.99% fidelities for two-qubit gate at large scale. At least, when we learn from history. Source: IonQ Technology Update, June 2025 [1956].

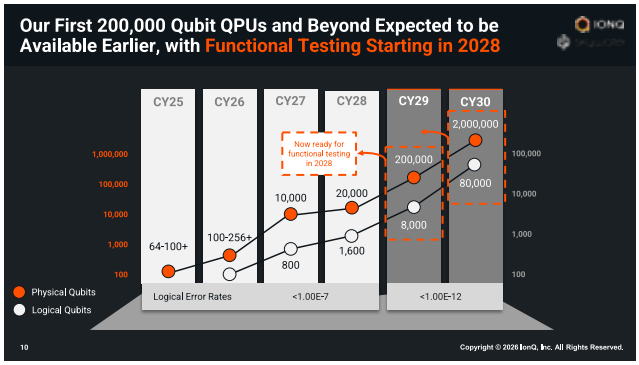


Figure 208: IonQ's updated roadmap after the acquisition of Skywater in January 2026 with pulling the 200K year from 2029 to 2028. They expected to deliver 256 qubits in 2026. In September 2026, the chip commercial availability was delayed until 2027. It is manufactured at Skywater, and the system will be named "Superion" [1965]). They then expect 200,000 qubits in 2028. In their May 2026 presentation, they wisely put the 200K mark back to 2029 and reused their June 2025 roadmap, as shown in Figure 206. Sources: [1950, 1966].

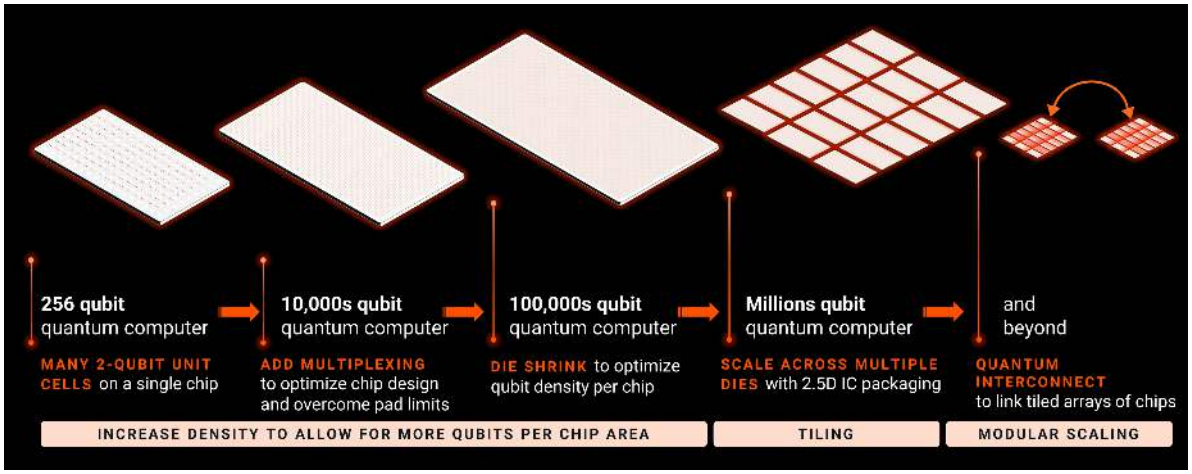


Figure 209: IonQ's roadmap update in May 2026 showing that starting with their 100K qubit chip, they will scale out by assembling multiple chips. They have also labeled their 256-qubit chip as assembling many 2-qubit cells. Source: [1950].

nered with Q-CTRL for the development of optimization solutions. They also work on quantum chemistry with QC-Ware.

Customers. IonQ sold two systems with 35 and then 64 algorithmic qubits to **QuantumBasel**, for their quantum "datacenter" (which is not really an appropriate naming for quantum computing) [1970]. In September 2023, IonQ got an order from **AFRL** to deliver two barium based QPUs for $25.5M, probably Tempo's 64 qubit system, completed by an order of a 4-year $54.4M contract in September 2024 to study QPU quantum networking. It fits a pattern in many countries where defense or civil agencies order pre-quantum advantage QPUs to fund in a non-dilutive way the R&D of the related companies. In September 2024, they announced a new $9M deal with the **University of Maryland**. In the USA, IonQ announced a $22M deal for the upcoming installation of a Forte QPU in Chattanooga in Tennessee and the opening of an office to support training, application development, and the creation of solutions for energy grid optimization. In March 2026, IonQ announced the creation of the IonQ Quantum Innovation Centre at Cambridge University which will host a 256-qubit system as part of a $80M investment. In April 2026, IonQ announced the sale of a 256-qubit system to Horizon Quantum in Singapore, in which IonQ is an investor.

Software. IonQ introduced its software offering for developers in April 2021 with the integration of its tools with IBM's Qiskit. They also support Google Cirq, TensorFlow Quantum, Xanadu Pennylane, Nvidia CUDA-Q, and the qBraid SDK. Their tools contain a hub for accessing IonQ's QPUs, including a web-based console for job submission, monitoring, and results gathering. It

supports both QPUs and emulators, including emulators supporting noise models based on Aria and Forte systems. Their API is JSON based to represent circuits. In December 2024, IonQ announced its redesigned Quantum OS and Hybrid Services suite, which brought a 50% reduction in classical overhead and up to 100x improved accuracy with quantum error mitigation tools.

Use cases. IonQ works with a couple of customers like **Goldman Sachs** on financial services on top of the above-mentioned Hyundai. They also partner with **Accenture** to develop customer applications. They also published various use cases which are far from reaching any quantum advantage given the number of qubits involved. One involved some oversold fancy human cognition modeling using a mere 11 qubits [1971, 1972], a Monte Carlo simulation done with 20 qubits with FCAT, a service subsidiary of **Fidelity**, a financial services company [1973, 1974] and some quantum learning testbed implemented with 4 to 8 qubits [1975] which are therefore far from being "business ready". Other applications worth mentioning were a Quantum Lattice Boltzmann Method (QLBM) for CFD, implemented with a Forte 64-barium qubit system in 2026 [1976] and some work on linear algebra workflow simulated on Nvidia GPU with up to 150 qubits [1977].

They work with **Airbus** on various use cases including QAOA-based cargo plane loading optimizations. IonQ partners with the DoE **Oak Ridge National Laboratory** to develop power grid optimization solutions [1978]. In 2024, they were awarded a phase 1 $5.7M contract from ARLIS, the Applied Research Laboratory for Intelligence and Security from the University of Maryland, which works for the US federal government [1979]. Their work will focus on multi-party quantum computation using blind quantum computing protocols.

In 2025, IonQ published several highly misleading case studies of quantum advantage or potential advantage. The first one, in March 2025, dealt with a case built with ANSYS on solving some optimization problem. It was finding some 12.5% speedup on a particularly simple case, when comparing IonQ Forte system to a PC workstation from 2019 with 4 Intel Xeon CPUs, costing about $25K [1980–1982].

In May 2025, IonQ presented two new hybrid quantum-classical methods enhancing large language models to generate synthetic materials data [1983] and another to fine tune LLMs [1984]. In this last case, the paper presents some energetic advantage for inferences compared to a single Nvidia H100 GPU starting with 46 qubits. It is highly questionable given this comparison is not fair with regards to the system costs which is much lighter for a Nvidia GPU-based system, it didn't account for the error correction overhead that is probably necessary beyond approximately 40 physical qubits and, finally, it was not comparing the QPU solution with a classical LLM solution but with a classical emulation of the quantum code. The cherries on the cake are that the quantum version was tested with only 18 qubits, and the quantum training lasted 90 hours just for this number of qubits. And they didn't provide any quantum computing times for their inferences.

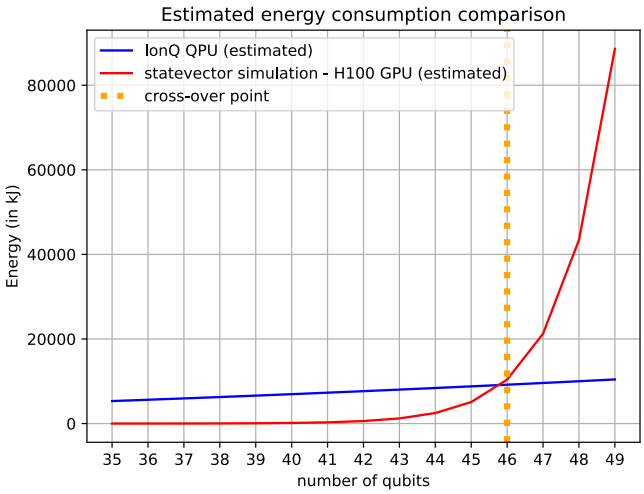


Figure 210: IonQ quantum energetic advantage on a LLM inference case presented in 2025. The comparison is uneven on systems costs. It does not account for the potential overhead of error correction, and it compares the quantum solution to its classical emulation instead of with a classical LLM inference. Source: [1984].

In June 2025, IonQ with AstraZeneca, AWS, and NVIDIA, presented a quantum-accelerated computational chemistry workflow *"which has the potential to power world-changing innovation in healthcare, life sciences, chemistry, and more"*. It was realized with 24 qubits which means that they are still far from any quantum advantage [1985, 1986].

Oxford Ionics

UK, 2019-2025, $47M

Oxford Ionics was a spin-off from the Department of Physics at Oxford University created by Chris Ballance [1987] and Tom Harty which developed a trapped ions QPU with low-noise control electronics. It was acquired by IonQ in June 2025. The UK government approved it at the conditions that Oxford Ionics' hardware and core operations remain in the UK, hardware be hosted in the UK, and the company's staff, IP, and manufacturing capacity must stay domestic. We will see if this holds with time. In 2024, they had opened an office in Boulder, Colorado, to benefit from the US trapped-ion ecosystem.

Manufacturing. They announced in July 2022 that they were teaming up with **Infineon** for the manufacturing of their trapped ions CMOS chips. Meanwhile, Oxford Ionics is also part of an integrated silicon photonic project led by Wave Photonics (UK) funded by Innovate UK with a mere £500K, and in collaboration with the CORNERSTONE silicon photonics foundry at the University of Southampton and the Compound Semiconductor Applications (CSA) Catapult.

Ion traps. In 2023, Oxford Ionics described WISE (Wiring using Integrated Switching Electronics), a proposal to wire an ion-traps chip supporting up to 1,000 ions qubits in a 2D qubit array layout (Figure 212). Ions are moving on the circuit at a speed of 100 m/s, enabling a 5 to 10 μs zone to zone connection speed. They use switches instead of DACs with the benefit of lower power dissipation, plus analog mux and demux components and a 3D chip internal layout (Figure 211).

In July 2024, the company published the first results with their all-electronic voltage control of trapped-ion qubits [121]. They obtained 2-qubit gate fidelities of 99.97%, but without any many-to-many connectivity, which relies on ions shuttling that is equivalent to nearest neighbor connectivity in 2D with solid-state qubits. They were using 10 ions over 7 zones of 2 ions. They also obtained record SPAM error rates below 10^{-5}, although using a heralding technique, with no overhead for computing [130]. Depending on the experiments, they use ^{137}Ba+ ions and ^{43}Ca+ ions [1988]. They improved the performance with 99.99% two-qubit gate fidelity on a system with only two qubits in 2025 with avoiding the technique of groundstate cooling, which could enable faster gate speeds [174]. They planned to build a 256 qubits chip in a couple years as of 2024 [1989].

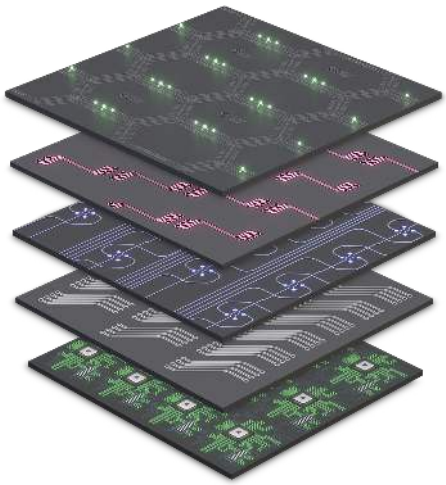


Figure 211: 5-layer QCCD ion-trap circuit from Oxford Ionics. It seems to operate at 20K [1841]. Source: Oxford Ionics.

Roadmap. Oxford Ionics published its roadmap in May 2025, exactly one month before being acquired by IonQ. They were planning to reach 256 physical and 16 logical qubits by 2026, then 10K physical qubits and 700 logical qubits by 2027, which was directly injected into IonQ's roadmap in 2025. In July 2025, they initiated a technology partnership with Iceberg Quantum (Australia) to support qLDPC codes.

Customers. They were selected in September 2024 by the Agency for Innovation in Cyber Security in Germany to build a portable quantum computer for the army as part of a €35M program split over three projects (with them, Quantum Brilliance (NV centers) and neQxt (trapped ions). They also were selected in April 2025 by DARPA in the first phase of the Quantum Benchmark Initiative program.

Quantinuum

USA, 2021, $2,935M

Quantinuum is the result of the merger in June 2021 of Honeywell Quantum Systems (USA, a branch of Honeywell) and the software company Cambridge Quantum Computing (UK), with an investment of $300M for a stake of 55% for Honeywell in the resulting company [1990], with an additional $300M equity in January 2024. The Quantinuum renaming occurred in December 2021. Its main teams are in Boulder, Colorado, Cambridge, UK and in Tokyo (with about 50 people there).

Company. Rajeeb (Raj) Hazra has been Quantinuum's CEO since February 2023, formerly from Micron and Intel. He replaced Ilyas Khan who was previously the founder and CEO of CQC who merged with HQS to become Quantinuum. The company has about 550 people overall as of mid-2025 with offices in Boulder, Minnesota, Washington DC, New Mexico, London, Munich and in Japan. Honeywell started working in quantum computing in 2016 in "stealth" mode. Their team came in particular from the NIST Boulder lab and the University of Colorado with some alumni from the University of Maryland and Christopher Monroe's team (IonQ). In March 2020, they announced the development of a quantum computer that was bound to become be "*the most powerful in the world*", doubling the power of the previous record that was then held by IBM [1991, 1992]. The initial announcement dealt with a four-qubit trapped ions-based quantum processor [1993], its power being evaluated using IBM's quantum volume benchmark. In July 2024, Honeywell was said to plan a $10B valuation IPO for Quantinuum, with the help of JPMorganChase, Mitsui & Co. and Amgen Inc. In May 2025, Quantinuum announced an "up to" $1B investment over 10 years from Qatar taking the form of a Joint Venture with Al Rabban Capital. It is geared at accelerating quantum computing adoption in Qatar and the region. The deal content is not public. It seems to mix commercial activities and some equity investment [1994]. In September 2025, Quantinuum announced a funding round of $500M at a pre-money valuation of $10B, with traditional investors. It then made a real IPO in June 2026, valuing the company at about $20B (as of early July 2026).

Technology. They used QCCD ion traps (for "quantum charge-coupled device") with ytterbium ions coupled with barium ions for cooling. This technique was developed in 2002 by Christopher Monroe, David Wineland and Dave Kielpinski [58]. They are reusing many other works from various research laboratories spread out between 2008 and 2012. Starting with their 98-qubit Helios QPU in 2025, they switched the role of their ions.

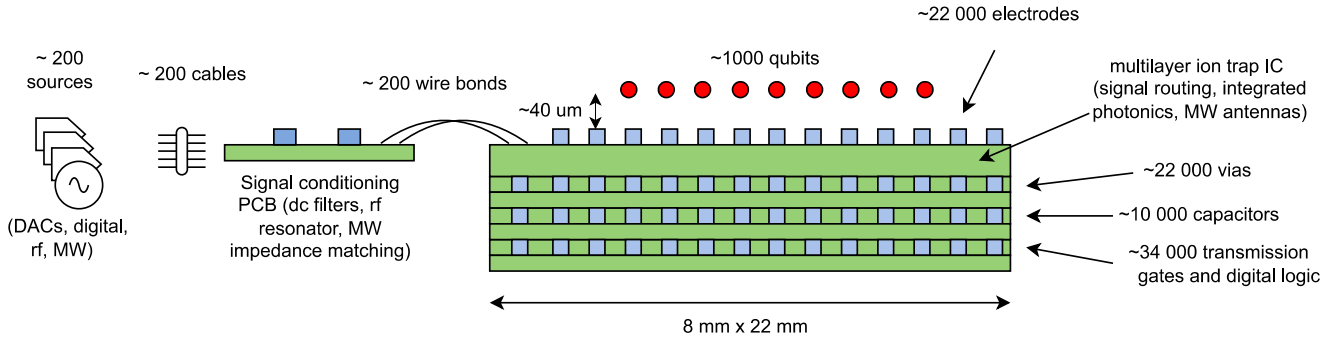


Figure 212: Electrical wiring of a 1000-qubit Oxford Ionics chip. The QPU combines an ion-trap integrated circuit with integrated capacitors and switches and requires a footprint of 8 mm × 22 mm (excluding interconnects). The QPU is controlled using approximately 200 electrical inputs, delivered from approximately 200 off-chip sources via wire bonds. Source: [68].

The data qubits are now barium ions ($^{137}Ba^+$) while ytterbium ions ($^{171}Yb^+$) are used for sympathetic cooling. In previous generations, barium ions were used for cooling while ytterbium ions were used for computing. Ion positioning is supported by 1,228 electrodes in the ion trap.

Ions are generated from a jet of collimated atoms obtained by heating a solid ions target. They are then "hit" by a laser, which removes an electron from the valence layer of the atom (the last one). Only one electron remains in this layer, giving rise to ions with a positive charge. The laser cooling of these ions is well-controlled thanks to their favorable energy level pattern. Thanks to their electrical charge, it is possible to trap and move these atoms using electrostatic and radiofrequency potentials. The ions quantum states correspond to two "hyperfine" energy states related to the interaction between the magnetic moment of the nucleus and that of the electrons of the ion.

Like most trapped ions vendors, Quantinuum uses ions shuttling, a technique proposed in 2002 by Dave Wineland and co. It prepares atoms, ionizes them and sends them into a hole that feeds their chip. It then uses ions storage and sorting areas. The ions were confined above a rail of three rows of electrodes whose variable voltage control their position and move them laterally. It enabled logical operations between several qubits while moving them at will between storage areas and interaction areas during operations. Their first system used 198 direct current (DC) electrodes for controlling the displacement and positioning of ytterbium ions coupled with barium ions used for cooling. The chip used cryogenic surface traps dynamically rearranging the position of the ytterbium/barium ion pairs and implementing quantum gates running in parallel on several areas of the circuit. Ions circulated above the green band, allowing arbitrary movements of the ions along the band. Once positioned, they were transferred to the middle band to get submitted to a single-qubit quantum gate, or in the side bands for two-qubit quantum gates. One of these operations is a SWAP gate that allows the ions to be physically interchanged. Helios is using a completely different arrangement as shown in Figure 214.

Figure 213: Quantinuum Helios installation shows on the right the experiment location and on the left all the racks with laser and control electronics. The system cryogenics is fed a helium liquefier. It cools the ions chamber at about 15 K. The total system power is of about 34 kW. Source: Quantinuum, November 2025.

Cooling. Their initial system operated at 12.6 K with a temperature stability of about 2 mK. Cryogenic operation suppresses several technical noise sources, including anomalous motional heating. This cryogenic cooling of the trap is distinct from laser cooling of the ions' motion. Quantinuum uses a second ion species as a sympathetic coolant: laser cooling is applied to the coolant ions, and Coulomb coupling transfers motional energy out of the shared normal modes without directly driving the data-qubit internal states. Depending on the generation, Doppler cooling and resolved-sideband or Raman-sideband cooling are used in the cooling sequence. Helios reverses the earlier species roles, using ^{137}Ba$^+$ data qubits and ^{171}Yb$^+$ coolant ions [119]. Helios operates its trap at about 15 K (Figure 213).

Qubit gates. Helios uses 7 lasers in total: a 369 nm laser for ytterbium ions sympathetic cooling, a pair of 515 nm lasers with 8 GHz frequency splitting for single gate and Mølmer–Sørensen two-qubit gates ($R_{zz}(\theta)$), 614 nm and 1,762 nm lasers for state preparation, 1,762 nm being used to avoid measurement crosstalk and leak-

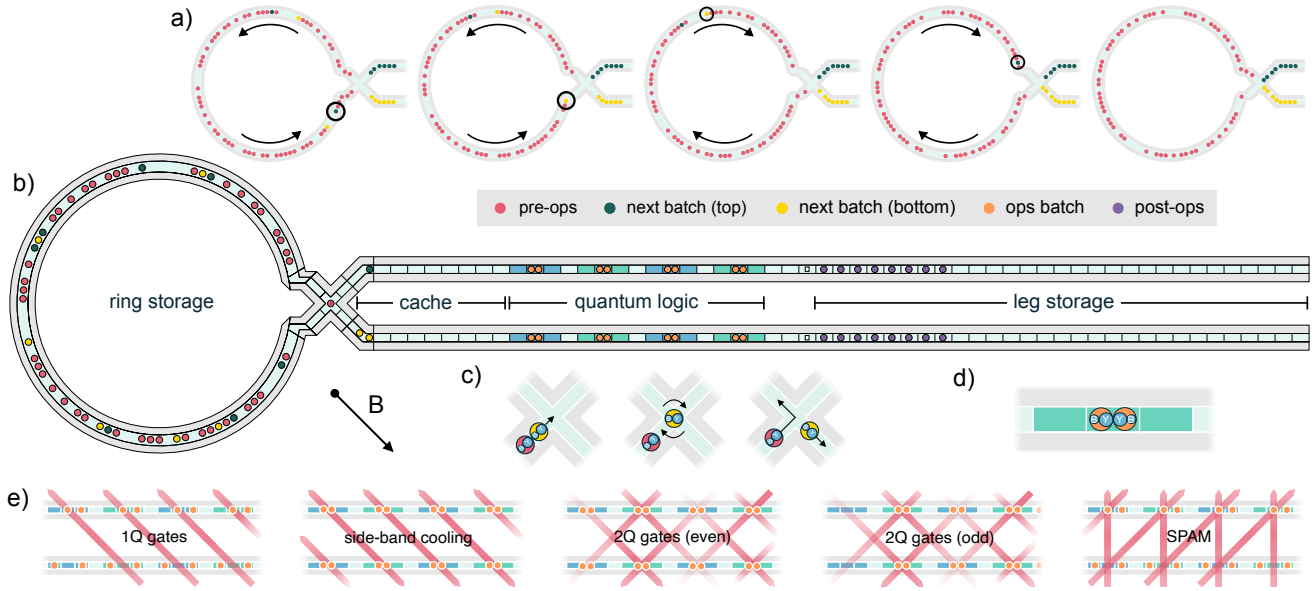


Figure 214: Quantinuum Helios is using different qubit zones with a circle shape ring storage memory region for qubit storage used as a random-access memory, connected through a four-way X junction to an intermediate cache zone and a gate zone for single-qubit gates, two-qubit gates and qubit readout, and a leg storage used as a first in, last out memory. The readout operation zone can accommodate for 16 ions and support 4 single or two-qubit gates in parallel at a time. Laser light is delivered to the ions in the gate zone using some in-chip integrated beam delivery and MEMS mirrors. Source: [119].

age errors, and finally, 493 nm and 650 nm lasers for fluorescence readout. Previous QPUs were using 370.3 nm Raman beams in circular polarization for single qubit gates and pairs of laser for two-qubit gates. Two ions are thus moved by the electrodes into the same potential well before being coupled by laser. The qubits can then be separated and moved elsewhere to interact with other qubits.

Gate speed. Gate operations are quite slow, given the ions shuttling required between zones. First generations has shuttling times of about 5 ms. In Helios, it became even worse since it takes about 40 ms to move ions from the storage to the computing zone. The time per layer with 98 qubits is between 40 to 55 ms. 300 μs of cooling time is also needed after two qubit gates (IonQ/Oxford Ionics found a way to escape this [174]).

Qubits readout is performed with a classical imager that detects the energetic state of the ions via their laser-activated fluorescence. This imager is a PMT array, i.e. a linear array of photomultipliers (Photo-Multiplier Tubes). Their architecture allows mid-circuit readout, without disturbing the neighboring qubits. This enables conditional logic, with IF THEN ELSE like with classical programming.

From 1D to 2D. Quantinuum started with a 1D trapped-ion bar. They planned to adopt a 2D bar layout that would allow them to move the ions in two directions and accumulate more of them and connect them with their neighbors in two dimensions [1995]. In 2023, they launched a "racetrack" 1D close circuit layout with their H2-1 QPU as shown in Figure 216 and described in detail in Figure 215. It added a Magneto Optical Trap (MOT) that replaces the oven used in system H1. It reduced startup time by cooling the atoms before sending them in the trap. Quantinuum later plan is to use ion shuttling in 2D arrays, leading to some optimization techniques to move the ions around and minimize its overhead [1996]. They then moved to the Helios layout in 2025 as already shown in Figure 214.

They also implement more efficient RF electronic signals routing with additional metal layers beneath the trap top metal layer and voltage broadcasting which ties external signals sources to multiple DC electrodes in the trap and relies on conveyor belt regions on each side of the trap where ions are stored. Thanks to the use of only three voltage signals for 20 ion wells on each side of the trap, it greatly improves electrode control efficiency [1997].

Manufacturing. In November 2024, Quantinuum announced that **Infineon** would manufacture their ion traps. This became a specialty of Infineon which also works with AQT and Oxford Ionics. Their chips are currently manufactured in Villach in the south of Austria, near Slovenia.

Interconnect. Quantinuum is partnering since February 2025 with Mitsubishi Electric, Keio University, SoftBank, Mitsui & Co., Yokohama National University, and LQUOM to develop QPU quantum interconnect technologies. This includes the creation of quantum memories, quantum repeaters (by LQUOM), high-efficiency transducers, subsystems for stabilizing transmission paths, and control systems for QPUs [1998].

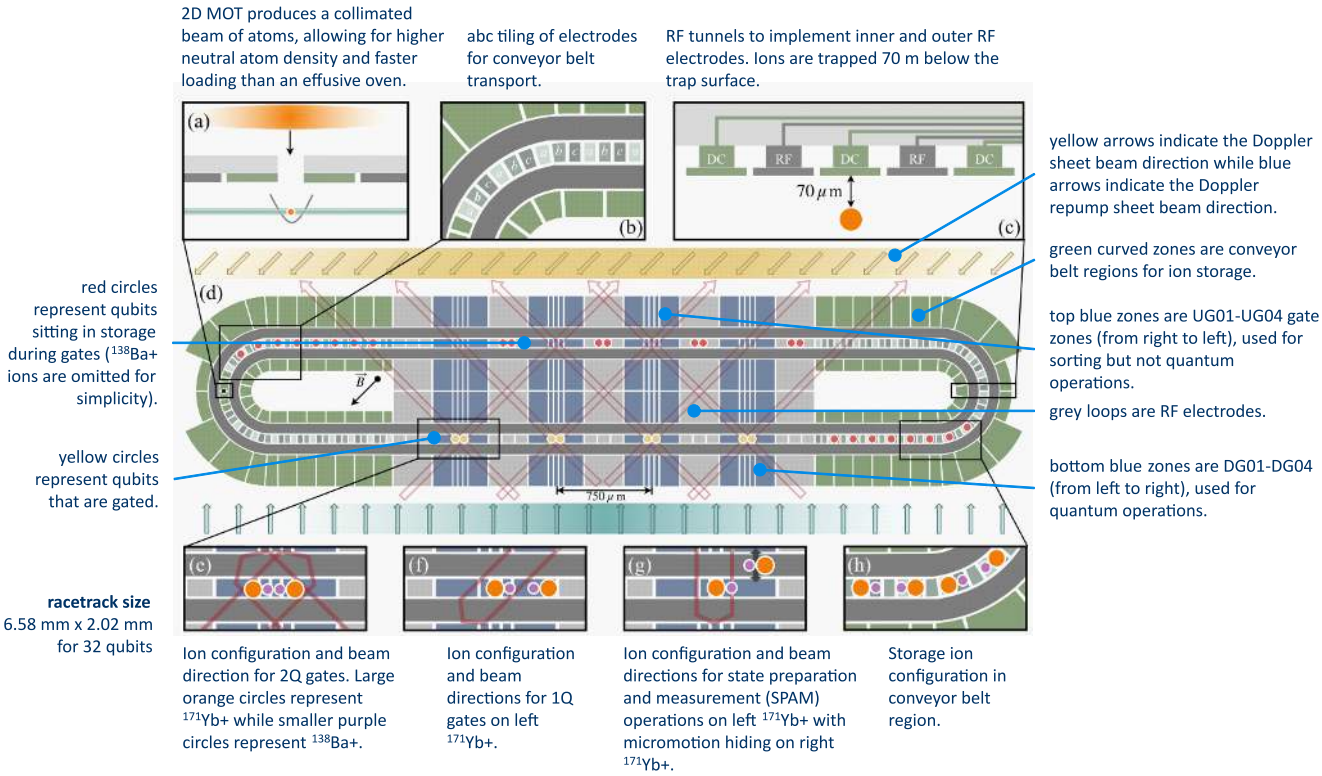


Figure 215: The layout of the "race track" processor released in 2023. Source: [1997].

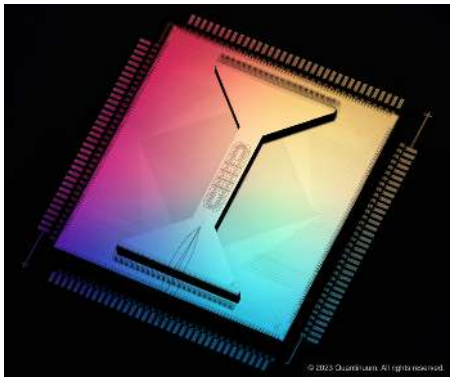


Figure 216: The "race track" processor released in 2023. It is a similar processor that supported 56 qubits in 2024. Source: [1997].

Qubit fidelities have always been very good. They launched their 6-qubit H0 system in June 2020, then their 10-qubits H1 system in October 2020 with an initial quantum volume of 128 (7 qubits x 7 gates depth). Their quantum volume reached 512 in March 2021 (9×9 qubits with 10 qubits). Single-qubit gate fidelities were above 99.991% and two-qubit gate fidelity above 99.76% while readout fidelity is at 99.75% with a measurement crosstalk at 0.2%, characterized as the decay of a qubit coherence in an equal superposition state, while repeatedly measuring the nearest qubit [1999].

As of April 2022, they had 12 running qubits reaching a quantum volume of 2^{12} with their System Model H1-2. It is a rare quantum processor with a quantum volume reached with all available qubits. Their related fidelities were 99.994% for single-qubit gates, 99.81% for two-qubit gates and 99.72% for qubits readout [2000]. Meanwhile, their H1-1 system launched in June 2022 had 20 qubits (despite a lower "version" number), which enabled them in September 2022 to reach a QV of 8,192 (2^{13}) [2001] (Figure 217). This system added arbitrary-angle two-qubit gates, which can shorten circuits such as those relying on a QFT (quantum Fourier transform). As of June 2023, their record quantum volume was 2^{19} with an H1-1 system using 20 qubits [2002]. In May 2025, Quantinuum reached a QV of $2^{23} = 8,388,608$ [2003], which then increased to 2^{25} in September. The peer-reviewed Helios characterization reports average infidelities of $2.5(1) \times 10^{-5}$ for single-qubit gates, $7.9(2) \times 10^{-4}$ for two-qubit gates and $3.3(5) \times 10^{-4}$ for SPAM, corresponding respectively to fidelities of about 99.9975%, 99.921% and 99.967% [119].

Error correction. Quantinuum's has a long history with quantum error correction that we will describe here step by step:

- 2021: first logical qubits using color codes with their 10-qubit QPU and real-time error correction [2005].
- 2022: 8 corrected logical qubits encoding in 10 physical qubits using their in-house Iceberg stabilizer code on a 12-qubit H1-2 QPU [2006]. The system had a quantum volume of only 2^8. In 2023, the $[\![6, 4, 2]\!]$ error detection code was used to run a small QPE supporting 920 physical two-qubit gates with 4 logical qubits [2007]. In 2025, they proposed a way to optimize the co-compilation of the algorithm code and this error detection Iceberg code [2008].

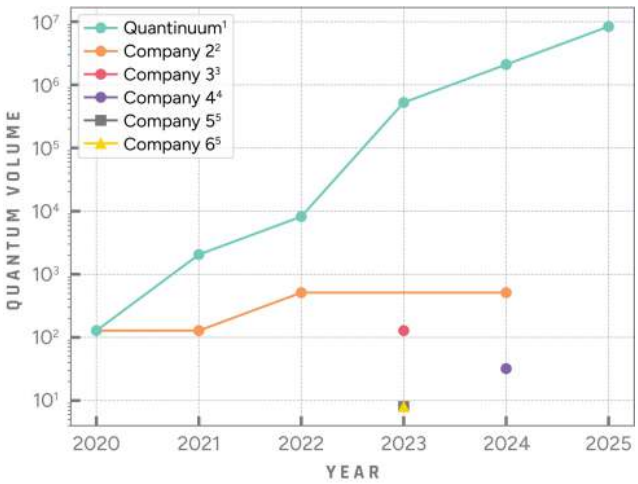


Figure 217: Evolution of Quantinuum systems quantum volume from 2020 to 2025. Source: [2003].

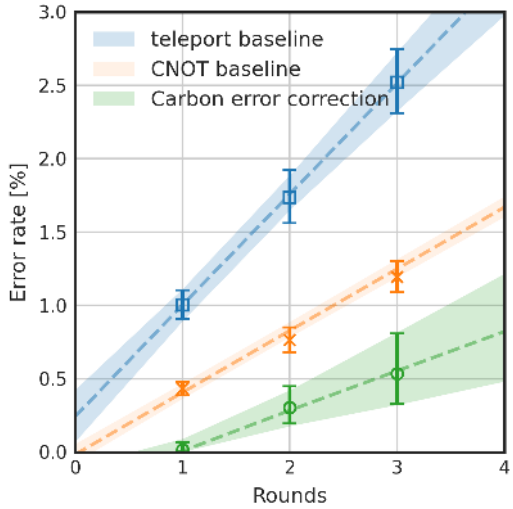


Figure 218: Figure 7 from the revised [2004] showing that the fidelity gain with Quantinuum's logical qubits happens only once.

- 2022: fidelity of logical CNOT and SPAM is better than with physical qubits using a 5-qubit $[\![5,1,3]\!]$ code and a $[\![7,1,3]\!]$ color code [2009].

- 2024: topological code with 27 qubits in 2024 [2010] and a GHZ entangled state of 32 qubits with a fidelity of 82%. This is a state superposing two computational basis states where all the qubits are either with values $|0\rangle$ or $|1\rangle$.

- 2024: fault-tolerant teleportation of a logical qubit with a fidelity of 97.5% [2011]. They simulated a non-Abelian topological order with their qubit, showing another potential technique to create protected logical qubits [2012].

- 2024-2026: with Microsoft, Quantinuum demonstrated logical error rates below corresponding physical-circuit baselines [2004, 2013]. The largest reported gain, about ×800, applied to a specific Bell-state preparation experiment, where the circuit error rate fell from about 8×10^{-3} for the physical baseline to about 10^{-5} for the encoded circuit. It used error detection, correction and post-selection, but the ×800 figure can't be interpreted as a general logical-gate fidelity improvement. However, the later peer-reviewed Nature paper also demonstrated repeated error correction during computation, with gains ranging from ×11 to ×800 depending on the protocol. Therefore, the earlier criticism that the benefit "can only be used once in the circuit" is no longer correct.

- 2024: three logical qubits to run a quantum Fourier transform (QFT), using a simple $[\![7,1,3]\!]$ Steane correction code, which created logical two-qubit gate average fidelities of 99.91% on their H1-1 QPU and 99.8% on the H2-1 [2014].

- 2024: support of 56 qubits with a many-to-many two-qubit gate fidelity of 99.84% on a H2-1 QPU using the same racetrack QCCD design as in 2023. It enabled them to show that, thanks to good qubit connectivity and better qubit fidelities, their system's circuits are way more difficult to simulate classically with tensor networks (although, with no input data) [2015].

- 2024: with the same chip, Quantinuum then achieved another interesting result by creating a 4-logical qubit GHZ state with a fidelity of 99.5%, after post-selecting 98% of the outcome, a much better result than Lukin's December 2023 paper with cold atoms. They were using a Tanner variation of a surface code encoding 4 logical qubits into 25 physical qubits [2016].

- 2024: "genon braiding", a concept in the study of topological phases of matter and braided toric codes and how it could be used to create logical gates using fewer physical qubits per logical qubit, in so-called "high rate" QECC. It involves sharing physical qubits between logical qubits which bring a load of operational challenges [2017].

- 2024: 4D surface code, leveraging the many-to-many connectivity of their H2-1 system. It enables single shot (faster) error correction [2018].

- 2024: 12 logical qubits were implemented on the 56-physical-qubit H2 system with Microsoft, including logical GHZ states of 4, 8 and 12 qubits [2019]. The experiment used three blocks of the tesseract subsystem color code, which encodes four logical qubits in 16 data qubits with distance four, rather than the parent $[\![16,6,4]\!]$ tesseract code. The logical circuit error rate improved by about one order of magnitude for the deeper repeated-error-correction

experiments (Figure 219). The protocols used rejection and post-selection with acceptance probabilities that decrease with circuit structure and number of correction rounds. This overhead is an important scalability issue, but it does not invalidate the demonstrated below-break-even error suppression. At that time the experiment did not yet demonstrate a complete universal logical gate set, which was addressed separately by later non-Clifford magic-state work.

Experiment	Qubits	Baseline error rate	Encoded error rate	Gain
Path-4	4	1.5(2)%	$0.10^{+0.11}_{-0.06}$%	15×
Cube-8	8	2.3(3)%	$0.2^{+0.2}_{-0.1}$%	11×
$\frac{\|0^{12}\rangle+\|1^{12}\rangle}{\sqrt{2}}$ Cat-12	12	2.4(3)%	$0.11^{+0.16}_{-0.08}$%	22×
Error correction 5×	4	2.7(4)%	$0.11^{+0.21}_{-0.09}$%	24×
	8	5.6(6)%	$0.7^{+0.7}_{-0.4}$%	8×

Figure 219: Logical (encoded error rate) and physical (baseline error rate) error rates for GHZ states with 4, 8 and 12 qubits showing the fidelity gains. These are significant compared to all other such benchmarks done in 2023/2024. Source: [2019].

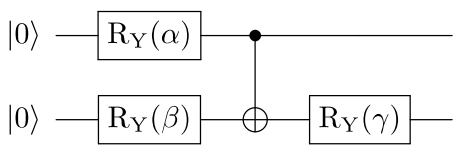


Figure 220: The circuit executed by Microsoft and Quantinuum with two logical qubits to conduct a very simple chemical simulation that can obviously be computed classically more efficiently. This kind of shallow circuit is far from representing large scale algorithms requiring FTQC QPU capabilities. Source: [2020].

- 2024: end-to-end chemical simulation using two of their logical qubits, also with Microsoft [2021]. It was presented as a worldwide premiere which is questionable, but it depends on the definition. It may be one with logical qubits, but the exhibited quantum computing capacity lagged behind some experiments done in Japan by IBM and Fujitsu, using NISQ QPUs and quantum error mitigation with way more physical qubits.

- 2024: another topological qubit using a Z3 toric code state on 24 qutrits with fidelity per qutrit exceeding 96.5%. It manipulated two types of defects: a parafermion, and its bound state which is related to charge conjugation symmetry. They demonstrated fusion detection and the transfer of entanglement between anyons and defects, which is the base for controlling topological qutrits. This is an alternative route but not the main one for Quantinuum [2010, 2012, 2022].

- 2025: decoherence-free subspace quantum error correction code with long probe times that extends quantum memory time by over an order of magnitude compared to physical qubits [2023].

- 2025: they experimented a $[\![6,2,2]\!]$ error-detecting code on H1-1 which produced logical magic states with an experimental infidelity of $7^{+3}_{-1} \times 10^{-5}$ and a discard rate of about 14.8%. They used them to implement a controlled-Hadamard non-Clifford gate with logical infidelity at most $2.3^{+9}_{-9} \times 10^{-4}$, below the approximately 10^{-3} unencoded baseline [2024]. The $\sim 10^{-10}$ performance corresponded to a circuit-level simulation for a self-concatenated $[\![36,4,4]\!]$ code at a physical two-qubit error rate of 10^{-3}, not an experimental result.

- 2025: code switching between the $[\![15,1,3]\!]$ quantum Reed-Muller code and the $[\![7,1,3]\!]$ Steane code produced an encoded magic state in the Steane code with an acceptance probability of 82.58% and an infidelity bounded by $5.1(2.7) \times 10^{-4}$ [2025]. The single-copy experiment used 28 physical qubits in total, including data and ancilla qubits. Code switching transfers a logical state between codes with complementary transversal gate sets and can therefore help circumvent the Eastin-Knill restriction on universal transversal gates. The demonstrated protocol switched from a 3D quantum Reed-Muller color code to the 2D Steane color code.

  After preparing four magic states in $[\![36,4,4]\!]$, before escaping to a higher-distance code, they would use code switching from $[\![36,4,4]\!]$ to $[\![16,4,4]\!]$ codes to reduce the encoding overhead, using fault-tolerant code switching between $[\![6,2,2]\!]$ and $[\![4,2,2]\!]$. Then, four such $[\![16,4,4]\!]$ codeblocks, each containing 4 magic states, could be teleported into a $[\![256,16,16]\!] = [\![4^4,2^4,2^4]\!]$ code via level-raising teleportation. The protocol would generate 16 magic states using 127 physical qubits per magic state and could be done in depth 5, assuming that two ancillaries $[\![256,16,16]\!]$ code blocks are prepared in parallel with the magic state protocol. It would require 1,015 physical qubits to fault-tolerantly initialize two $[\![256,16,16]\!]$ code blocks. This qubit overhead would be lower than with the magic state cultivation protocol introduced by Craig Gidney from Google in 2024 [916].

  As a reminder, the notation $[\![n,k,d]\!]$ characterizes a quantum error-correcting code, with n being the number of physical qubits, k, the number of logical qubits being encoded with these physical qubits and d, the code distance, which indicates the minimum number of physical qubit errors required to transform one logical codeword into another. A distance-2 code is a quantum error-detecting code, that can detect a single qubit error but cannot correct it without additional information or repetition. But you need more than n physical qubits to implement these codes.

- 2026: they mentioned having created 48 logical qubits on their Helios 98-qubit QPU released in November

2025. These were documented in 2026 [120]. Two-qubit gate fidelities reached a record 99.92%, the best ever for a commercial system with such a number of qubits. They obtained a logical error rate of 1.2×10^{-4} per two-qubit gate vs physical errors of about 8×10^{-4}. On Helios, they tested QEC/FTQC features using their error detection Iceberg codes with QAOA for a simple portfolio optimization using 5 to 12 logical qubits and HHL with 5 logical qubits applied to the Poisson equation using a $[\![7,1,3]\!]$ Steane code which enables transversal Hadamard gates. However, their logical Hadamard is prepared using a repeat-until-success (RUS) approach which presumably doesn't scale well for large circuit. With 12 logical qubits and 2,132 physical two-qubit gates, they claim "better-than-random" performance which is a weird statement. They also implemented a pFT (partial fault-tolerant) approach with FTQC applied to Clifford gates, but not to arbitrary rotations, using concatenated Iceberg codes and what they deem is some "reasonable" postselection [2026]. In September 2026, they demonstrated on Helios a new approach using a $[\![20,2,6]\!]$ code named C_4-Helix, supporting two logical qubits and Clifford group operations, a three-logical qubit GHZ state generation with a distance-5 surface code, completed by a blueprint proposal to support magic states [2027].

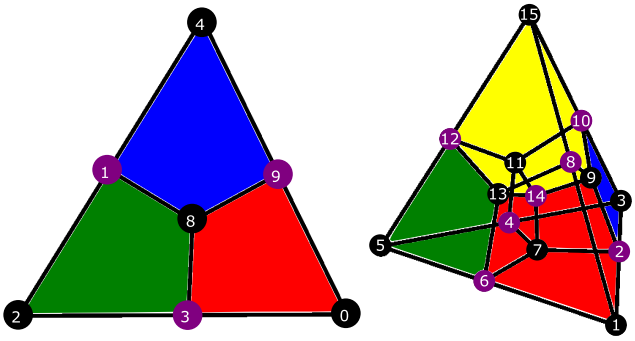


Figure 221: Visualization of a 7-qubit 2D Steane code $[[7,1,3]]$ and 15-qubit quantum Reed-Muller (qRM) $[\![15,1,3]\!]$ 3D code. Source: [2024].

Roadmap. In September 2024, Quantinuum updated its roadmap which was so far respected (Figure 222). They plan to assemble thousands of physical qubits and hundreds of logical qubits by 2030 with error rates below 10^{-6}, which can be positioned in the early stages of the FTQC era. One question arises with their 2D QCCD layout: will it enable many-to-many qubit connectivity like they do with their H2 racetrack design. This layout seen on their upcoming SOL and APOLLO generations seems to rely a lot on ion shuttling to enable qubits connectivity. For more on this, you can listen to a podcast I recorded with Chris Langer from Quantinuum in February 2025 [2028].

Software tools. Let's have look at Quantinuum software stack:

- **TKET** (September 2021) is Quantinuum's open-source toolkit, the equivalent of IBM's Qiskit. It was originally created by Cambridge Quantum Computing before its merger with HQS to create Quantinuum.
- **InQuanto** (May 2022), a quantum computational chemistry software platform that was developed with the support of BMW, Honeywell, JSR, Mitsui& Co, Nippon Steel Corporation and TotalEnergies. The platform makes it possible to associate various quantum algorithms coupled with chemistry-specific noise-mitigation techniques running on NISQ systems. It also breaks down larger problems into smaller subproblems that fit existing NISQ machines. InQuanto is based on Quantinuum open-source toolkit **TKET**.
- **lambeq** (March 2022), a Python library that "*converts any natural language sentence into a quantum circuit*" that contains Bobcat, a neural-based Combinatory Categorial Grammar (CCG) parser, Bobcat. It is used to pre-process natural language training data to be subsequently used for various NLP applications (classification, summaries, etc.). Quantinuum used AlphaTensor from Google DeepMind to reduce the number of T gates required for FTQC algorithms [2032].
- **Quixer** (July 2024), a quantum transformer [2033] based on LCU (Linear Combination of Unitaries) and QSVT (Quantum Singular Value Transform) quantum algorithms. It was evaluated on a dataset with 966K training tokens, 77K validation tokens, and 86K test tokens, and tested on 6 qubits. Still, it was not faring better than a regular classical Transformer [2034].
- **Nexus** (July 2024), a cloud platform that enables users to run, review, and collaborate on quantum computing projects. It contains a typical batch manager to run or emulate your quantum circuits, associated APIs to run your Python scripts, and supports InQuanto and TKET V2 [2035].
- A simulation of the dynamics of some quantum Ising model in 2025 to observe the emergence of Floquet prethermalization on timescales, where accurate classical simulations are challenging, with a circuit containing 2,000 two-qubit gates [2036] (Figure 223).
- **Guppy**, an open-source Python-based programming language, and **Selene**, a platform that partially emulates the 98-qubit Helios QPU, were introduced in 2025. Guppy supports structured and dynamic software with real-time feedback and programming constructs such as 'if' statements and 'for' loops. It also connects with Nvidia CUDA-Q for hybrid workflows. In the Helios random-circuit-sampling benchmark, Quantinuum estimated the classical tensor-network sampling cost under specified memory and GPU-efficiency assumptions. The extremely large quoted power-equivalent values, reaching around 10^{73} W for

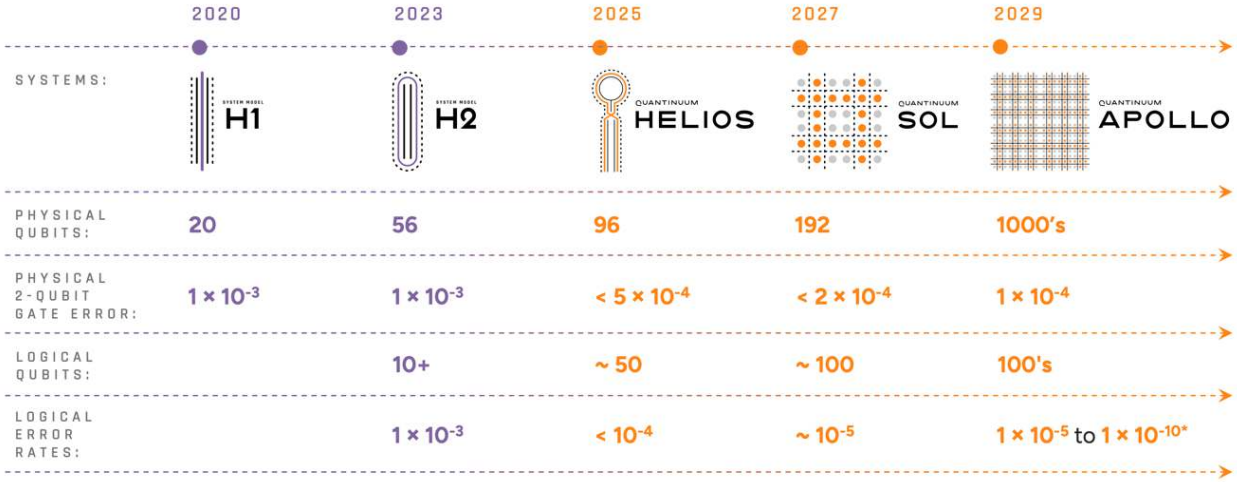


Figure 222: Quantinuum 2024 roadmap. Quantinuum launched its Helios QPU with 98 qubits in November 2025, and several associated case studies including an improved QRNG. Source: [119, 2029–2031].

some instances, are extrapolated computational-cost equivalents, not measured power consumption and not a general lower bound on classical simulation [119].

Customers. Quantinuum customers include **DHL**, **Merck**, **Accenture**, **Samsung**, who works on new batteries designs, **JPMorganChase** to create quantum algorithms in the financial sector, as well as **Amgen**, **Sanger Institute**, **Inquanto** and **Crown Bioscience** in life sciences, and **Aramco**. They also work with **JSR Corporation** (Japan) to improve semiconductor design and research with organic and inorganic materials. In May 2023, **HSBC** announced it was to use Quantinuum Quantum Origin QRNG solution based on using their QPU in their cybersecurity deployments, on top of some PQC. HSBC also investigates future QML use cases, including NLP cases [2037]. Quantinuum sold a 20-qubit system nicknamed Reimei to **RIKEN** in Japan in January 2024 which was operational in February 2025 [2038]. According to RIKEN, this installation's power is 12 kW for the Reimei QPU and 100 kW for the total system when you include the HVAC, chilled water production, UPS, orchestration servers and network gateways [2039]. Quantinuum was also accepted in the second phase of the DARPA QBI program in November 2025. At last, it sold a Helios QPU to A*Star in Singapore in November 2025, to be installed in 2026.

Case studies. Quantinuum and its customers or partners published several early stage case studies, some of which are nearing a computational quantum advantage:

- A team from **JP Morgan Chase Bank** and the **University of Maryland** published a paper in July 2022 saying that a (Quantinuum) QPU may be better at summarizing long documents [2040]. It was a hybrid algorithm with a classical part analyzing a dataset of 300,000 news articles from CNN and the Daily Mail and precomputed with a BERT NLP classical deep learning model that handles sentences extraction and converted them into vectors. The experiment summarized text from respectively 20 to 8 and 14 to 8 sentences, corresponding to the number of used qubits in Quantinuum QPUs versions H1-1 and H1-2. On the H1-1, 765 two-qubit gates with a computing depth of 159 were run on 2,000 shots. The experiment was based on using three quantum optimization algorithms working under constraints: QAOA, L-VQE [2041] and XY-QAOA and the comparison was made vs a classical random guess, with XY-QAOA being the best. Its capability was limited to simple and short texts. It could not summarize a 300-sentence document given there are not enough physical qubits available with sufficient fidelities. Since then, Quantinuum has been overselling a little the benefits of quantum AI with natural language processing [2042].
- With **Oak Ridge National Laboratories**, Quantinuum tested in 2023 some quantum physics simulation, that was tested on 20 qubits. It would deliver some quantum advantage with 70 qubits [2043].
- In September 2023, Quantinuum released an interesting paper showcasing a use case involving superconductivity physics simulation, using 32 qubits, which is quite rare nowadays [2044].
- In April 2024, Quantinuum did create some combinatorial optimization algorithm to solve a Max-Cut problem, finding that a quantum advantage would require about 1,000 physical qubits [2045, 2046].
- In September 2024, they showcased a simple spinless Fermi-Hubbard fermionic simulation run with 48 qubits [2047] and interesting chemical simulations although using only 8 qubits [2048].
- **Generative Quantum AI** *aka* GenQAI was proposed in February 2025, which is based on the Generative Quantum Eigensolver (GQE) which uses

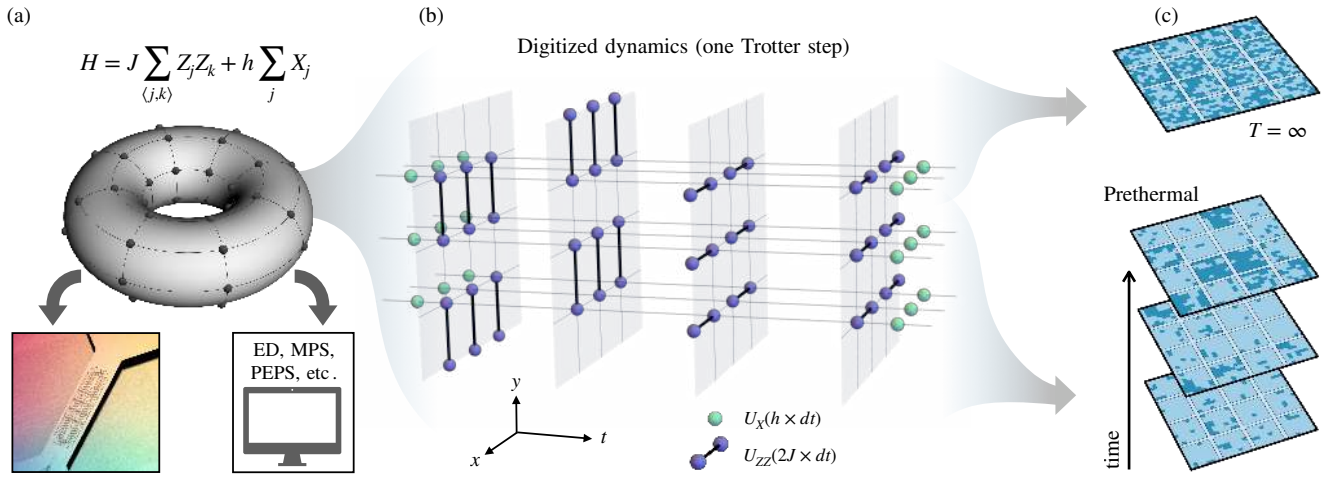


Figure 223: Quantinuum's process for digitizing a 3D Ising quantum magnet on the H2 QPU on a 7×8 rectangular lattice that was compared to a classical simulation. Source: [2036].

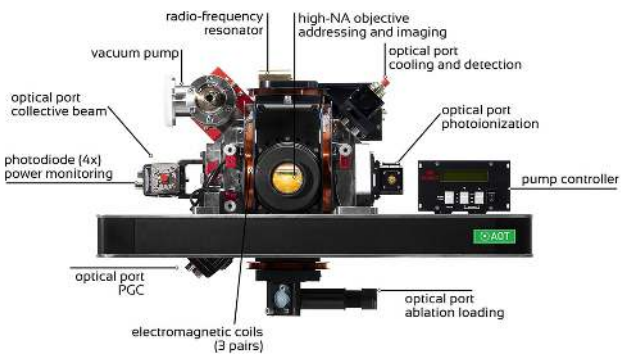


Figure 224: AQT PINE QPU setup. Source: [2049].

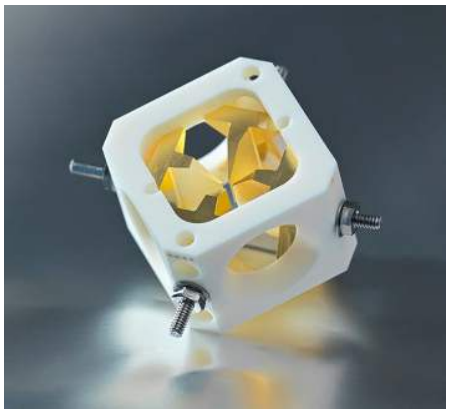


Figure 225: AQT PINE system to trap their calcium ions.

quantum-generated data to train a Transformer-based machine learning model that proposes better quantum circuits in a feedback loop [2050]. In a nutshell: quantum data helps train a classical Transformer-based AI which helps tune a quantum circuit, to find a chemical ground state. It was tested at small scale with H_2, and unfortunately, with no information on how the process would scale with a large number of orbitals [2051].

- A demonstration in May 2025 with RIKEN of an end-to-end QPE pipeline with partial fault-tolerance using a Steane code for a quantum computation of the electronic structure of molecular systems, tested with dihydrogen H_2. It was running on 22 qubits and 2,000 two-qubit gates, which is under the advantage threshold [2052]. The same team computed photo-induced biomolecular chemical reactions and excited-state energies in 2026, using the Fugaku HPC and 20 qubit on the nearby Quantinuum system, meaning that the workload is essentially classical [2053].

- The **Quantum Paldus Transform** algorithm proposed in June 2025, which can help solve the electronic structure problem in quantum chemistry, with a system made of d spatial electron orbitals. It is based on block-diagonalising fermionic, spin-free Hamiltonians in the second quantisation. The algorithm size scales with $\mathcal{O}(d^3)$ Toffoli gates, and FTQC resource estimates are provided, which could then bring some exponential speedup vs classical equivalents [2054].

- **Qubit Pharmaceuticals** scientists implemented a quantum Markov Chain Monte Carlo workflow on H2 and Helios in 2026. One reported amplitude-estimation circuit used 6 qubits and 237 gates [2055]. This experiment does not establish a generic circuit-size limit for H2 or Helios: tolerable depth depends strongly on the gate mix, connectivity, measurement/reset operations, compilation and the success metric, and other Helios benchmarks execute much larger circuit families.

- **Lattice gauge theories** and Hamiltonian dynamics simulation with their H2-1 system, published in 2026 [2056].

- **1D Heisenberg model** simulation with the University of Tokyo in July 2026, using the Reimei system installed in Japan [2057].

AQT

Austria, 2017, $34.8M

Alpine Quantum Technologies (AQT) is a spin-off from the University of Innsbruck created by Rainer Blatt, Peter Zoller and Thomas Monz (CEO). Ignacio Cirac (MPI) and Jonathan Home (ETH Zurich) are among their scientific advisors. They were about 35 people as of mid-2025.

Technology. AQT uses calcium ($^{40}Ca^+$) trapped ions. The qubit is optical, encoded in the $S_{1/2}$ ground state and the metastable $D_{5/2}$ state connected by a quadrupole transition at 729 nm. Targeted 729 nm laser pulses create single-qubit gates and a bichromatic 729 nm field, detuned around the motional sidebands, implements Mølmer–Sørensen (MS) two-qubit gates, while 397 nm serves for Doppler cooling and fluorescence readout [2058–2061].

The fidelity of their qubits was 99.6% for two qubits and dropped to 86% for 10 qubits in 2019 [1908]. AQT has 20 working qubits working out of two 19-inches datacenter rack with 99.96% single-qubit gate fidelity and 99.847% two-qubit gate fidelity. The associated research team had already entangled 14 ions back in 2011 [2062]. It reached 24 qubits in 2023.

Their PINE system uses a linear Paul trap that supports up to 50 ions, including from multiple species (Figure 224). It can be used beyond quantum computing for quantum clocks or spectroscopy experiments. AQT is also experimenting using qudits of dimension 5 with its ions [2063]. They also manufacture and sell IVY, an 729 nm optical filter Fabry–Pérot cavity module that suppresses high frequency phase noise from an incoming laser light.

On top of the PINE system, they also developed the BEECH diode lasers and control system which provides frequency stabilization of the lasers they used covering 397 nm for Doppler cooling, 423 nm for photoionization, 866 nm for repumping and 854 nm for shelving. The 729 nm laser is handled separately.

In 2024, AQT and their research partners demonstrated a 2D architecture using a QCCD ion trap, developed and manufactured with Infineon on a fused silica substrate. They label it a Quantum Spring Array (QSA). It uses registers made of 6-ion strings which are displaced using axial and radial ion transport instead of individual ion shuttling [2064, 2065] (Figure 228). They use laser wave guides made with aluminum nitride (AlN) and aluminum oxide (Al_2O_3) which support wide bandgaps and low optical losses in the 397 and 729 nm wavelengths used to control calcium ions and 866 nm used to cool them. In 2025, they proposed an heterostructure architecture for an ion-trap that would convey all electric signals as well as light signals in wave guides and dedicated optics for the laser control of individual ions [1857] (Figure 226). Its experimental realization was presented in a preprint in August 2026 [2066].

In 2023, they obtained a quantum volume of 128 (7 qubits) with this PINE QPU, which is behind the state of the art in trapped ions as we've seen with IonQ and Quantinuum results [2068]. In 2026, their supported quantum volume reached 32,768 (15 qubits) with a LYNX system which was introduced in May 2026, a record for a European hardware vendor at the time.

Logical qubits. In May 2022, Thomas Monz's team announced the first realization of a fault-tolerant CNOT gate across two logical qubits made with 16 physical qubits and using 7-qubits color codes quantum error correction plus one measurement qubit (in Figure 227, *right*, so $16 = 2 \times (7 + 1)$). They characterized a similar setting in 2025 but using a seven-qubit Steane error-correcting code [2059]. They separately implemented a fault-tolerant T gate using magic state preparation with flag qubits, fully using their 16 qubits [2067]. In 2023, they published a blueprint to implement an FTQC architecture [2069] which was completed with a proposal to use color codes in 2025 [2070]. The company is also studying the implementation of qudits to scale the computing mathematical space. They experimented the entanglement of two qudits, encoded in five states of calcium ions [2071]. In July 2026, they presented experiments using holographic quantum error correction codes, which can correct burst errors where multiple consecutive qubits are affected by errors [2072]. They also experimented the same month with transversal logical H and CCZ (Toffoli) gates across multiple codes (color codes, surface codes), accessed via lattice surgery between two different codes, combining a Hadamard gate on a four-qubit surface code and a doubly controlled Pauli-Z [2073]. In September 2026, they did test the teleportation of a logical state encoded in a small $[\![5, 1, 3]\!]$ code (1 logical qubit, distance 3) in a 16-qubit system [2074].

Software tools. Their PINE system supports Qiskit, Cirq, PennyLane and Pytket (Figure 227). They team up with NTT on developing financial applications [2075]. Since December 2024, IonQ is also partnering with Classiq, to adapt the Israeli startup compiler and circuit optimizer to their trapped ions.

Case studies. Their use cases seem positioned in the chemical simulation field, one being done with QC Ware on the simulation of the reduction of NO to N_2O, catalyzed by a nitric oxide reductase (NOR) [2076] and another one on small molecules simulations using a VQE algorithm variant [2077]. They also prototyped a QAOA-based warehouse optimization algorithm, with resource estimations for scaling [2078].

Customers. They sold a 20-qubit QPU to the Leibniz Supercomputing Centre (LRZ) in 2023 for €9.8M [2079].

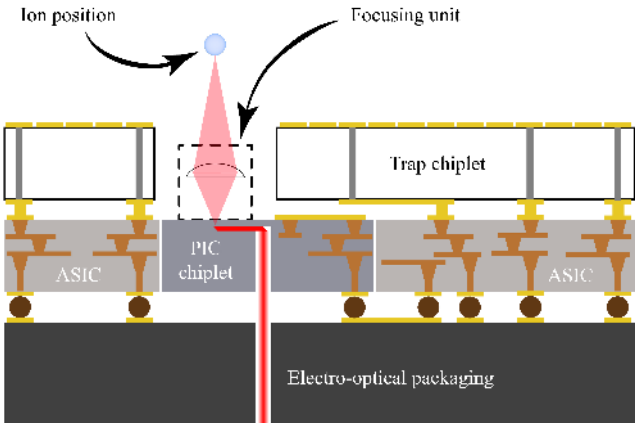


Figure 226: AQT and partners heterostructure proposal for an ion trap to convey both electric signals and laser light for controlling ion gates. Source: [1857]. Added in 2026.

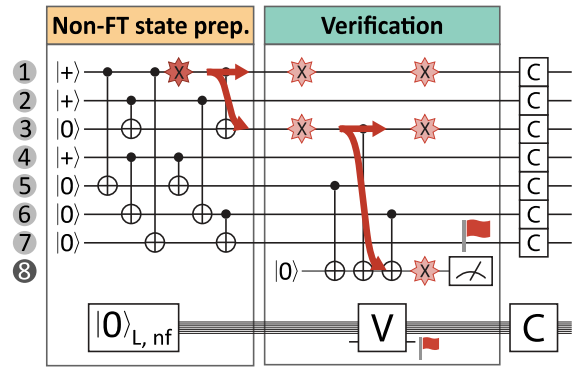


Figure 227: How AQT implemented a fault-tolerant T gate with magic state preparation. Source: [2067].

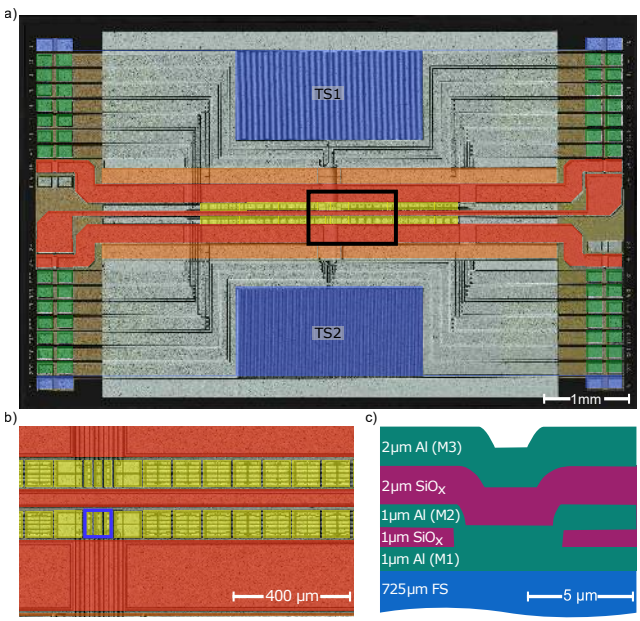


Figure 228: AQT Quantum Spring Array QCCD trap manufactured by Infineon. Source: [2065]. Added in 2025.

Figure 229: AQT 2-rack system. It consumes about 2 kW.

It became operational in September 2024. Another system, the IBEX Q1, was deployed in 2024 at the University of Innsbruck in a hybrid HPC-QPU environment, with the HPC cluster LEO 5 [2080]. Another one, the PIAST-Q, was sold in July 2024 to the Poznan Supercomputing and Networking Center (PSNC) in Poland, as part of the EuroHPC JU and was inaugurated in June 2025. Their 20-qubit QPU is named MARMOT.

Open Quantum Design

Canada, 2024

Open Quantum Design is a non-profit spin-off of the Perimeter Institute in Waterloo that is developing an open-source barium-based trapped ion quantum computer, including some UHV pump [2081]. It comes out of the work from Crystal Senko, Rajibul Islam, and Roger Melko. The platform was formally introduced in January 2025. Their current system as of 2026 supports 26 qubits.

Universal Quantum

UK, 2018, $14.6M

Universal Quantum is a spin-off from the Ion Quantum Technology Group at the University of Sussex in the UK led by Winfried Hensinger [2082, 2083].

Company. Their CEO is Sebastian Weidt. The company had a staff of about 100 as of mid-2026. In September 2026, they established an R&D center in Singapore, with EDBI (SG Growth Capital) investing in the com-

pany. It will focus on ion trap chip development, packaging and integration.

Technology. The company is developing a scalable trapped ion system based on a modular architecture allowing direct transfer of qubits between modules. Gate operations are performed with microwaves transmitted by electrical circuits and magnetic fields instead of lasers. They use 2D QCCD based Paul traps which are well known, with ytterbium ions clock qubit ($^{171}Yb^+$) along with barium ions (Ba^+) for sympathetic cooling (Figure 230). Qubit gates are enabled by local magnetic field gradients which allow individual ion addressing by shifting resonance frequencies, giving selective control even with global microwave fields. Local microwave emitters embedded in the ion trap generate localized fields to perform high-fidelity gates. The ion trap chips require multiple metal layers and use a silicon interposer as well as backside layers. One side effect related to the conveyed current in the traps is their heating. The cooling is around 70K, which is achieved using gaseous helium. They still need to use lasers at least for the Doppler cooling of ions during their preparation, then for the qubit state readout combining the usual laser excitation and fluorescence readout with a silicon photomultiplier [2084]. They published a paper in 2024 on quantum error correction, explaining a novel decoding method for transversal CNOT operations that can be natively realized on their hardware due to their long-range qubit connectivity. The method is necessary to reduce propagation of artificial correlated errors between logical qubit patches, which can occur using simple decoding methods such as MWPM (Minimum Weight Perfect Matching) [2085].

Multi-module. In 2022, they announced their plan to reach one million qubits, some day, using a modular approach with side-by-side arrangement of 2D ion traps [2088] (Figure 231). They have demonstrated transferring ions between modules using electric fields. They call this technology UQConnect [2089] and it has been demonstrated to show connections between chip modules at 2,400 transfers per second, each transfer between chip modules, with a fidelity of 99.999993%. The complexity of the system does not scale with the number of controlled qubits. Multiple links are enabled by their CMOS silicon based wafer and advanced packaging methods.

Their hardware is also designed for scaled heat removal, unlike with some other trapped ions systems. Their chips are thermally conductive, which enables them to remove heat efficiently. Still, the generated heat seems to be a significant problem yet to fix. In July 2024, the company announced the creation of an ASIC which operates at 70K which abstracts control complexity away from the ion trap device.

Customer. They won a $67M deal with DLR in Germany in November 2022. It led them to establish an R&D and sales branch there.

Aquabits

Canada, 2021

Aquabits is developing a trapped ions qubit processor using 'aquaporins', that trap ions inside artificial water channels.

It avoids using lasers and micro-nano fabrication techniques, making these qubits highly scalable. There's no public way to find out how all these qubits are controlled, entangled and measured.

eleQtron

Germany, 2020, €73.5M

eleQtron spun out from the University of Siegen and develops a NISQ trapped ions quantum computer.

eleQtron got a $21M funding from the North Rhine-Westphalia (NRW) region to build a hybrid and modular supercomputer associating a QPU and classical processing units as part of the EPIQ project and along with FZ Jülich, in the JION Quantum Computer center. The first 30 qubits QPU was supposed to be delivered by the end of 2024 [2090]. It seems like it was delivered in September 2026, with an undisclosed number of supported qubits, the goal being to reach 200 physical qubits.

Technology. They use the Magnetic Gradient Induced Coupling (MAGIC) technology to control ytterbium ions in 1D, which was introduced in 2012 by the University of Siegen [2091]. Creating magnetic field gradients to make individual ions addressable in frequency space and to induce coupling between them. Creating strong and stable magnetic gradients at the very ions location is challenging. You need both strong magnetic fields to enable fast two-qubit gates but the frequency separation between ions due to the gradient needs to be large enough to allow for selective microwave addressing. It can also contribute to the anomalous ions heating phenomenon. Their ion traps are manufactured by FMD in Germany.

Qubits. Their current CNOT two-qubit gate fidelity is 98%, which is not stellar for trapped ions. They initially planned to release a 10-qubit processor in 2023. In May 2024, they announced the availability of a first demonstrator, QSea-I, as part of this project, that was built with the help of NXP and ParityQC [2092].

Software. They are partnering with ParityQC (Austria) for software development within the ATIQ consortium with a total funding of €44.5M including €37M from the German government through DLR, of which eleQtron got €9.1M. eleQtron researchers along with other researchers proposed a way to solve 3-SAT combinatorial problems using a PUBO formulation which is directly implemented, the cost Hamiltonian encoding the problem being defined by the three-body interaction strength. The idea is to use a digital quantum annealing, or Trotterized quantum annealing, via a Trotterization of the time evolution of the Hamiltonian on a gate-based QPU.

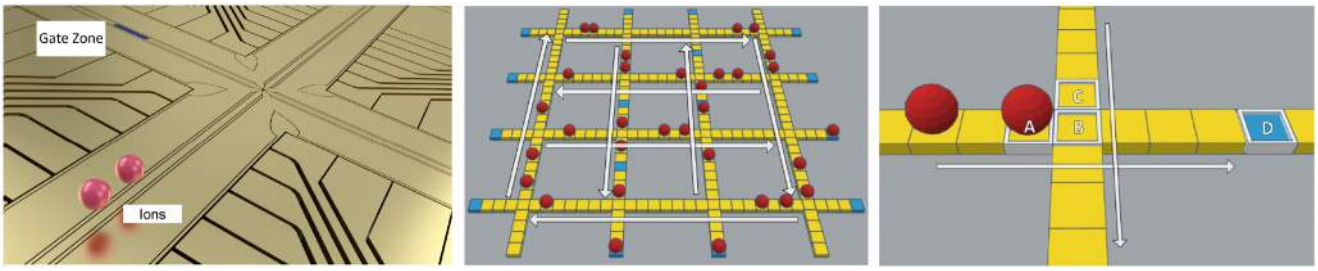


Figure 230: Universal Quantum's shuttling ion architecture in their Paul traps. Source: [2086, 2087].

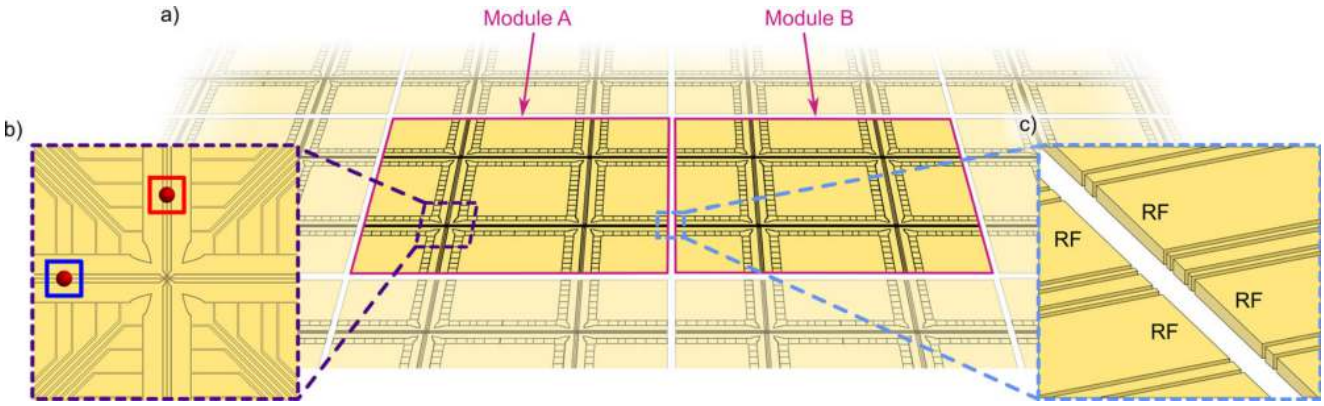


Figure 231: Universal Quantum plans to interconnect side-by-side several ion traps with ions moving from module to module in a seamless fashion as if there were moving on a larger ion trap. The individual modules have a size of 20 mm size in their first generation. Source: [106].

This could bring some exponential advantage but it would require the implementation of native three-body spin interactions, which could be done with trapped ions [2093].

Qudora Technologies

Germany, 2022

Qudora Technologies is a spin-off from PTB and the University of Leibniz Hannover launched by Amado Bautista (CEO), Henning Hahn (also CEO), Christian Ospelkaus, Piet O. Schmidt and Andreas Waag who have a strong experience in semiconductor circuits design.

They develop a trapped-ion QPU with the goal to assemble 50 qubits, particularly as part of a €42M contract with DLR. They use a mix of lasers, oscillating magnetic fields and microwave-based controls embedded inside the ion trap, including for qubit readouts (*aka* Near-Field Quantum Control or NFQC).

In 2026, they developed a machine learning based optimization of ions shuttling [2094]. They also launched in December 2025 their Qamelion Emulator, which supports adaptive noise modeling which is good for testing NISQ circuits.

One of their first customers is the AI and quantum cloud vendor QAI in South Korea, with a system to be installed in 2027.

Foxconn

Taiwan, 2021

Hon Hai (Foxconn) announced in December 2021 that it started the development of a trapped ions quantum computer in its quantum computing research center, part of its Research Institute [2095]. The quantum lab is directed by Min-Hsiu Hsieh who was previously an associate professor at the Centre for Quantum Software and Information from the University of Technology Sydney, and is a board member for Quobly. The trapped-ion research team is led by Guin-Dar Lin. Their new trapped-ions lab opens at the end of 2023 in the Baokao Science and Intellectual Park Xindian in New Taipei City.

The lab focuses on hardware development with trapped ion qubits, enabling technologies development and algorithms and software tools development for Foxconn's internal usage. In April 2023, the company announced it would deliver a 5-10 ions QPU within 5 years. In October 2025, it published a paper describing an ion-trap manufacturing technique to reduce the effect of ion Heating in a 1D RF Paul trap [2096].

Crystal Quantum Computing

France, 2021

Crystal Quantum Computing was created by Quentin Bodart (with a long-lasting experience with neutral

atoms, including quantum micro gravimeters) and Luca Guidoni (from the CNRS MPQ laboratory in Paris).

Its goal is to create a trapped ion quantum computer using strontium 88 ($^{88}Sr^{+}$) ions that are excited at Rydberg levels [2097], based on earlier and existing work from Markus Hennrich from Stockholm University [2098], Ferdinand Schmidt-Kaler from Johannes Gutenberg Universität Mainz and also at NeQxt [2099], and Markus Müller from RTWH Aachen. Their ions would be easier to control than classical trapped ions, using UV lasers at 243 nm (generated with infrared lasers and double frequency doubling) and RF directive antennas, all being handled in a Paul trap on a chip running at 30K. Two-qubit gates are to be implemented with CPHASE gates or Rydberg blockade [64].

In September 2024, Advans Lab, the innovation branch from Advans Group, an engineering services group, invested an undisclosed amount in the startup.

neQxt

Germany, 2023

neQxt is a startup cofounded by Sebastian Deuser (CEO), Christian Zimmermann (COO), Björn Lekitsch (CTO), Janine Hilder (CSO), and Ferdinand Schmidt-Kaler (scientific advisor, who worked before on Rydberg ions, and early on, worked with Serge Haroche and Michel Brune at Ecole Normale Supérieure in Paris [2100]). It spun out of Universität Mainz. They were 47 people as of September 2025.

They use some shuttling ions-based architecture and laser driven qubit gates, which are both commonplace [2101, 2102]. They also made some proposals related to the code switching technique in the realm of quantum error correction [2103].

In July 2025, they presented in a preprint paper their Quantum Internet in a Nutshell (QI-Nutshell), a tool to simulate QKD and quantum Internet protocols on trapped-ions QPUs with the aim of testing QKD error correction codes [2104]. This is a very original use case for a QPU.

They were selected in September 2024 by the Agency for Innovation in Cyber Security in Germany to build a portable quantum computer for the army. Portable meaning, operating from a movable rack!

Quantum Art

Israel, 2022, $140M

Quantum Art is a trapped-ions startup based in Tel Aviv that was created by Tal David, the former coordinator of the defense minister and then for the whole government quantum strategy for 10 years, with Roee Ozeri from the Weizmann Institute (who was a research fellow in David Wineland's team at NIST) and Amit Ben Kish from Raphael. They were 40 as of mid-2025. They started with a 5 trapped-ions experimental system built by Roee Ozeri in 2023-2024 [1892, 2105].

Technology. Their ion trap technology has the following specifics, seemingly based on $^{88}Sr^{+}$ [2106]:

- Optical segmentation of long 1D ion chains into independently operating cores using laser-defined boundaries, as shown in Figure 232.
- Optical tweezers based and Mølmer-Sørensen multi-qubit gates executing up to 1,000 two-qubit operations in a single cycle [2107].
- Dynamic reconfiguration of multi-core arrays for rapid entanglement generation and distribution.
- Modular, high-density 2D structures allowing physical qubits to scale efficiently within compact footprints.
- Multi-qubit gates support using multi-tone and multi-mode laser modulation, which implements many pairwise interactions in a single operation. It is based on using a mix of global and semi-global drives combined with single-qubit flips, which can reproduce a full set of multi-qubit gates [2108, 2109].

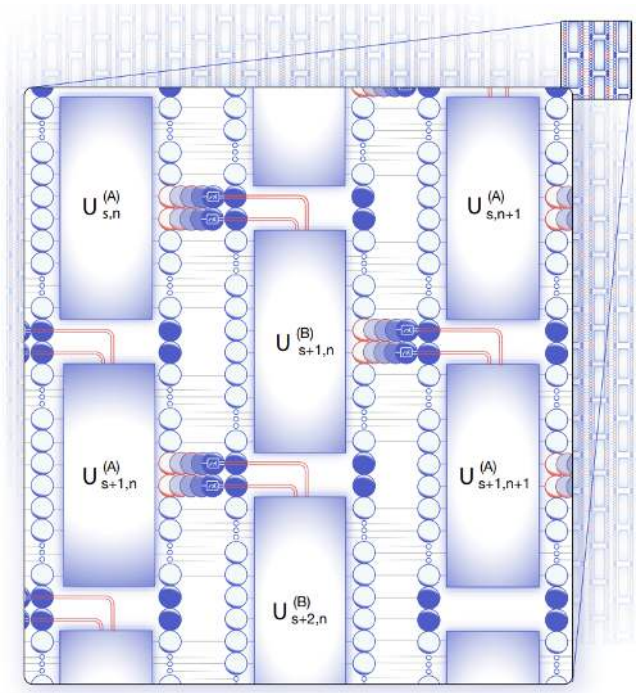


Figure 232: Quantum Art ion trap structure with 1D arrays of ions (vertical). Source: [2105].

They claim that their systems will be 100 times faster than trapped ions competitors. They are also investigating the use of their platform to run analog simulations of Ising Hamiltonians [2110] and how to interconnect trapped ions and cold atoms qubits with photonic interconnect using the same atom species (^{88}Sr atoms and $^{88}Sr^{+}$ ions) [1839].

Roadmap. In June 2025 with an update in 2026, they published their FTQC roadmap which targets 50 physical qubits in 2025 with their Montage QPU, 1,000 physical qubits and 100 logical qubits by 2027 with the Perspective series, an ultra-dense 2D architecture in 2029 scaling to 12K physical qubits with the Landscape series, and thousands of logical qubits by 2031, and 1M physical qubits by 2033 or later with the Mosaic series, fitting in a 50×50 mm^2 trap footprint.

In August 2025, Quantum Art demonstrated the control of a 1D-chain of 200 ions. It didn't mean it was a fully functional QPU with quantum gates and readout.

HYQ CO

China, 2022, $27M

HYQ Co *aka* Huayi Boao (Beijing) Quantum Technology Co. and Hyqubit was created by Yao Lin (CEO), who worked before at the Brookhaven National Laboratory, USA, and Duan Luming (CSO), the Executive Director of the Quantum Information Center of Tsinghua University. The company raised $27M in two rounds in 2024.

The company operates as a trapped ion QPU in the cloud, starting with the HYQ-A37 which seemingly hosts 37 ^{171}Yb+ ions. In October 2024, they published a paper proposing to encode two qubits per barium ion using different orbital angular momentum ($S_{1/2}$ and $D_{5/2}$), using hyperfine splitting with the total angular momentum quantum number F for each qubit manifold, and a process to entangle these two qubits using a Raman transition at 532 nm, but with a moderate fidelity of 96.3%[2111]. They also work on two-species systems using ^{171}Yb+ ions for cooling and ^{137}Ba+ ions for memory [2112].

They developed specific components for their QPU including a narrow linewidth laser frequency stabilization system, optical light path modules, electronic control systems and ion trap circuits. They also developed an experimental ion-based analog quantum simulator supporting up to 300 ions [2113] and contributed to a photonic over fiber QPU interconnect experiment published in 2025, but this time, using calcium ions [2114].

The company also published a preprint on oil production optimization [2115].

In China, there also seems to be another company **Guokai Ke Quantum Technology** that developed a 20-qubit trapped ions QPU. It is part of the offering from the Wuyue QuantumAI cloud platform that is mentioned in [2116].

Zuriq

Switzerland, 2024, $30M

Zuriq is a trapped ions company spun-out of Jonathan Home's team at ETH Zurich.

Technology. Zuriq uses micro-Penning ion traps with beryllium ions [26, 1852]. These use static electric fields together with a strong static magnetic field for confinement, unlike Paul traps which require an RF trapping drive and therefore introduce RF micromotion and RF-electrode power dissipation. The total thermal advantage remains architecture-dependent. Micro-Penning traps can support dense 2D arrays and parallel operations (Figure 233). Single-qubit gates use 313 nm optical control, while two-qubit interactions may use optical or microwave fields. Their demonstrated cryogenic setup operates around 6.5 K [26].

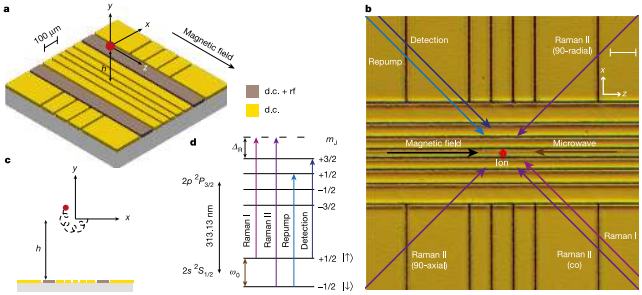


Figure 233: Zuriq ion trap layout using a mix of laser, microwave, magnetic and static current controls. Source and detailed caption: [26].

Qubitcore

Japan, 2024, $10M

Qubitcore was created by Ryuta Watanuki (CEO), Hiroki Takahashi (CSO), Ezra Kassa, Shaobo Gao, and Koichiro Miyanishi as principal researchers. It spun out of OIST's Experimental Quantum Information Physics Unit led by Hiroki Takahashi. The company develops a distributed ion trap architecture combining ion trap processors using photonic quantum interconnects. They plan to reach 1000 qubits by 2029 with commercial deployment by 2030. Their micro-optical cavity was built at OIST.

Unitary Quantum Co

China, 2022, ≈$30M

Unitary Quantum *aka* Hefei Unitary Quantum Co develops full systems and components for trapped ion based quantum computing, seemingly for universities and academic labs. They also contribute to academic research in trapped ions photonic interconnect [2122]. The company spun out of the CAS Key Laboratory of Quantum Information led by academician Guo Guangcan at USTC. It was cofounded by Han Yongjian, Huang Yunfeng, Xu Xiaoye, Li Chuanfeng, Cui Jinming, and He Ran.

They build trapped-ion quantum computers and experimental systems using ytterbium ions, including QCCD ion-traps, photonic and optoelectronic components, multi-photon entanglement sources, femtosecond fiber lasers, pulse compressors, ultra-stable cavities, and

Industry vendor	Local vs global addressing	Two qubit gate mediation (gradient vs motional mode)	Pulse vs continuous	Spatial addressing method
IonQ / Oxford Ionics (EQC)	Global microwave field shared across chip, per-ion control is local and electronic [121, 1848]	Motional-mode-mediated MS gate driven by an oscillating near-field gradient (> 100 T/m per A) from on-chip AC currents [121, 1841]	Pulsed [60]	DC/AC voltages displace the ion in the near-field gradient plus frequency separation [121, 1848]
Universal Quantum	Global microwave + RF fields, local voltage-controlled selection [25, 2124]	Static gradient (permanent magnets / current wires) couples spin to a shared mode, MS-type gate, gradient-mediated [2124, 2125]	Continuous, dressed state with engineered clock qubits [2124]	Voltages shuttle ions along the static gradient into/out of resonance with the global fields, modular links between modules [25, 106]
eleQtron (MAGIC)	Global microwave, individual addressing in frequency space [2091, 2126]	Static gradient (MAGIC) gives effective spin-spin coupling via a common mode, gradient-mediated [1894, 2091]	Pulsed with AWG or DDS shaping [1894]	Frequency-space addressing from the static gradient (distinct transition per ion), single register up to ∼30 ions [2126]
Qudora (NFQC)	Near-field microwave from on-chip components, local per-zone control [1847]	Motional-mode-mediated gate via an oscillating near-field gradient [59, 1847]	Pulsed [1847]	Multi-zone registers, ions shuttled between zones by voltages, near-field control localized on-chip [1847, 1898]

Table 7: Microwave-driven single- and two-qubit gate approaches across commercial trapped-ion vendors using microwave drives, complementing Table 9. MS = Mølmer-Sørensen two-qubit gate. RF = radio frequency, AC = alternating current, DC = direct current, AWG = arbitrary waveform generator, which creates a shaped baseband waveform that can be mixed with a carrier, DDS = direct digital synthesizer, which digitally generates a phase- and frequency-controlled tone. 🅭 Olivier Ezratty, September 2026.

fiber microcavities. It currently supports 12-qubit systems with a Quantum Volume of 32 (5 qubits). Their ion trap is cooled at 4 K. See their past academic work in [1931, 2123].

Key trapped ions quantum computing reviews

Here is a selection of trapped ions scientific reviews to dig into the concepts presented in this section:

Quantum dynamics of single trapped ions by Leibfried *et al.*, 2003 (44 pages): the founding physics review, trap potentials and motional modes, laser cooling, ion-light coupling, nonclassical motional states and the early gate schemes [2117].

Quantum computing with trapped ions by Häffner *et al.*, 2008 (49 pages): the classic synthesis of the first decade, Cirac-Zoller and Mølmer-Sørensen gates, entanglement of small registers, decoherence sources and tomography [2118].

Trapped-Ion Quantum Computing: Progress and Challenges by Bruzewicz *et al.*, June 2019 (about 50 pages): with qubit species trade-offs, gate mechanisms, error sources and the routes to scaling [1827].

Shuttling-based trapped-ion quantum information processing by Kaushal *et al.*, February 2020 (25 pages): with ion transport, separation and merging in segmented traps, waveform generation, and the fidelity cost of moving qubits [2119].

Engineering of microfabricated ion traps and integration of advanced on-chip features by Romaszko *et al.*, April 2020 (15 pages): trap fabrication processes, materials, junctions, and on-chip integration of optics, photodetectors and electronics [2120].

Materials challenges for trapped-ion quantum computers by Brown *et al.*, October 2021 (14 pages): anomalous heating and electric-field noise from electrode surfaces, the dominant coherence limit, and the materials work needed to suppress it [2121].

Ion-Based Quantum Computing Hardware: Performance and End-User Perspective by Strohm *et al.*, May 2024 (44 pages): vendor metrics, qubit counts, gate times and fidelities, wall-clock end-to-end runtimes and which algorithms would be supported [1825].

	Helios	Forte				
elements	$^{137}Ba^+$ (data) $^{171}Yb^+$ (cooling) [119]	$^{171}Yb^+$ [144] $^{133}Ba^+$ in Tempo	$^{40}Ca^+$ [2063, 2127]	$^{9}Be^+$ [26]	$^{88}Sr^+$ [2106]	$^{88}Sr^+$ [2097]
ion trap type	QCCD [58, 119]	1D Paul trap [144]	1D Paul trap [2127]	micro-Penning traps QCCD [26, 1852]	RF trap with dynamic optical potentials [2105]	Paul trap [64]
trap manufacturer	Infineon	IMEC, Global Foundries	home made, Infineon [2064, 2065]	Infineon [2128]	in-house	
cryogenics	15 K, LHe [119]	10 K	RT	6.5 K [26]	RT	30 K
single-qubit gate operations	515 nm lasers Raman transition [119]	≈355 nm laser Raman transition [144]	729 nm laser [2060, 2127]	two 313 nm confocal lasers [26]	laser [2107]	243 nm UV laser and RF [2098]
two-qubit gate operations	515 nm laser Mølmer–Sørensen + ions shuttling [119]	Mølmer–Sørensen (bichromatic laser) [144]	Mølmer–Sørensen (bichromatic 729 nm laser) [2060, 2061]	laser or microwave [26]	Mølmer–Sørensen (bichromatic laser) [2107, 2108]	UV laser [64, 2098]
two-qubit gate time	50-100 μs 50 ms gate cycle [119]	950 μs [144]	10-100 μs [2061, 2127]	10 μs [26]	≈100 μs (estim.)	
two-qubit connectivity	many-to-many [61, 119]	many-to-many [1834]	many-to-many [2062]	3D ion shuttling [26]	full connectivity [1892, 2109]	nearest neighbor
record qubits #	98 [119]	64 [1976]	30	1 as of 2024 [26]	32	

Table 8: Comparison of trapped-ion vendors' key characteristics, part 1, with laser-driven ions. RT = room-temperature operation. LHe = uses a helium liquefier. Cells carry a reference when an arXiv or peer-reviewed source documents the value. Olivier Ezratty, September 2025, updated in September 2026, including additional references. Some data may be incorrect due to changes in vendors' technology approaches.

elements	$^{171}Yb^+$ [1846, 2101]	$^{171}Yb^+$ and $^{137}Ba^+$ [2111, 2112]	$^{137}Ba^+$ [121, 1988]	$^{43}Ca^+$ and $^{171}Yb^+$ [2124]	$^{171}Yb^+$ [1894, 2126]	$^{171}Yb^+$ [1898]
ion trap type	surface traps [2101, 2102]	surface traps [2113]	CMOS [68]	QCCD Paul trap [25, 106]	QCCD [2091]	microfabricated surface traps [1847, 2129]
trap manufacturer	in-house at Mainz University [2101]	in-house	Infineon, then Skywater	Global Foundries	FMD (Germany)	NXP
cryogenics	RT	RT	20 K [1841]	70 K [25]	RT≤30 qubits, 4-10 K>30 qubits	4 K
single-qubit gate operations	laser [2101]	Laser Raman transition [2111]	MW global RF local [121, 1848]	local and global MW [2124]	microwaves and RF [1894, 2126]	near-field microwave [59, 1847]
two-qubit gate operations	laser [2102]	laser [2123]	MW global + oscillating magnetic gradient [60, 121]	local and global MW + static magnetic field gradient [2124, 2125]	microwave via magnetic gradient [1894, 2091]	near field microwave and magnetic field gradient [59, 1847]
two-qubit gate time	≈100 μs (estim.)	≈100 μs (estim.)	≈220 μs [121]	313 μs [2124]	≈100 μs (estim.) [1894]	50 μs [1847]
two-qubit connectivity	full connectivity [2101]	full connectivity [2113]	many-to-many [68]	many-to-many [106, 2086]	all-to-all via global microwave [2126]	modular transport zones [1898, 2094]
record qubits #	20	37	10		10	50 (target)

Table 9: Comparison of trapped-ion vendors' key characteristics, part 2, with laser-driven ions (grey) and microwave-driven ions (blue). RT = room-temperature operation. Microwave-driven operations are further detailed in Table 7. Cells carry a reference when an arXiv or peer-reviewed source documents the value. Olivier Ezratty, September 2025, updated in September 2026, including additional references. Some data may be incorrect due to changes in vendors' technology approaches.

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This **Trapped ions qubits** subsection contains 338 bibliographical references and notes containing at least 4,862 pages.

1.8 Neutral-atom qubits

Neutral-atom quantum computers generally use laser-cooled neutral atoms and are therefore often called cold-atom systems, although "cold atoms" is a broader term and neutral atoms are not intrinsically cold [2130]. Unlike trapped ions, neutral atoms are usually confined by optical dipole traps and optical tweezers rather than radio-frequency electrodes. Atom preparation proceeds in several stages. An atomic beam or vapor is first decelerated and collected, then a MOT (magneto-optical trap) combines three orthogonal pairs of red-detuned, circularly polarized laser beams with a weak quadrupole magnetic field. The first MOT was demonstrated in 1987 by Raab, Prentiss, Cable, Chu and Pritchard [2131]. The velocity-dependent Doppler shift provides damping while the position-dependent Zeeman shift provides a restoring force. Sub-Doppler temperatures are obtained with polarization-gradient cooling, including Sisyphus cooling [2132]. A different mechanism, the Zeeman slower, uses a spatially varying magnetic field to compensate the changing Doppler shift while an atomic beam is decelerated [2133]. Optical tweezers, often generated with SLMs and AODs, then position individual atoms in programmable arrays [2134–2137]. This technology belongs to atomic, molecular and optical physics and ultracold-atom trapping, rather than to the usual field of optomechanics of levitated mesoscopic particles.

The two basis states of a neutral-atom qubit are selected internal atomic states whose nature depends on the species and encoding. Alkali platforms commonly use two hyperfine ground states. Alkaline-earth-like atoms can use nuclear-spin, metastable or optical-clock states. Rydberg states are usually temporary auxiliary states used to mediate strong interactions for entangling gates, while ground-Rydberg encodings are also used directly in analog Rydberg simulators and in some qubit schemes [2138].

Neutral-atom processors can implement analog quantum simulation and gate-based quantum computing [2139]. In analog mode, the atoms evolve under a programmable many-body Hamiltonian. Depending on the protocol, this can prepare low-energy states, implement adiabatic or quasi-adiabatic evolution, or study coherent real-time dynamics, quenches and nonequilibrium phenomena. Gate-based processors instead execute sequences of one- and multi-qubit operations. Most leading vendors now also target QEC and FTQC, while analog quantum simulation remains an active product and research modality.

Neutral-atom analog simulators address programmable spin Hamiltonians, including Ising, XY and Heisenberg-type models, as well as bosonic and fermionic lattice models depending on the atomic species and trapping architecture. Rydberg arrays are also used for combinatorial optimization mappings such as unit-disk-graph MIS and related problems, and have been explored for quantum machine learning demonstrations [2140].

Relevant physics problems include Hubbard-family models. The Fermi-Hubbard model describes interacting fermions on a lattice, while the Bose-Hubbard model describes interacting bosons, so "Hubbard model" is not synonymous with "Fermi-Hubbard model" [2141]. Programmable spin models can investigate antiferromagnetism [2142], ferromagnetism, frustrated magnetism, spin liquids, excitations and phase transitions. Ultracold-atom platforms are also used to study Bose-Einstein condensates, strongly interacting Fermi gases, superfluidity [2143], quantum transport, nonequilibrium dynamics [2144], topological phases, superfluid-to-Mott-insulator transitions and high-harmonic generation [2145]. The experimental geometry, species, internal-state preparation and interaction protocol depend on the Hamiltonian being simulated.

Most of these physics simulation applications relate to fundamental research in physics and are relatively remote from practical industry needs. Quantum chemistry problems are outside the capabilities of usual cold-atoms analog quantum simulators. They can be solved in two different settings: gate-based cold-atoms QPUs, or fermionic cold-atom systems that we cover later in this part.

One limitation of annealing-like analog protocols is that coherent and incoherent errors accumulate during the evolution, while the useful schedule duration is bounded by relevant coherence and lifetime scales. In 2026, [2146] introduced an accuracy-oriented benchmark and classical variational Monte Carlo and Green-function Monte Carlo methods for Rydberg-array QUBO instances. Their variational method reached up to 10^8 atoms on a single CPU at moderate target accuracy, while the more accurate Green-function method reached much smaller, but still very large, instances. This is a strong classical baseline for the benchmarked Rydberg-QUBO problem classes, but it does not establish that every neutral-atom analog simulator is far from quantum advantage, particularly for native many-body dynamics without a costly problem embedding.

Neutral atoms are very versatile and have various other use cases beyond quantum computing and simulations, including quantum sensing, with applications in micro-gravity detection, electromagnetic spectrum analysis and atomic clocks and quantum memories and repeaters [2147, 2148]. We cover these various use cases in other parts of this book.

1.8.1 History

Neutral atom-based computing grew out of decades of atomic physics before quantum computing was conceptualized. High-lying atomic spectra were organized by Johannes Rydberg in the late nineteenth century and later understood through quantum mechanics. Research on laser cooling, ultracold gases and Bose-Einstein condensates was directly relevant because it developed much of the trapping, cooling, imaging and coherent-control

toolbox later reused in neutral-atom quantum processors [2149].

Laser cooling developed through several distinct milestones. Optical molasses was demonstrated by Steven Chu and colleagues in 1985. Zeeman-slower deceleration had already been demonstrated by William Phillips and Harold Metcalf in 1982 [2133]. The first MOT followed in 1987 [2131]. In 1988–1989, polarization-gradient mechanisms including Sisyphus cooling explained and enabled temperatures below the Doppler limit [2132]. Claude Cohen-Tannoudji, Steven Chu and William Phillips shared the 1997 Nobel Prize in Physics for methods to cool and trap atoms with laser light. Laser cooling, followed by magnetic trapping and evaporative cooling, enabled the first dilute-gas Bose-Einstein condensate in ^{87}Rb at JILA in 1995, with condensation appearing near 170 nK [2150]. Bose and Einstein had predicted Bose-Einstein condensation in the 1920s.

Cold-atom techniques also enabled major advances in atomic clocks, first through atomic fountains and later through optical lattice clocks. These developments should be distinguished from room-temperature vapor-cell clocks and from the SI realization of the cesium hyperfine transition.

In the 1980s, Serge Haroche started to work with Rydberg atoms and their integration in superconducting cavities, pioneering cavity quantum electrodynamics (CQED), light-matter interactions, coherent atom control and the experimental study of quantum decoherence.

So, how about neutral atoms and quantum computing? Richard Feynman proposed quantum simulation in 1981. In 1996, Seth Lloyd showed that universal quantum simulators can efficiently reproduce the dynamics of local quantum systems [2151].

Quantum simulation is investigated with several hardware modalities, including neutral atoms, trapped ions, superconducting circuits and photonic systems. Neutral atoms combine large programmable arrays, tunable geometry, strong Rydberg interactions, and a commercial analog quantum simulation offering, coming mainly from QuEra and Pasqal.

Then things started to get serious with two-qubit gates proposals from Dieter Jaksch, J. Ignacio Cirac and Peter Zoller [2152] and from Gavin K. Brennen et al. in 1998 [2153], with improvements from Jaksch, Zoller and Mikhail Lukin in 2000 [2154]. In 2012, J. Ignacio Cirac and Peter Zoller proposed a set of criteria for quantum simulators like those from David DiVincenzo's 2000 for gate-based quantum computing (in Figure 235) [2155].

The first Rydberg-blockade two-atom gate and entanglement demonstrations were published in January 2010. The University of Wisconsin team demonstrated a CNOT gate between individually addressed neutral atoms [2156], while the Institut d'Optique team generated entanglement between two ^{87}Rb atoms using Rydberg blockade [2157]. Both papers were received in 2009.

Many advances during the 2010s encouraged some scientists to create their own companies. It started with the creation of ColdQuanta, now Infleqtion (2007), Muquans (2011), both using cold atoms for quantum sensing in absolute gravimetry, BraneCell (2015), Atom Computing (2018), Pasqal (2019) and QuEra (2020). Besides Muquans (now in France's Exail), all the others are positioned in the quantum computing market although Exail is also a technology provider for Pasqal for some of their lasers.

1.8.2 Science

Neutral atoms are non-ionized atoms with equal numbers of protons and electrons. Neutral-atom quantum processors use several atomic families. Alkali atoms such as rubidium and cesium have one valence electron and convenient optical cycling transitions and microwave hyperfine splittings. Alkaline-earth and alkaline-earth-like atoms such as strontium and ytterbium have two valence electrons and offer additional clock, metastable and nuclear-spin structure.

Ytterbium and strontium can support several distinct qubit encodings. Fermionic isotopes such as ^{87}Sr, with nuclear spin $I = 9/2$, and ^{171}Yb, with $I = 1/2$, can encode qubits in nuclear-spin sublevels [2158–2160]. On their side, bosonic ^{88}Sr has $I = 0$ and cannot host a nuclear-spin qubit. Their qubit can instead use optical-clock or fine-structure states. In properly designed alkaline-earth-like encoding, leakage or decay events can be converted into detectable erasures, as demonstrated for metastable ^{171}Yb [2161]. Atom loss is another important erasure channel and can be detected and replenished in some architectures.

The relevant coherence time depends strongly on the encoding. Hyperfine and nuclear-spin ground-state qubits can retain coherence from seconds to tens of seconds under suitable trapping and dynamical-decoupling conditions, while Rydberg states used during entangling operations typically have lifetimes of order tens to hundreds of microseconds, depending on principal quantum number, temperature and electromagnetic environment [2138, 2162]. Additional encodings under active investigation include optical-clock and fine-structure qubits in strontium and ytterbium [2163, 2164].

Rydberg states are highly excited atomic states with principal quantum number $n \gg 1$. Neutral-atom processors commonly use states with n of several tens to around one hundred, although this is an engineering choice rather than a definition. Their characteristic orbital size scales approximately as $n^2 a_0$, electric-dipole matrix elements between nearby Rydberg states scale strongly with n, and their radiative lifetime scales approximately as n^3 before blackbody-induced transitions are included [2138]. Their strong, controllable interac-

TABLE I. Criteria for quantum simulators and quantum computers

Criteria	Quantum computers	Quantum simulators
Quantum system	A scalable physical system with well characterized qubits	A system of quantum particles (bosons, fermions, pseudo-spins) confined in space and collectively possessing a large number of degrees of freedom
Initialization	The ability to initialize the state of the qubits to a simple fiducial state, such as $\|000\ldots\rangle$	The ability to prepare (approximately) a known quantum state (typically a pure state)
Coherence	Long relevant decoherence times, much longer than the gate operation time	
Interactions	A "universal" set of quantum gates	An adjustable set of interactions used to engineer Hamiltonians/quantum master equations including some that cannot be efficiently simulated classically
Measurement	A qubit-specific measurement capability	The ability to perform measurements on the system; either individual particles or collective properties
Verification		A way to verify the results of the simulation are correct

Figure 235: Comparisons of gate-based quantum computing (left) and quantum simulation (right). Source: [2130].

tions are used for entangling gates and programmable many-body Hamiltonians.

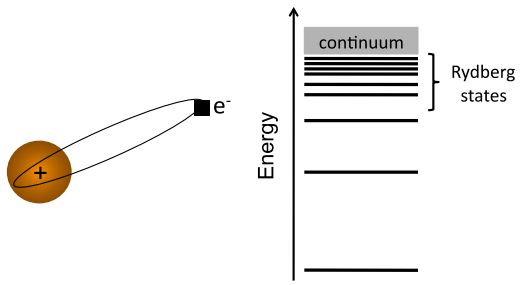

Figure 234: Rydberg states are high-lying electronic states with very large spatial extent and strong transition dipole matrix elements. Rydberg-Rydberg interactions can be resonant dipole-dipole or van der Waals interactions and enable entanglement and blockade. A stationary parity eigenstate does not generically carry a permanent electric dipole in zero electric field. Circular Rydberg states are a special high-angular-momentum family. Source: [2138, 2165].

The Rydberg-state lifetime is not the qubit coherence time when information is stored in hyperfine or nuclear-spin ground states. Those computational states can remain coherent orders of magnitude longer. Rydberg lifetime instead limits the duration and fidelity of operations that temporarily populate a Rydberg level.

Cold-atom processors exploit the Rydberg blockade effect. When the interaction-induced shift of the doubly excited state is large compared with the excitation linewidth and Rabi frequency, excitation of a neighboring atom to the same interacting Rydberg manifold is strongly suppressed [2138]. The blockade condition is therefore not set by a universal threshold such as $n > 50$ or 70. The blockade radius depends on the chosen Rydberg states, Rabi frequency, detuning, geometry and Förster structure, and is typically of order a few to several tens of micrometers. For $n \sim 100$, the electronic wavefunction has an order-micrometer spatial extent. Rydberg atoms can also be used as nonlinear optical media and for single-photon generation [2166, 2167].

Rydberg interactions also support nonlinear quantum optics and single-photon interfaces [2167]. These applications use related Rydberg physics but are distinct from the blockade-gate protocol used in quantum computing.

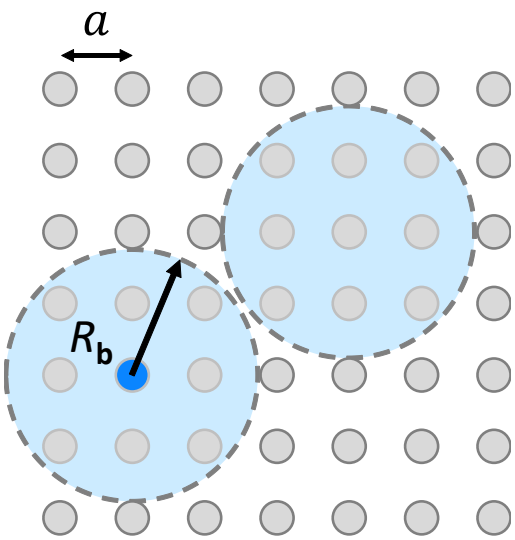

Figure 236: How Rydberg state connects neighbor cold atoms.

There are several neutral-atom qubit encodings (Figure 237). A convenient informal nomenclature distinguishes ground-Rydberg (gr), Rydberg-Rydberg (rr) and ground-ground (gg) encodings. Alkali ground-ground qubits commonly use two hyperfine ground states driven by microwaves or Raman fields, while Rydberg excitation is added for entangling operations. Alkaline-earth-like atoms add nuclear-spin, optical-clock and fine-structure encodings. Global microwave or optical fields can be combined with local light shifts or local addressing beams to select individual qubits.

Pasqal and QuEra have extensively used ground-Rydberg encodings for analog Rydberg simulation and hyperfine ground-state encodings with temporary Rydberg excitation for digital gates. Other vendors use different alkaline or alkaline-earth-like encodings. The exact mapping in Figure 237 should therefore be read as

representative and generation-dependent rather than as a fixed vendor taxonomy. Topological many-body states are also studied on neutral-atom arrays [2168, 2169].

Neutral-atom arrays can support gate-based and analog quantum-computing paradigms. Measurement-based quantum computing is also possible in principle once a suitable entangled resource state has been prepared [2170]. It does not eliminate the cost of entangling operations, since that cost is shifted to preparation of the cluster or other resource state before the measurement sequence.

With analog quantum simulation [2171–2176], a programmable Hamiltonian is engineered through atom geometry, local detunings, Rabi frequencies and Rydberg-mediated interactions. The system then follows a controlled time evolution. Some protocols aim at a low-energy or ground state, while others study quenches, transport, thermalization or other nonequilibrium dynamics. Analog programming therefore consists of continuous control waveforms rather than a sequence of discrete quantum gates, and local parameters can also vary during the evolution.

Fast and high-fidelity single-qubit gates can also be implemented on neutral atom platforms, thus enabling mixed digital-analog quantum programs.

Many hardware elements are shared between analog and gate-based neutral-atom processors, but not every encoding or architecture maps directly to both paradigms. Gate-based operation adds demanding requirements for calibrated universal gates, site-selective control, measurement and reset, and QEC. In reconfigurable architectures, compilation must also optimize atom transport, placement and parallelism [2177–2182].

Other cold-atom based models are proposed like Quantum Optical Neural Networks (QONN), a neural network architecture where each neuron is a cold atom, and their synapses are photonic-based feed-forward interactions between these atoms, the neural network weights being trained by backpropagation. The quantum advantage is however not clear both from a theoretical and practical standpoint [2183].

Gate-based processors are computationally universal when equipped with a universal gate set, whereas analog simulators implement restricted families of programmable Hamiltonians. This makes gate-based systems more general, but usually more demanding in control, calibration, measurement and QEC. Analog scalability is not limited by a universal qubit-count ceiling. Its useful scale depends on Hamiltonian programmability, coherent evolution time, preparation and readout fidelity, embedding overhead and the strength of classical baselines. Large-scale entanglement is therefore only one of several relevant criteria [1882].

Noise scaling in analog simulation remains an important question [2200]. Analog shots can contain shaped ramps, quenches and time-dependent controls, so their duration and error accumulation are protocol-dependent rather than intrinsically independent of system size [2201].

Startups such as Pasqal and QuEra initially emphasized analog programmable-Hamiltonian systems while also developing gate-based architectures. Atom Computing emphasized gate-based processing from the start. A major milestone came in December 2023 when the Harvard-MIT team reported a programmable logical processor operating with up to 280 physical ^{87}Rb atoms and circuits involving up to 48 encoded logical qubits [69]. The work demonstrated logical control, transversal operations, mid-circuit readout and several fault-tolerant primitives. Post-selection was used in some benchmarks, but it is misleading to characterize the whole experiment as a post-selected realization of fault tolerance.

A second concern is the experimental repetition rate. In analog mode, a complete shot can take about half a second in some systems because atom loading and preparation dominate the cycle time (see the decomposition in Fig. 6 of [2202]). The programmed coherent evolution itself can take only about 5 μs, with additional time for imaging, atom disposal and reloading. Faster loading, rearrangement and readout could improve the repetition rate by one to two orders of magnitude. Scaling also requires efficient atom placement and control because tweezer rearrangement and coherent many-body evolution generally use different optical configurations (Figure 239).

In gate-based mode, the main speed trade-off is architectural. Coherent Rydberg entangling pulses can be hundreds of nanoseconds to a few microseconds, while atom transport, rearrangement, cooling and imaging can take orders of magnitude longer. Zoned architectures trade this transport latency for flexible many-to-many connectivity and transversal logical operations. Resource estimates therefore exhibit a space-time trade-off rather than a simple "slow-gate" limitation, and compilation aims to maximize parallelism and minimize transport [2203, 2204].

1.8.3 Qubit operations

We look here at the way qubits lifecycle works in a cold-atom gate-based model, from initialization to readout, with quantum gates in-between [2205, 2206]. There are some commonalities with the way analog quantum simulations work in these devices. All these operations are using atom energy transitions which depend on the element and on the encoding of the qubit in atom energy levels (Figure 241).

The general principle is as follows:

- **Quantum state**. The $|0\rangle$ and $|1\rangle$ basis states are two selected internal states and are not generally a ground and an excited state. In alkali gate-based processors they are commonly two hyperfine ground states. Other encodings use nuclear-spin, metastable,

cold-atom qubit manifolds: analog Rydberg simulation vs gate-based encodings

gate-based side split by atom class, then by physical manifold for two-electron atoms

family	analog simulation		gate-based				
atom class	Rydberg-based alkali or two-electron atoms		alkali hyperfine with one valence electrons	alkaline-earth-like with two valence electrons			
atom species	^{87}Rb, ^{88}Sr	^{87}Rb	^{87}Rb, ^{133}Cs	^{87}Sr, ^{171}Yb	^{171}Yb	^{88}Sr	^{88}Sr, ^{171}Yb
qubit type	**gr-qubit** ground–Rydberg	**rr-qubit** Rydberg–Rydberg	**gg-qubit** ground–ground	**ground nuclear spin** $^1S_0$, m_I	**metastable / clock nuclear spin** $^3P_0$, m_I	**fine-structure qubit** $^3P_2$–$^3P_0$	**optical clock qubit** $^1S_0$–$^3P_0$
encoding states	$\|0\rangle$ = g $\|1\rangle$ = r (Rydberg)	$\|0\rangle$ = r′ $\|1\rangle$ = r (two Rydberg)	two hyperfine ground states (F, m_F)	nuclear-spin sublevels of the $^1S_0$ ground state	nuclear-spin sublevels of the metastable $^3P_0$	$\|0\rangle$ = $^3P_2$ $\|1\rangle$ = $^3P_0$ (valence spin-orbit)	$\|0\rangle$ = $^1S_0$ $\|1\rangle$ = $^3P_0$ (electronic energy)
transitions	UV or visible / IR lasers	microwaves	microwave (hyperfine) + optical (Rydberg gates)	RF / microwave (nuclear spin) + optical (Rydberg gates)	clock laser + RF (spin) + optical (Rydberg gates)	THz Raman ($^3P_2$–$^3P_0$) + mag. quadrupole init	ultrastable clock laser (698 nm Sr, 578 nm Yb)
T_2* order of magnitude	**2 to 100 µs**	**22 µs**	**~1 to 10 ms**	**up to ~40 s**	**~1 to 10 s**	**10s of ms**	**up to 10s of s**
industry vendors	QuEra, Pasqal	Pasqal	QuEra, Pasqal, Infleqtion, Q-Factor (?)	atom computing, Google (?)	logiqal, Oratomic (?)	planqc	Google, planqc

Figure 237: The various ways to control cold atoms. The listed T_2^* values are representative orders of magnitude taken from different species. (?): manifold inferred from academic team background and publications, not yet publicly confirmed. Source: [2130] and additions by Olivier Ezratty, 2022-2026.

neutral atoms key takeaways

highlights

- **Large programmable arrays**: up to 11K trapped atoms with single-qubit gates, but two-qubit gates on smaller subsets [107, 2162].
- **Long-lived storage qubits and fast coherent gates**: hyperfine coherence of 12.6 s in a 6,100-atom room-temperature array [2162], and parallel CZ gates with 99.5% fidelity in 2023 [107].
- **Identical atomic species**: same isotope atoms share the same energy transition. Variability is elsewhere with local light shifts, traps inhomogeneity, and addressing laser fields. demonstrations.
- **Programmable logical processing** with reconfigurable atom arrays, including transport-based transversal operations and fault-tolerant primitives, demonstrated in 2023 [69].
- **Works in both** simulation and gate-based paradigms.
- **No qubit-bearing solid-state chip required**, although large systems still need RF, optical, photonic and classical-control hardware.
- **Mature AMO hardware stack**: lasers, optics, vacuum systems, cameras and RF/microwave controls. Cryogenics is optional and used to improve vacuum and Rydberg lifetime.
- **Potentially modest QPU thermal load**, but there is not yet a standardized system-level energy benchmark that establishes a general neutral-atom advantage.

challenges

- Crosstalk between qubits can be mitigated with dual-species architectures.
- The experimental duty cycle can be limited by atom loading, rearrangement, transport and readout even though coherent one- and two-qubit pulses are typically sub-microsecond to few-microsecond operations.
- Atom motion is one powerful route to programmable long-range connectivity and low-overhead non-local QEC, but it is not mandatory. Other architectures use long-range Rydberg interactions, local optical addressing or globally driven constructions. Transport adds loss and motional-heating constraints [35].
- Fast nondestructive mid-circuit measurement, reset and ancilla reuse are highly valuable for many QEC architectures [33], although measurement-free fault-tolerant schemes also exist.
- **Optical-power handling**: scaling SLM/AOD systems is constrained by available laser power, diffraction efficiency, thermal loading, optical damage thresholds and uniformity across a large field of view.
- AOD and SLM uniformity is hard to maintain over a large number of tweezers.

variations

- **Dual-species qubits**: to improve QND readout [70, 71] or with same species ancilla atoms using different states [2184].
- **Nuclear-spin qubits**: with longer coherence times, in seconds [2158].
- **Circular Rydberg atoms**: more stable but complex to implement [2185].
- **Native fermionic computing**: physical fermionic atoms can reduce or avoid some fermion-to-qubit mapping overheads for fermionic models [2186].
- **Bosonic and large-spin encodings**: cat-like and GKP-inspired encodings provide alternative QEC strategies, with benefits depending on the physical noise bias, control and readout architecture [2187, 2188].
- **Hybrid gate-based and analog**: for specific case studies [2189].
- **Atoms trapped on nanophotonic circuits**: enabling interactions [2190, 2191].
- **Hybrid atom-photon and solid-state interfaces**: nanophotonic, cavity and superconducting interfaces are investigated for readout, networking and heterogeneous architectures [2190–2192].
- **Collective atom encodings and superatoms**: ensemble and blockade-constrained collective excitations provide alternative quantum-information and quantum-optics architectures [2193, 2194].

path to scalability

- **Optical power and stability**: larger arrays require more optical power, larger uniform fields of view and tighter control of intensity, phase and aberrations.
- **Atoms positioning**: large-scale photonic integrated circuits, fiber arrays and metasurfaces to trap up to 10K atoms [31, 32].
- **Vacuum and lifetime**: cryogenic surfaces can suppress background-gas collisions and blackbody radiation and thereby extend atom and Rydberg lifetimes, but room-temperature arrays with more than 6,000 qubits have also been demonstrated [2162, 2195].
- **QND measurement**: using dual species, atom shuttling and other methods [2196].
- **Faster operations and duty cycle**: faster atoms loading and qubit readout [34], fast classical controls (FPGA, ASIC) [76, 77].
- **QPU interconnect**: photon-based, including for memories, and can also use nanophotonic-circuit traps [75].

Figure 238: Neutral atoms qubits key takeaways, with their highlights, challenges, variations and paths to scalability. A July 2026 review paper assembling scientists from multiple academic organizations and industry vendors lays out very well all these challenges and related solutions [2197]. See also another review from China in [2198] and one from Mark Saffman which describes very well the atomic energy transitions used in controlling cold atoms [2199]. Olivier Ezratty, 2021-2026.

clock or Rydberg states. Initialization is usually performed by optical pumping, followed when needed by microwave, Raman or optical rotations.

- **Atoms arrangement**. Unlike qubits fixed in a solid-state circuit, neutral atoms are loaded and arranged before computation and can also be moved during a circuit. The qubits can form 1D, 2D [2207] or 3D arrays [2208]. Atoms are typically produced from a thermal vapor or atomic beam, decelerated and laser-cooled in one or more MOT stages, then transferred to optical tweezers whose positions are generated by SLMs, AODs/AOMs or other optics [2209, 2210].

Rearrangement fills defects and prepares the desired geometry. Its fidelity depends on the light source, trap depth, motional heating and optical aberrations [2211].

Programming SLM/AOD systems becomes increasingly demanding for large arrays. Jian-Wei Pan's team proposed a machine-learning-based technique to rearrange up to 2,024 atoms into defect-free 2D and 3D arrays with a reported approximately constant 60 ms rearrangement time over the tested sizes. The model computes the holograms and control patterns used for real-time rearrangement [2212]. At the architecture level, dedicated compilation can reduce the cost of atom shuttling and rearrangement, as proposed with PachinQo [2213] and other zoned-routing approaches [2214–2217]. High-end FPGAs can further reduce latency in atom detection and rearrangement control [76, 77].

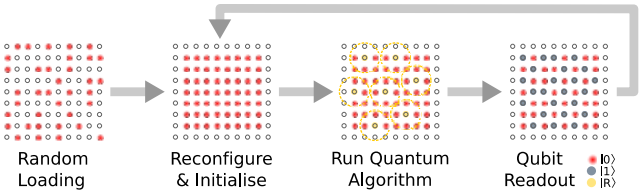

Figure 239: Preparation of a 2D cold-atom array by random loading, followed by reconfiguration and initialization. Source: [2218].

Atom arrangement can also use specific zones with one for storage qubits and single-qubit gates, one for entangling gates and one for readout, as brilliantly demonstrated by Lukin's team in 2023 [69]. While enabling many-to-many qubit connectivity reducing the overhead of quantum error correction with non-local codes like qLDPC, it requires some optimization that can be driven by specific software [2224]. Shuttling happens in several steps with a progressive acceleration imprinted on the atom, the transit where the shuttled atom travels between sites, the deceleration, and some cooling and stabilization before a gate can be executed.

- **Single-qubit quantum gates** implement arbitrary rotations using microwaves, Raman transitions, optical clock transitions or combinations of global drives with local light shifts, depending on the encoding. They are not generally limited to $R_z(\theta)$ operations. Single-qubit fidelities above 99.9% have been demonstrated [2162, 2225]. Stabilizer QEC itself mainly uses Clifford operations, measurement and reset. Universal fault-tolerant computation additionally requires a non-Clifford resource such as logical T or CCZ gates, usually implemented through transversal constructions, magic-state protocols or gate teleportation [2226].

- **Two-qubit quantum gates** are commonly mediated by temporary Rydberg excitation and Rydberg blockade or resonant dipole-dipole interactions [2227]. In 2023, Evered et al. demonstrated parallel CZ gates with 99.54(2)% fidelity on 20 atoms and 99.48(2)% on 60 atoms [107]. A 2026 preprint reports 99.85% without post-selection and 99.94% with post-selection in a zoned architecture [117]. Multiqubit Rydberg gates are also possible.

  The main error channels include spontaneous decay and blackbody-induced transitions from Rydberg states, off-resonant scattering, Doppler and motional effects, laser phase and intensity noise, light-shift noise, atom-position uncertainty and atom loss. Rydberg gates can provide interactions beyond nearest neighbors within a finite interaction radius, and atom transport can further extend effective connectivity. Typical demonstrated computational entangling pulses are of order hundreds of nanoseconds to a few microseconds. The 6.5-ns result in [143] is an ultrafast resonant Rydberg energy-exchange experiment, not a benchmarked high-fidelity computational two-qubit gate. In zoned architectures, millisecond-scale transport and imaging can dominate the logical cycle even when the entangling pulse itself is sub-microsecond [69].

  There are proposals to decrease two-qubit gate times, like using an ultrastrong coupling regime between the connected atoms which interact with a shared bosonic mode [2228] and with fast SWAP Rydberg blockade gates [2229].

- **Qubit readout** commonly uses state-dependent fluorescence imaged on a CCD or CMOS camera, as illustrated in Figure 240. Alkali gate qubits such as ^{87}Rb and ^{133}Cs are typically encoded in two hyperfine ground states. Alkaline-earth-like platforms can instead use nuclear-spin, clock or metastable states. A near-closed cycling transition makes one state bright while the other is dark or shelved. Because only a fraction of scattered photons is collected, readout trades acquisition time against heating, loss and state-discrimination error. Cavity-enhanced or single-photon-sensitive methods can substantially accelerate this process.

  Many neutral-atom experiments have historically used destructive or loss-sensitive fluorescence and push-out measurements, which require reloading lost atoms. Modern processors increasingly use nondestructive mid-circuit measurement by moving selected atoms to readout zones, shelving data qubits, using ancillary species or states, adaptive optical protection, or cavities [2196, 2230–2234]. Measurement-free fault-tolerant schemes are also being investigated [2235]. State-selective field ionization is destructive and therefore not QND [2236].

  Leakage and atom loss must be managed for large-scale QEC [2237]. Alkaline-earth-like species provide particularly natural erasure-conversion channels because their level structure can reveal decay outside

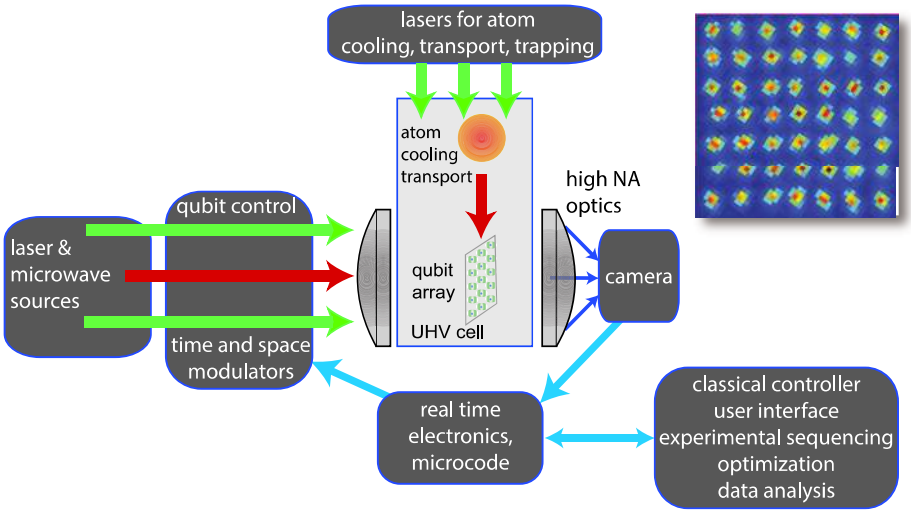

Figure 240: Typical device arrangement for controlling cold atoms. Source: [2219].

the computational manifold [2161], but erasure detection is an encoding- and measurement-design property rather than a universal requirement to replace rubidium. Atom loss can be detected and, in zoned architectures, replenished while other qubits retain coherence. Readout crosstalk, sensitivity, speed and spatial resolution remain additional constraints.

Several recent experiments exceed 99.9% under specific conditions. A cavity-enhanced single-atom experiment reached 99.1(2)% in 200 ns and 99.985(8)% in 9 μs, published in 2025 [2238]. Large-array imaging has also exceeded 99.99% fidelity with high atom survival [2162]. These numbers are not directly comparable because the methods, species, array sizes, destructiveness and survival probabilities differ.

Analog simulations do not usually decompose the evolution into explicit two-qubit gates. Instead, many atoms interact simultaneously under a programmed Hamiltonian whose couplings depend on geometry, Rydberg state, detuning and drive amplitude. Digital-analog quantum computing alternates such analog evolution blocks with discrete gates or local rotations.

Nonadiabatic errors arise when controlled Hamiltonian parameters are changed too rapidly relative to the relevant instantaneous energy gaps, causing population to leave the intended adiabatic eigenstate. Environmental fluctuations can add further transitions, but they are not the defining origin of nonadiabaticity. Counterdiabatic protocols add approximate adiabatic-gauge-potential terms or related controls to suppress these transitions and shorten state-preparation schedules [2239].

1.8.4 Setup

Many neutral-atom systems operate with room-temperature vacuum hardware while the atoms themselves are laser-cooled below 1 mK, often to the few-μK scale before computation. Vacuum pumps reduce background-gas collisions but do not thermalize the atoms. Qubit preparation and control use lasers, beam-shaping optics, SLMs, AOMs/AODs, cameras and, for some encodings, RF or microwave fields (Figure 242). Cryogenic operation is an optional engineering route to improve vacuum and suppress blackbody radiation, not a requirement for controlling large atom numbers.

Figure 243: Example of a glass cell, Infleqtion's Square Cell. Its dimensions are 26 mm × 26 mm × 63 mm. Source: Infleqtion [2245].

Here are some explanations on the other mentioned devices [2246]:

Glass cell. This component hosts the cold atoms in an ultra-high-vacuum environment, typically around 10^{-10} to 10^{-11} Torr in high-performance experiments, to suppress collisions with background gas. It is made from low-outgassing, non-magnetic materials such as fused silica and uses anti-reflection-coated, low-aberration windows for cooling, trapping, manipulation and imaging beams. Typical cells are a few centimeters across (Figure 243) and are surrounded by the MOT magnetic coils. Suppliers include Infleqtion (USA), Japan Cell, Preci-

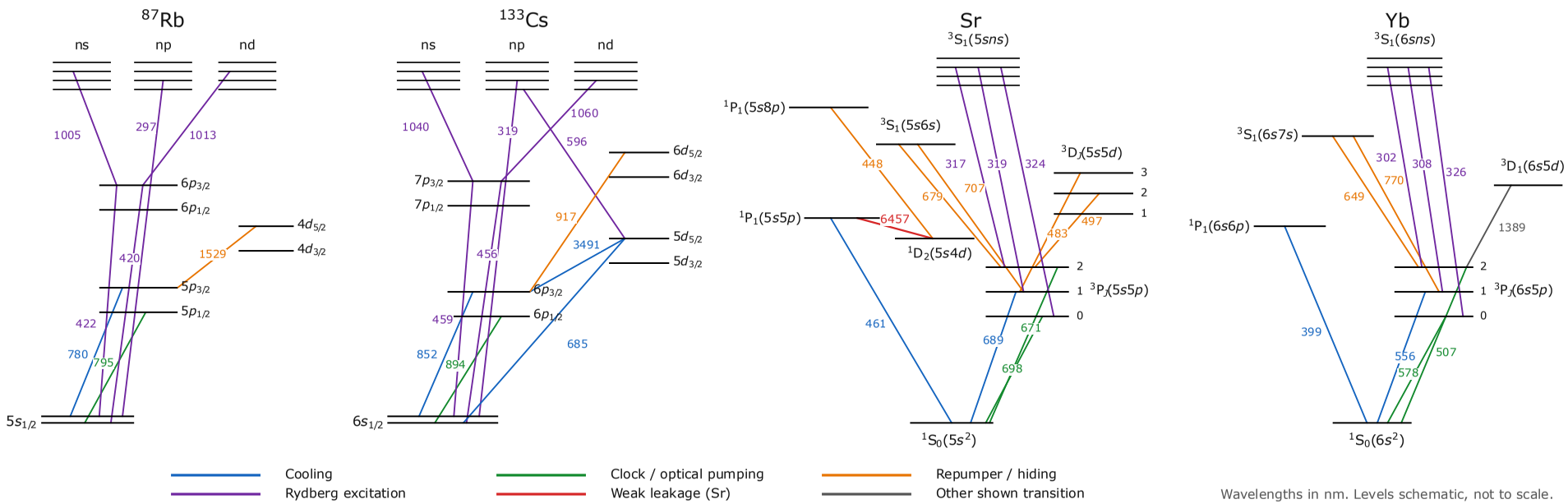

Figure 241: Atomic transitions used with alkali atoms with one valence electron (rubidium and cesium) and alkaline-earth-like atoms with two valence electrons (strontium and ytterbium), showing multiple roles in cooling, state preparation, single- and two-qubit gates and repumping. For strontium and ytterbium, clock and Raman transitions can drive qubit operations while Rydberg excitation can mediate entangling gates. This chart is adapted from [2199]. The ${}^1P_1(5s5p) \rightarrow {}^1D_2(5s4d)$ strontium transition lies near 6,457 nm, not 1,500 nm [2220]. The chart does not show the far-off-resonant trapping light, whose AC Stark shift creates the optical dipole potential. Typical "magic" or convenient trap wavelengths are species- and state-dependent, so the listed wavelengths should be read as examples rather than unique values [2221, 2222]. Standard Rydberg-gate protocols often switch off or modify the tweezers during excitation because the free-electron-like Rydberg polarizability differs strongly from the ground-state polarizability, although this is not universal [2223].

Company	Qubit species	Local single-qubit mechanism	Single-qubit fidelity	Two-qubit (CZ) mechanism	Two-qubit fidelity	Atom shuttling
Infleqtion	^{133}Cs hyperfine clock	Focused light-shift R_Z plus global microwave GR	R_Z 99.902(8)%	Rydberg blockade on individually addressed pairs; interspecies Rb-Cs gate for readout	99.35(4)% (99.73(3)% loss-excluded)	Avoided. Beam steering sets the clock rate; in-place mid-circuit readout [33, 2240, 2241]
Atom Computing	^{171}Yb ground nuclear spin	Individually controlled focused Raman rotations	99.963(2)% (Clifford RB)	Rydberg blockade via state-selective clock excitation, zoned	99.72(3)% (99.40(3)% raw)	Used. Zoned architecture with atom rearrangement [2160]
QuEra (Harvard, MIT)	^{87}Rb hyperfine and Rydberg	Local Raman through a 2D AOD; mostly logical-block level	Not separately standardized here	Global Rydberg pulses in an entangling zone	99.854(4)% raw (99.941(3)% loss-postselected, 2026 preprint)	Central. Coherent transport between zones [69, 117, 2242]
Pasqal	^{87}Rb hyperfine and Rydberg	Local Raman rotations with zoned transport	99.96(1)% (2026 preprint)	Rydberg blockade CZ in digital mode	98.7(2)% median (99.4(4)% peak, 2026 preprint)	Used in a zoned architecture [2243, 2244]
planqc	^{88}Sr optical lattice	Single-site optical-lattice addressing (early stage)	Early stage	Rydberg blockade (early stage)	Early stage	Lattice-based; single-site control is the open challenge [2163]

Table 10: Local single-qubit control, two-qubit gates, and shuttling strategy across neutral-atom quantum computing companies. The reported fidelities use different protocols, array sizes and postselection rules and are therefore not directly comparable as a vendor ranking.

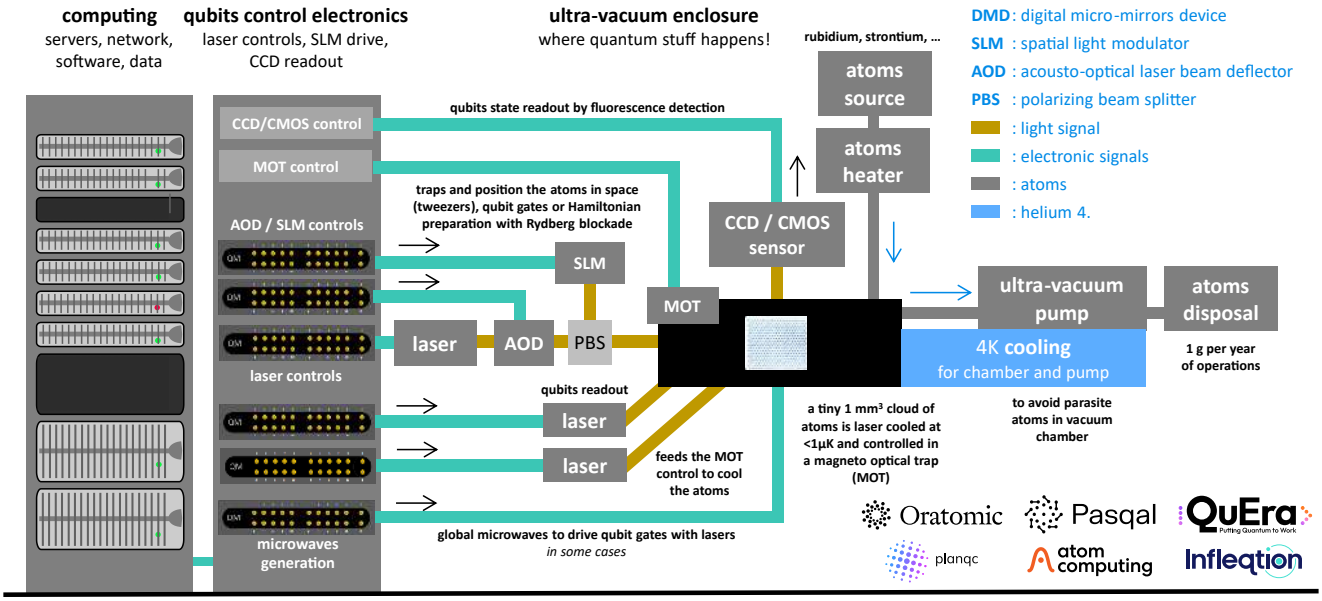

Figure 242: Overall architecture of a cold-atom-based computer. The diagram is schematic. The 4 K cooling path shown is optional and, when used, improves cryopumping and suppresses blackbody radiation rather than generically "avoiding parasite atoms". The "1 g per year" atom-consumption annotation is not a platform-independent requirement and should be removed unless tied to a specific sourced system. ⓒ Olivier Ezratty, 2022-September 2026.

sion Glassblowing (USA), Hellma Optics (Germany), and WZW Optic AG (Switzerland).

MOT (magneto-optical trap) combines three orthogonal pairs of red-detuned circularly polarized beams with a weak quadrupole magnetic field. Doppler shifts provide velocity damping and the spatially varying Zeeman shift creates a restoring force toward the trap center [2131]. Typical MOT temperatures are below 1 mK.

Polarization-gradient or Sisyphus cooling can be applied as a subsequent sub-Doppler stage [2132].

SLM (spatial light modulator) systems shape the phase or amplitude of optical fields. Phase SLMs used for tweezer arrays are commonly based on liquid-crystal-on-silicon devices and synthesize holographic trap patterns. They provide site-resolved, sub-micrometer-scale control of tweezer positions, with finer relative calibration possible in optimized experiments [2247, 2248]. SLMs generate large static or slowly reconfigurable arrays, while AODs provide faster beam steering and transport. Their finite update rate, optical power handling, field of view and uniformity are important scaling constraints.

Typical tweezer spacings are several micrometers, but there is no universal requirement of 4–5 μm or of being larger than the blockade radius. For blockade gates, the relevant interacting atoms are intentionally placed within the chosen blockade radius, while analog simulators tune spacing to engineer the interaction graph. In 2024, Caltech reported more than 6,100 ^{133}Cs atomic qubits in 11,998 tweezer sites at room temperature, with 12.6(1) s hyperfine coherence, 99.9834(2)% global single-qubit gate fidelity and imaging fidelity above 99.99% [2162]. This demonstrated large-scale trapping and coherent single-qubit control, not simultaneous high-fidelity entangling gates on all 6,100 atoms.

AOMs (acousto-optic modulators) and **AODs** (acousto-optic deflectors) use the acousto-optic effect to diffract, frequency-shift and steer light with radio-frequency acoustic waves. A piezoelectric transducer launches an acoustic wave in a crystal or glass-like medium, producing a traveling refractive-index grating [1903, 2249]. In tweezer systems, an SLM can generate a large trap pattern while one or more AODs provide faster beam steering, local rearrangement and transport between storage, entangling and readout zones. Acousto-optic modulation could also be integrated directly in photonic circuits. A CMOS-fabricated SiN acousto-optic modulator performing GHz-frequency phase and frequency modulation of high-power visible light was demonstrated in 2026 [2250]. Such devices could eventually integrate part of the spectral-control chain required for Raman gates, cooling and state preparation, although they do not provide the spatial beam-steering function of an AOD. The same approach also applies to trapped-ion hyperfine qubits.

In the spatial control domain, holographic metasurfaces can replace part of the bulk-optics or SLM function for static generation of very large tweezer arrays, with demonstrations and proposals ranging from tens of thousands of traps to more than 10,000 trapped atoms [31, 32, 2251] (Figure 244). This approach is studied by Infleqtion, Columbia University [2252, 2253], and several groups in China. Conventional passive metasurfaces do not provide fast dynamic reconfiguration by themselves, so sorting and defect correction require an additional active element such as an AOD, SLM, EOD or movable optical path.

Optics. Optical fields shaped or steered by SLMs and AODs are relayed to high-NA (numerical-aperture) microscope objectives with shallow depth of field and finite field of view, typically positioned close to the science cell.

Image sensors. CCD, EMCCD and CMOS cameras are used both for atom-array imaging and qubit readout. Their required speed depends on the architecture. Conventional fluorescence imaging can take hundreds of microseconds to milliseconds, while cavity-enhanced readout has reached sub-microsecond discrimination for a single atom [2238]. A QEC-compatible measurement must fit within the error-correction cycle and preserve the unmeasured qubits. It need not be shorter than the longest physical gate. Computational Rydberg gates typically take hundreds of nanoseconds to a few microseconds rather than a few nanoseconds.

Other investigated setups trap atoms near integrated nanophotonic circuits [2190, 2191]. These platforms can enhance local light-matter coupling, routing, readout and photonic interconnect functions, but they also introduce surface-force, heating, fabrication, optical-loss and trapping-uniformity constraints.

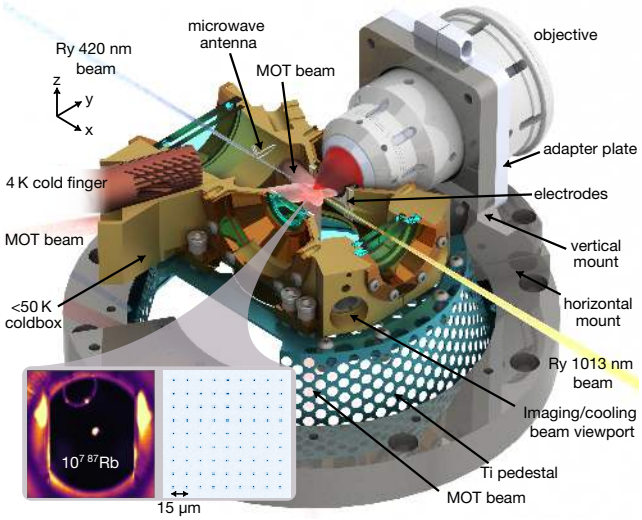

Figure 245: An example of cold-atom setup showing how a high-NA microscope objective is close to the glass cell in the middle, given only one of these is shown here. Source: [152]. Added in September 2026.

Implementing gate-based computing with neutral atoms can use local addressing and, in some architectures, atom shuttling to create programmable non-local connectivity. An alternative proposed by Francesco Cesa and Hannes Pichler and published in 2023 uses only global resonant Rydberg driving, without local addressing [2254]. They present one construction in which the circuit is encoded in the static trap geometry and another in which the geometry is circuit-independent and the algorithm is encoded in the global pulse sequence. Their central result is that a quadratic overhead in atom number is sufficient for universal computation without local control.

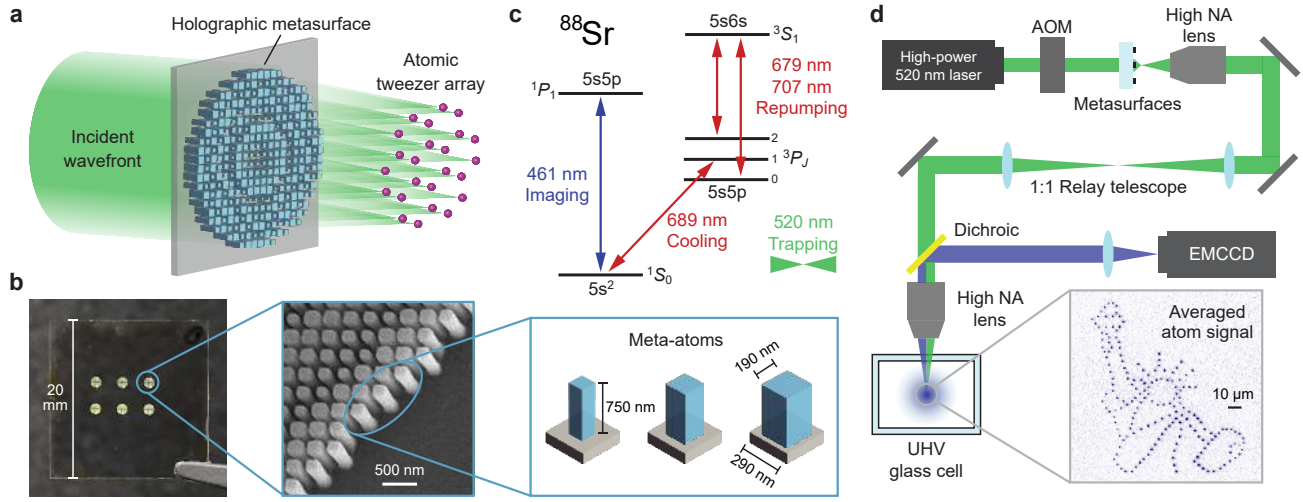

Figure 244: A holographic metasurface imprints a designed phase profile on an incident beam and can generate a very large two-dimensional array of optical tweezers at the focal plane. The metasurface itself is generally static or passively patterned, while dynamic sorting or defect correction can be supplied by AODs or other active optics. Source: [2251].

Cryogeny. Neutral-atom QPUs can operate at room temperature, including arrays with more than 6,000 atomic qubits [2162]. Cryogenic enclosures are nevertheless attractive because cold surfaces improve cryopumping and reduce blackbody radiation, which can extend background-gas-limited trap lifetimes and reduce blackbody-induced Rydberg transitions. A 2025 JILA experiment demonstrated a 3,000-s *atom-trap lifetime* in a cryogenic ^{87}Rb tweezer array [2195]. This is not a 3,000-s qubit coherence time and does not imply that cryogeny becomes necessary above a few hundred atoms.

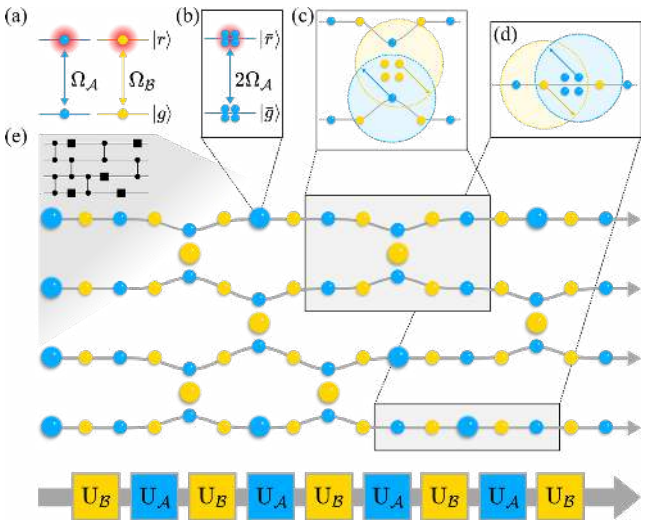

Figure 246: The process described in [2254] enables universal programming of a Rydberg-atom processor without local addressing. It uses dual-species arrays and blockade-constrained collective excitations or "superatoms". One construction imprints the circuit in the static atom arrangement, while the other stores the algorithm in a sequence of global pulses. The paper proves that a quadratic $O(n^2)$ overhead in atom number is sufficient to remove local control. Circuit execution also incurs a pulse-count overhead that depends on circuit size and depth.

1.8.5 Research

The most active research laboratories with cold atom-based qubits are:

- In the **USA** (Harvard with Mikhail Lukin, University of Wisconsin with Mark Saffman [2219] (also with Infleqtion), Adam Kaufman from JILA in Colorado [2255] (part of Google since March 2026), Caltech in Manuel Endres team [2256] (which led to the creation of Oratomic in 2026) and the University of Maryland which is developing dual-species systems using ^{87}Rb and ^{174}Yb [71].
- In **Germany** at Max Planck Institute, Free University of Berlin, University of Stuttgart, University of Darmstadt [2257, 2258] and with the startup Planqc. **Johannes Zeiher** from the Max Planck Institute of Quantum Optics created SNACQ in 2022, a research group on cold atoms ("Scalable Neutral Atom Quantum Computing"). Its ambition is to create the first error-corrected logical qubit [2259]. It complements **Immanuel Bloch**'s team (Quantum Many-body Systems) which proposed in 2026 to use atom velocity as a new degree of freedom and controlled Doppler shifts to implement state preparation and measurement on moving atoms [2260], **Gerhard Rempe**'s group (Quantum Dynamics) and **Arno Rauschenbeutel**'s team at Humboldt-Universität in Berlin. At last, Kristel Michielsen from the Jülich Supercomputing Center is benchmarking cold-atoms systems from Pasqal and QuEra and comparing these with its HPC-based classical simulator, particularly to characterize these systems' noise [2261, 2262].
- In **France** with Institute d'Optique Graduate School with Antoine Browaeys and Thierry Lahaye who co-founded Pasqal, the Unistra laboratory in Strasbourg run by Shannon Whitlock along with Guido Pupillo, who are behind the project aQCess and the European

Flagship EuRyQa (with Pasqal) [2263] and the ENS LKB and Michel Brune's team which is investigating circular Rydberg atoms [2185, 2264, 2265]. Guido Pupillo and the QPerfect team are advancing the field of controlled gate-based cold atom quantum computing and QEC [2266–2268].

- In the **UK** at the University of Cambridge and the University of Strathclyde in the group of Jonathan Pritchard [2269].
- In **Austria** at the University of Innsbruck, particularly with Hannes Pichler [2270, 2271] and the University of Vienna.
- In **the Netherlands** at the Eindhoven University of Technology [2272].
- In **Singapore**, several teams are working on cold atoms with Kai Dieckmann (CQT, NUS) and Wenhui Li (CQT, NUS) who focused on fundamental physics, David Wilkowski (NTU, CQT, and Université Côte d'Azur) who works on strontium for quantum simulation and quantum sensing, and Rainer Dumke (NTU, CQT) who works on atomtronics, and miniaturized optics.
- In **Taiwan** at Academia Sinica and NTU [2273].
- In **Russia**, researchers from Lomonosov Moscow State University and the Russia Quantum Center develop cold atoms Rubidium based simulators, supporting 72 qubits as of 2026, with sub-stellar two-qubit gate fidelity of 94%. Other researchers at Novosibirsk devised a theoretical dual-species rubidium and cesium analog simulator setup, using atoms arranged in Kagome lattices [2274].
- In **China**, academic teams include the Key Laboratory of Quantum Optics in Shanghai, the Center for Cold Atom Physics in Wuhan, both from the **China Academy of Science** [2275] and **Xidian University** [2276–2278], Jian-Wei Pan's and Guang-Can Guo Hefei labs [2279] and Shanxi University with Tiancai Zhang [2280], and Pai Peng's team who controlled 2,400 ^{174}Yb in 2025 [2281]. Some of these labs are focused on building cold atom based quantum sensors and repeaters. They also investigate cold atoms quantum computing [2282] with interesting recent achievements in the implementation of gate-based models [2283]. As with other qubit modalities, the principal challenges concern scalability and the implementation of non-destructive qubit measurement to enable QEC and FTQC. In 2025, a research team from multiple universities and public labs sold a 100-qubit cold atom QPU to Pakistan, Hanyuan-1, with two-qubit gate fidelities of 98%. Another one was sold to China Mobile. In 2025, Pan's team proposed an original system using "orbit qubit" where the qubit state corresponds to the atom occupying left or right wells in a lattice, which enables some MBQC model (see this topic in the photon qubits subsection) [2284]. In 2026, Tsinghua's University in Beijing also trapped 11,000 individual atoms in a tweezer array using a 2 cm diameter metasurface that removes the need for diffractive optics to focus the tweezer light on the atoms [32], this work being done with the help of Qosmos, a developer and service provider of atomic quantum computing technology (Figure 247). This was based on the realization in December 2025 of a 78,400 optical tweezers metasurface [2285]. Other teams in China are developing fiber-array optical techniques to control individual atoms with very low atom losses and heating effect [2286].

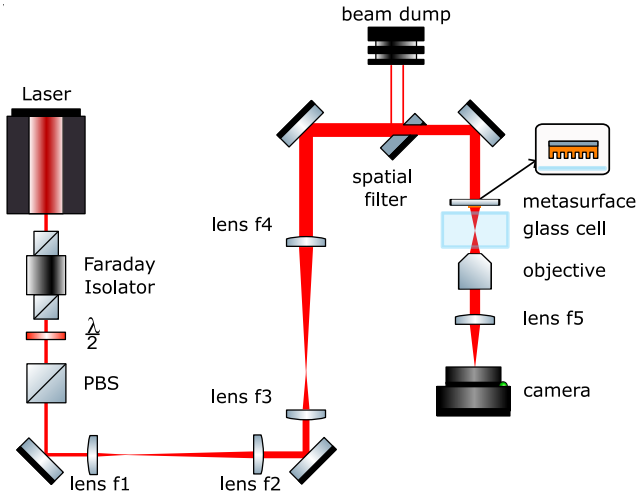

Figure 247: Tsinghua University tested the control of 11K cold atoms using a metasurface chip in 2026. Source: [32].

- In **Japan**, RIKEN, Osaka University, NTT and the Institute for Molecular Science are active in neutral-atom research [2287]. Kenji Ohmori's group demonstrated ultrafast resonant energy exchange between two single Rydberg atoms on a 6.5-ns timescale [2288]. This is an important coherent-interaction result, but it is not equivalent to a fully benchmarked computational two-qubit gate with a quoted logical truth-table or randomized-benchmarking fidelity. The group has also developed large 2D arrays and, in 2026, announced the Shunkai full-stack prototype.
- In **South Korea** at KAIST [2289].

Another European H2020 project, **AtomQT**, covers research with cold atoms, both qubits and sensing. In France, it involves the Bordeaux Optics Institute and the LPMMC in Grenoble with **Benoît Vermersch**.

In 2017, Mikhail Lukin's team from **Harvard** University and a team from **MIT** assembled 51 rubidium atoms [2290]. It went up to 256 qubits in July 2021 [2291]. In 2023, it handled two-qubit CZ gates with 60 atoms with 99.5% fidelities [107]. Antoine Browaeys's team at **Institut d'Optique** reached 72 cold atoms in a 3D structure in 2018, 196 in 2020 [2292], 500 in 2021 and 828 in 2024. Several startups are positioned in

the cold atoms computing market, including **Infleqtion** (formerly ColdQuanta, 2007, USA, working initially on quantum sensing), **Atom Computing** (2018, USA), **Pasqal** (2019, France), **QuEra Computing** (2020, USA, linked to Mikhael Lukin and Harvard) and **Planqc** (2022, Germany).

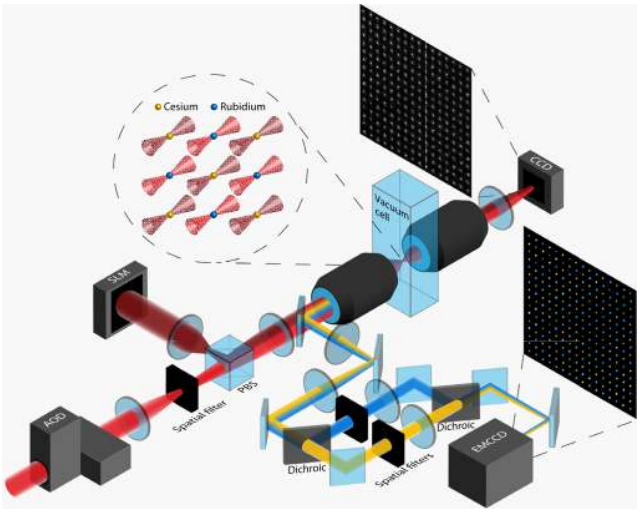

Figure 248: Mixing two types of atoms, cesium and rubidium, from the University of Chicago. Source: [70].

Scalability depends on atom loading and lifetime, qubit coherence, gate and measurement fidelity, transport fidelity, optical uniformity and duty cycle. Parallel CZ gates at 99.5% fidelity were peer-reviewed in 2023 [107], while pushing raw two-qubit fidelity beyond 99.9% with low loss and leakage remains an important target. Dual-species arrays can reduce measurement crosstalk and separate data and ancilla functions [70, 2293].

Many research efforts aim to improve analog-simulation fidelity and scaling [2294], characterize high-dimensional entanglement [2295], understand noise and build error resilience [2296–2300], and measure observables beyond the computational basis [2301]. Three-dimensional trapping is also progressing [2302]. Arrays containing tens of thousands of atoms can demonstrate collective or many-body physics even when they do not provide site-resolved, gate-based control of every atom [2303].

Another direction uses **circular Rydberg atoms** with nearly maximal angular momentum. Their suppressed radiative decay can produce lifetimes above 30 ms and make them attractive for quantum simulation and gate proposals [2304, 2305]. Low-angular-momentum Rydberg states used in most current processors instead have lifetimes typically in the tens-to-hundreds-of-microseconds range for common n, depending strongly on temperature and state [2138]. Describing stationary low-l eigenstates as classical elliptical orbits with a permanent dipole is misleading. Hybrid use of circular and low-l states is also being explored [2306].

Ytterbium and strontium provide additional control options rather than being uniformly "more stable" than rubidium. Fermionic isotopes offer nuclear-spin qubits and narrow optical-clock transitions, while metastable manifolds can support erasure conversion and state-selective operations [2159, 2161]. These advantages come with more complex laser systems and species-specific Rydberg spectroscopy and trapping constraints.

Cold atoms quantum computing can also be based with other programming paradigms, like fermionic computing. One proposal from the MIT associates pairs of cold atoms in 2D optical lattices in which the quantum information is encoded in the vibrational state of the atom pairs [1682]. Other hybrid paradigms are also investigated involving a mix of gate-based and analog circuits [2307]. There are even ways to implement bosonic codes with Rydberg atoms, with cat-codes, the cat-manifold being based on atom nucleus spins [2187] or their hyperfine Zeeman spin [2188], and even GKP codes [2308].

Two other approaches are atom ensembles or "superatoms", used for both gate-based and analog computing [2193, 2194], and hybrid interfaces between Rydberg atoms and other hardware. The work cited in [2192], for example, concerns a Rydberg-atom/superconducting-qubit hybrid rather than a neutral-atom/trapped-ion architecture.

1.8.6 Native fermionic quantum computing

Simulating quantum matter or quantum chemistry involves bosonic, fermionic and spin degrees of freedom. Neutral-atom analog simulators are not restricted to bosonic isotopes. Rydberg spin simulators can use either bosonic or fermionic atomic species because the effective spin Hamiltonian is encoded in internal states with approximately one atom per site, while optical-lattice platforms can exploit the exchange statistics of genuinely mobile bosonic or fermionic atoms.

Electronic-structure problems involve fermionic electrons. On a conventional qubit processor, fermionic creation and annihilation operators are therefore mapped to qubit operators using transformations such as Jordan-Wigner or Bravyi-Kitaev. A different route is a native fermionic simulator or processor based on mobile fermionic atoms.

Sign problem. In many fermionic quantum Monte Carlo formulations, antisymmetry produces configurations with positive and negative, or more generally complex, statistical weights. Their cancellations make the average sign exponentially small in difficult regimes, so the variance of an unbiased estimator grows exponentially and the required sampling cost becomes prohibitive. The Pauli exclusion principle is related to fermionic antisymmetry, but it is not by itself the mathematical cause of every sign problem.

The severity of the sign problem is model-, basis- and parameter-dependent. Many important models have special sign-free formulations, including in dimensions above one. For generic fermionic QMC, however, the

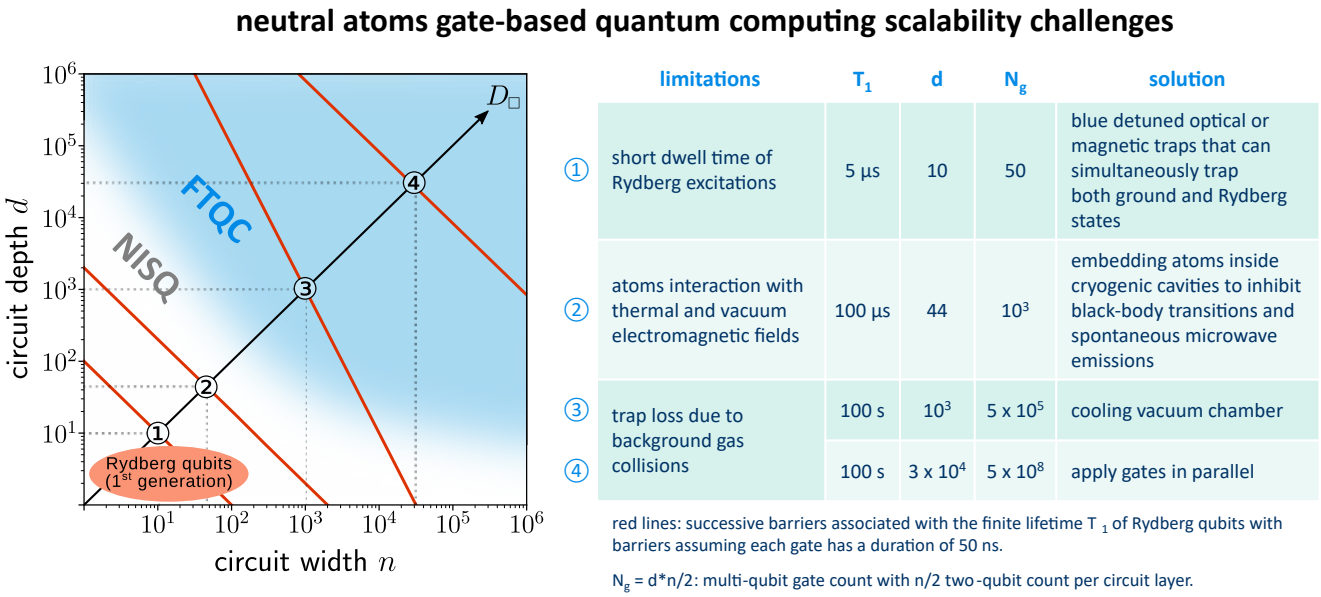

Figure 249: Historical 2022 qualitative sketch of neutral-atom scalability challenges, adapted from [2130]. Modern gate-based neutral-atom processors generally store quantum information in long-lived ground or nuclear-spin states and populate Rydberg levels only transiently during entangling operations. Atom loss can also be detected as an erasure and mitigated by replenishment and QEC. In addition, the chart assumes 50 ns gates, whereas benchmarked high-fidelity computational Rydberg CZ gates are typically hundreds of nanoseconds to a few microseconds. Text formatting by Olivier Ezratty, 2022.

sign problem can produce an exponential computational cost, and finding a generic polynomial-time cure is NP-hard [2309, 2310].

Mitigation and quantum approaches. Several strategies can reduce or avoid the sign problem for specific models [2311]:

- Reformulating the problem in representations or bases that reduce the sign problem, for example through mappings inspired by Kitaev-type honeycomb models implemented with cold atoms [2312].
- Developing new QMC algorithms that are less sensitive to the sign problem.
- Employing methods that approximate the fermionic system while avoiding the sign problem entirely.

Encoding fermions on qubit processors introduces non-local parity information. In a Jordan-Wigner mapping, an individual fermionic operator can contain a Pauli string of length $O(N)$ in an unfavorable ordering. Whether this becomes a long SWAP sequence depends on hardware connectivity and compilation. Bravyi-Kitaev-type mappings reduce parity-string locality to roughly logarithmic scaling at the cost of a more complex encoding. The practical overhead therefore depends on Hamiltonian sparsity, mapping, circuit design and qubit connectivity rather than on a universal fixed gate penalty.

A 2025 proposal from Mikhail Lukin and collaborators maps fermionic problems to reconfigurable qubits using non-local connectivity, mid-circuit measurement and classical feedforward. The method generates dynamical fermion-to-qubit mappings with asymptotic space-time overhead $O(\log N)$ in the worst case, compared with $O(N)$ for generic qubit mappings, and reaches $O(1)$ only for circuits with additional structure such as the fermionic fast Fourier transform [2313]. This favors platforms with programmable non-local connectivity, including neutral atoms and trapped ions. In 2026, Ignacio Cirac and collaborators proposed an encoding that adds a small number of auxiliary fermionic modes to the physical fermionic modes, eliminating long Jordan-Wigner strings for the targeted constructions [2314].

Fermionic computing. A more direct route is to process information in the occupation and motion of physical fermionic atoms or molecules, so that fermionic exchange statistics are native rather than encoded into ordinary qubits. Different isotopes of the same element can indeed be bosonic or fermionic according to the total number of constituent fermions. Trapped-ion and superconducting qubit processors can simulate fermions after a mapping, but they are not themselves native mobile-fermion processors in this sense.

One solution would be to use cold fermionic atoms trapped in optical lattices [2315]. They could be implemented as Hamiltonian simulators as proposed by J. Ignacio Cirac [2316–2318], Immanuel Bloch [2319, 2320] and Markus Greiner [2321] with Fermi-Hubbard quantum simulators. Peter Zoller and Hannes Pichler are behind a proposal for the creation of a gate-based fermionic cold-atom QPU in 2025, using strontium 87 trapped in optical tweezers [2322–2324]. There is even a proposal for a gate-based FTQC fermionic system by Michael J. Gullans at MIT and fellows from the University of Maryland [2325]. Adam M. Kaufman from JILA

and NIST is also working on this topic along with folks already named [2186].

Fermionic systems obey a parity superselection rule: physical observables do not coherently connect sectors of even and odd total fermion parity. This is not the same as a universal prohibition on superpositions of different particle numbers within a fixed parity sector. Proposed fermionic processors can introduce ancillary fermionic modes or reference frames to implement operations while respecting the global parity constraint.

As of September 2026, no commercial vendor had publicly announced a native mobile-fermion QPU as its primary product architecture. Current proposals include gate-based fermionic processors using ^{87}Sr, a fermionic isotope of strontium, with tunneling and interaction gates in programmable optical tweezers. Small-scale proposals include variational algorithms, while key hardware challenges include leakage, phase errors, imperfect tunneling control and atom loss (Figure 250).

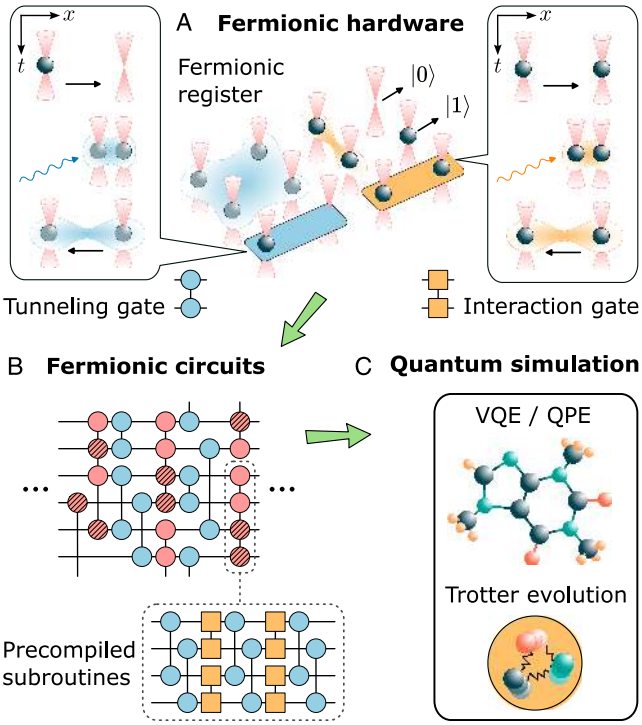

Figure 250: The architecture for a fermionic quantum processor using programmable neutral atom arrays. Quantum information is encoded in the atomic occupation and processed using fermionic gates, including tunneling processes, delocalizing atoms between different tweezers (lighter spheres), as well as interaction gates, based on the Rydberg blockade mechanism. These gates are used to construct fermionic quantum circuits, where certain subroutines are first precompiled to minimize circuit depths. Caption and image source: [2186].

In China, researchers realized an analog fermionic quantum simulator with ^{6}Li atoms in a 3D optical lattice containing about 800,000 lattice sites. This is not an 800,000 individually addressable qubit processor. The experiment studied the three-dimensional Fermi-Hubbard model and observed the antiferromagnetic phase transition [2326].

1.8.7 Vendors

Let's cover them by order of creation.

Infleqtion

USA, 2007, $306M

Infleqtion, formerly ColdQuanta, is a company created by Dana Anderson, now his CTO, which develops laser-based solutions for cooling cold atoms and designs cold atoms gate-based quantum computers.

Company. The startup is in Boulder, Colorado, not far from the NIST Quantum Laboratory. Mark Saffman from the University of Wisconsin is their Chief Scientist for Quantum Information while Fred Chong from the University of Chicago is their Chief Scientist for Quantum Software (he also works for QCI). Their CEO is Matthew Kinsella since April 2024.

In November 2022, the company raised $111M, but to help them focus on developing and selling quantum sensors which are generating short and mid-term revenues. They also changed their name to Infleqtion. They introduced SupercheQ in December 2022 at the Q2B in Santa Clara, a quantum algorithm tool that checks if two files are identical. After its rebranding, Infleqtion was quite silent about neutral atoms computing but research was going on with gate-based mode control of neutral atoms with the work of Mark Saffman from the University of Wisconsin-Madison [2225, 2233]. The startup had over 200 people onboard as of mid-2024. In January 2024, Infleqtion made the acquisition of **SiNoptiq** (ultra-low loss silicon nitride platform) and **Morton Photonics** (silicon photonics-based component and sub-system technologies that enable microwave photonics and sensing systems, ultra-low noise semiconductor lasers). In June 2025, the company raised an additional $100M after a 2024 year with $30M in revenue, this time, back on quantum computing. It announced an upcoming SPAC in September 2025 and became public in February 2026 on the Nasdaq, ending with a relatively modest $2.7B market cap as of early July 2026. It declared having a 12-month trailing $29M revenue stream.

Technology. Their initial core technology was the Quantum Core (Figure 251), a light guide that converges laser beams to control cold atoms that are usually cooled to less than 50 μK. It is integrated into QuCAL, a complete Bose-Einstein condensate generator, and in the Physics Station (Figure 252), a complete optical device for the control of cold atoms that can be used for various purposes. Atom chips are chips that can be integrated in these systems including miniaturized cold atom control optics. The startup uses these generic technologies to create a wide variety of systems, and above all for quantum sensing, especially for geopositioning

Figure 251: Infleqtion Quantum Core.

Figure 252: Infleqtion Physics Station.

instead of GPS, microgravimetry or cesium quantum clocks.

They also sell ultra-high vacuum pumps for the control of cold atoms, called RuBECi as well as a cryogenic trapped ions package and magneto-optical traps, magnetic coils and cold atoms sources. They have equipped the ISS space station with measuring instruments for NASA and JPL.

In January 2024, Infleqtion released the desktopMOT, a commercial cold atom platform for quantum education and workforce development aimed at experimenting with cold atom physics, including light-matter interaction, atom fluorescence, controlling a cloud of atoms with a magneto-optical trap (MOT), practical geometrical optics, light polarization, absorption spectroscopy, laser trapping and cooling and Zeeman effect. This is part of their Oqtant offering for quantum matter experiments.

Their overarching goal was to create and sell cold atoms gate-based quantum computers [2327]. They obtained some funding from DARPA in April 2020 under the ONISQ program with a $7.4M collaborative project involving numerous universities and Raytheon BBN. DARPA asked them to develop a scalable (>1,000 qubits) system that can demonstrate quantum advantage on real-world problems.

The company is focused on creating gate-based systems [2225] (setup shown in Figure 255). Their first 2021 100-qubit "Hilbert" cloud-based quantum system was supposed to work in July 2021 but was said to be commercially available only by May 2022. It was using cesium atoms. It seems the DARPA project did not get through. During the summer of 2022, they released some interesting numbers on their gate-based system with fidelities of 99.4% for single qubit gates (lasting between 0.2 and 5 μs) and 96.5% for two qubit gates (CZ, lasting 0.75 μs), a measurement time of 1.5 ms, a T_2 of 1 second, all of this with 121 qubits. In September 2025, Infleqtion published a preprint on the realization of a 114 atom QPU with their Sqale architecture, supporting all-to-all connectivity and up to 12 error-detected logical qubits obtained by postselection rather than by repeated correction, yielding median logical CNOT fidelities of 99.48%. The code, the physical-qubit count and the retained-shot fraction should be reported alongside that figure [2328]. They are working on ways to improve the fidelity of the Rydberg based two-qubit entanglement gates [2329, 2330]. They also reported a compiled Shor-algorithm demonstration. Such problem-specific compiled demonstrations can validate control primitives, but they do not demonstrate scalable generic factoring because much of the modular-arithmetic structure is specialized away before execution.

Roadmap. In February 2024, Infleqtion announced its 5-year roadmap (Figure 256). First, they presented the Sqorpius QPU with 1,600 cesium atom qubits arranged in a 40×40 array, with no fidelities. They target 100 logical qubits with 40,000 physical atoms and a physical two-qubit gate fidelity of 99.95% by 2028. These are roadmap targets, not demonstrated values. They plan to implement dual species elements, using rubidium atoms as ancilla qubits used for error syndrome measurements [2332, 2333], and to use qLDPC error correction codes [2334]. Their technology roadmap was detailed in an August 2024 preprint [33] (Figure 257). Unlike QuEra, they do not exploit atom shuttling to implement two-qubit gates, but laser beams focused on single atoms, enabling faster gates and circuits and long range entanglement gates as explained by Mark Saffman in May 2025 in [2335]. They obtained a two-qubit

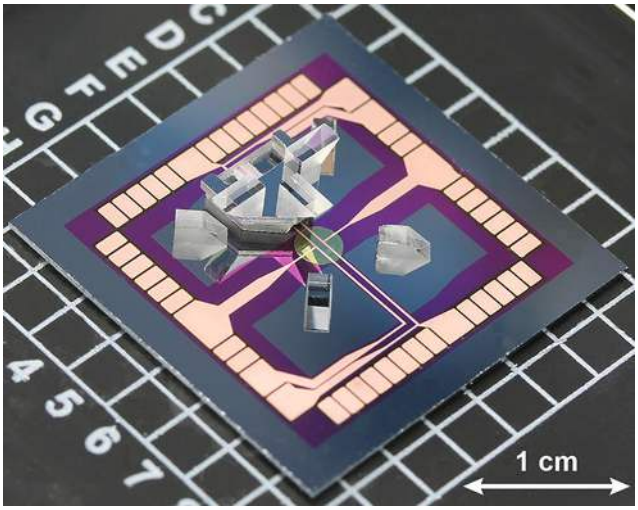

Figure 253: Infleqtion atoms control chip. Source: Infleqtion.

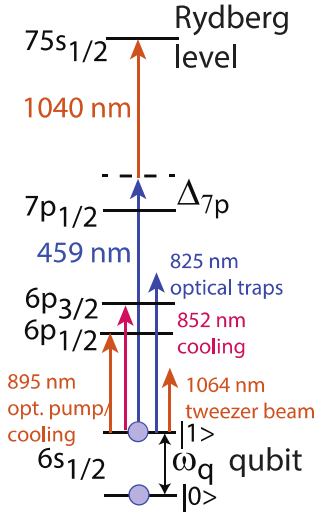

Figure 254: Infleqtion's gate-based system energy transitions in 2022. Source: [2331].

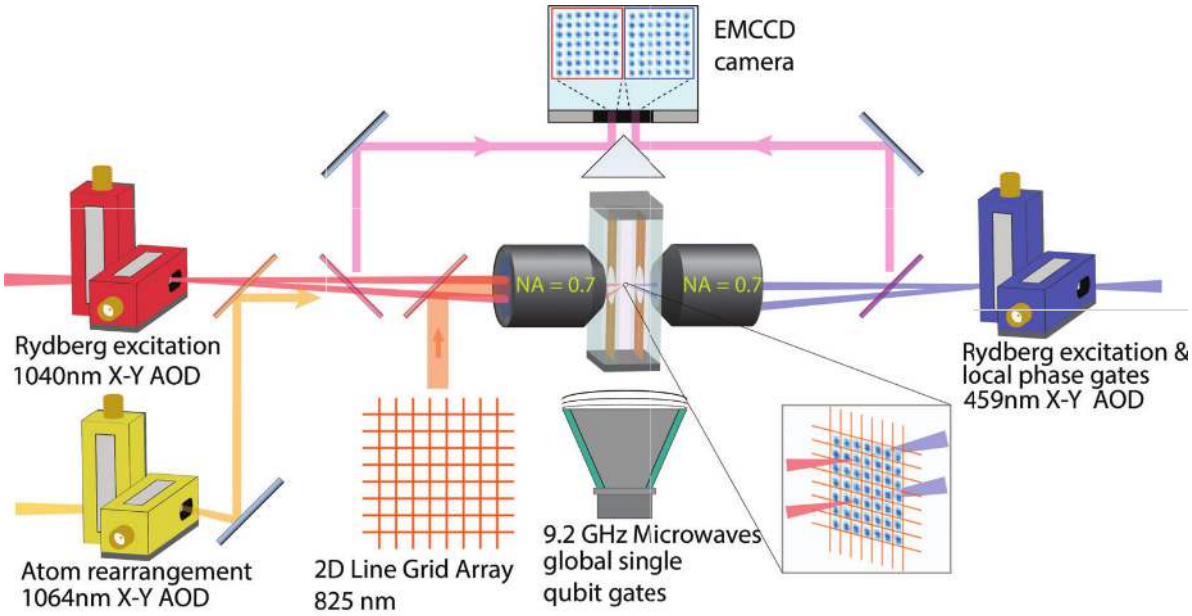

Figure 255: The various lasers used to control Infleqtion QPU. Source: [2225].

CZ gate fidelity of 99.35%, or 99.73% with excluding atom-loss events, and single qubit RZ gate fidelity of 99.902%. They also implemented atoms non-destructive readout (QND) of alkali-atom qubits with an error rate <1%. ON the road to scaling the number of controlled atoms, they work on metasurfaces to replace SLMs using crystalline silicon–on–sapphire (c-SOS) metasurfaces to create optical traps [31, 2336]. In July 2026, along with QPerfect (France), they presented a bus architecture using intermediate atoms to enable long distance communications between atoms from different logical qubit patches. With this architecture, transversal gates with distance up to 25 could be implemented without any atom shuttling, enabling faster operations and reducing source of errors generated by motional atom heating and dephasing errors while shuttling [2337]. In September 2026, Infleqtion announced the support of 30 logical qubits with 80 physical qubits (fewer than the previous experiment with 114 physical qubits). They implemented logical CZ and CCZ (Toffoli) gates, but with still using post-selection [2338].

Software. In May 2021, Infleqtion joined a couple other quantum computers vendors like Pasqal with supporting IBM's Qiskit, formally joining the "IBM Quantum Network". As a result, it seems it became possible to control neutral atom QPUs with Qiskit back in 2022 [2339]. In May 2022, Infleqtion acquired **Super.tech**, a software company providing pulse-level optimization, optimized transpilation and error mitigation techniques (SuperstaQ, which entered as an open beta in September 2023 [2340]) and benchmarking tools (SupermarQ). In 2025, Infleqtion and JPMorgan Chase released an

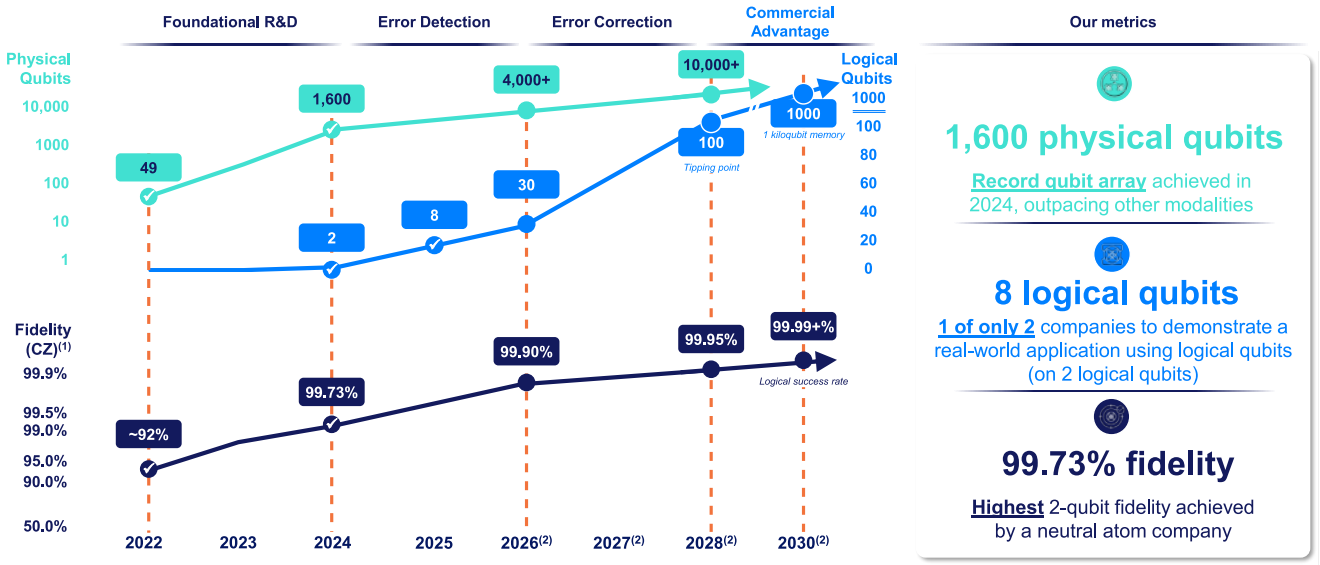

Figure 256: Infleqtion roadmap published in September 2025. In their February 2024 roadmap, they planned to support 8K physical qubits in 2026 and 40K by 2028. As of July 2026, they supported only 100 qubits in gate-based mode. The 1,600 physical qubit number in 2024 doesn't correspond to some commercial viable product. Source: Infleqtion investor presentation, September 2025.

open-source software library, qLDPC, whose goal is to minimize the physical overhead of quantum error correction. It can also help design error-correcting stabilizer and subsystem codes.

In September 2022, the company was awarded a contract to build some AI/quantum machine learning solution for the UK Ministry of Defense as part of the project Q-CALC, which will use SuperstaQ. They are also teaming up with **Classiq** to handle code compilation and with **ParityQC** (Austria) for the development of quantum software targeting optimization problems.

Use cases. Late 2024, they developed a prototype FTQC solution for the simulation of quantum materials using 6 logical qubits [2240]. They tested some Lipkin-Meshkov-Glick (LMG) spin model simulation with VQE running on 3 qubits (! … and in March 2025) [2341].

Customers. In July 2024, Infleqtion deployed a 256-atoms (16×16) analog quantum computer at NQCC in the UK, as part of the Scalable Quantum Atomic Lattice computing tEstbed (SQALE) project [2342]. In March 2026, they delivered this time a 100 qubit system. They were moving backward? Not exactly. This last system seems to be an upgrade to the 2024 machine that supports 100 qubits in gate-based mode [2343]. They were also selected in April 2025 in the first phase of the DARPA QBI program, and in April 2026, they got a $2M DARPA contract under the HARQ program for the development of software supporting heterogeneous quantum computing systems, built on the Multistaq platform to support circuit compilation across multiple qubit modalities and architectures. And they closed in February 2026 a $6.2M funding as part of the ENCODE program from ARPA-E (USA) for the development of quantum-enhanced solutions for optimizing energy grids along with the National Laboratory of the Rockies (NLR), which also works with their competitor Atom Computing. It complements their prototyping of a photon-based neutral atom networking node in 2026 [2344].

Atom Computing

USA, 2018, $300M

Atom Computing develops gate-based neutral-atom quantum computers using nuclear-spin qubits. Its first Phoenix platform used ^{87}Sr nuclear-spin qubits [2159]. The later large-scale architecture and high-fidelity universal gate set use ^{171}Yb ground-state nuclear-spin qubits [2160].

Company. The company was created by Ben Bloom (CTO, coming from Rigetti) and Jonathan King (Chief Scientist, directly coming from Berkeley), joined in 2021 by Bob Hays (CEO). They are based in Berkeley, California. They also established an R&D facility in Boulder, Colorado, in 2022.

Technology. The Phoenix platform assembled individually controlled ^{87}Sr nuclear-spin qubits and demonstrated coherence approaching the minute scale [2159]. Atom Computing later moved to ^{171}Yb, for which it developed large arrays, mid-circuit measurement and a universal gate set [2160]. The platform uses optical tweezers, SLM/AOD beam control and fluorescence imaging, with atom motion between functional zones in later architectures.

Fidelities. Atom Computing's peer-reviewed ^{171}Yb gate benchmark reports a CZ fidelity of 99.72(3)% with post-selection and 99.40(3)% without post-selection [2160]. The system uses zoned operation and atom rearrangement. The cesium forbidden-transition readout result in [127] and the Rb-Cs gate in [2345] are Uni-

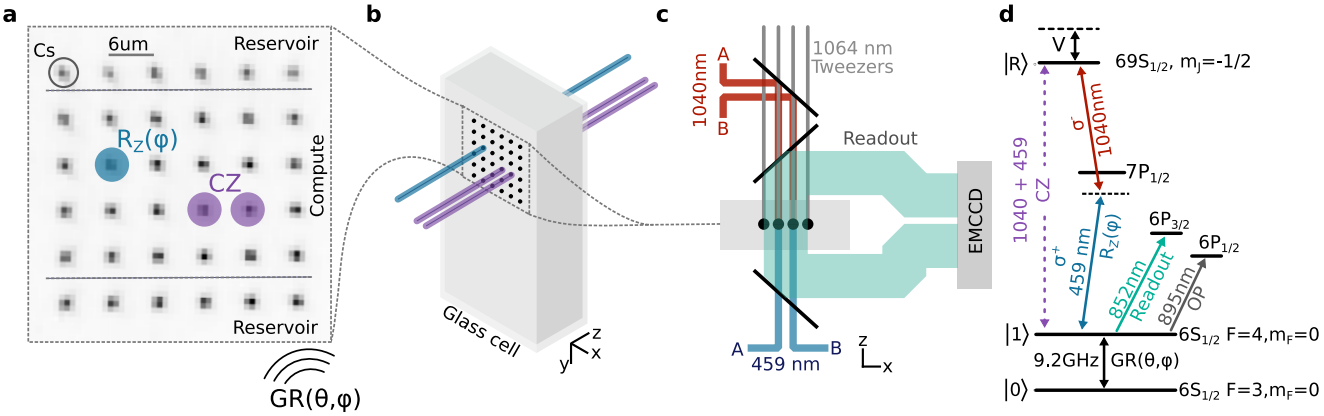

Figure 257: Infleqtion physical architecture as published in August 2024. Atoms are confined inside a glass cell using an AOD (and in the future, SLM) driven tweezers, within the MOT (magneto-optical trap). The test platform supports 32 atoms. Source: [33].

versity of Wisconsin/Infleqtion-related research and are not necessarily linked to Atom Computing.

FTQC. In November 2024, Microsoft and Atom Computing reported logical-state and error-detection demonstrations using neutral atoms. A subsequent peer-reviewed experiment demonstrated repeated mid-circuit measurement, reinitialization and replacement of ancilla atoms while preserving coherence of data atoms, including up to 41 rounds of syndrome extraction in a repetition code [2346]. These are important QEC primitives, although full fault-tolerant logical computation requires additional demonstrations of logical error suppression across complete universal circuits.

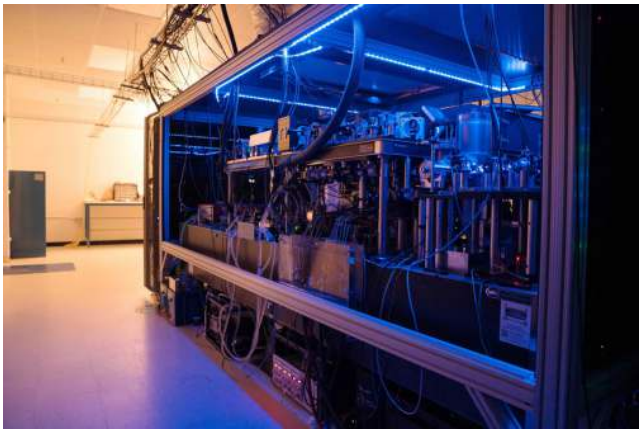

Figure 258: Atom Computing QPU.

Customers. In January 2023, the company got the endorsement of DARPA as part of their inclusion in a five-year program to develop FTQC in the scope of the Underexplored Systems for Utility-Scale Quantum Computing (US2QC) program, that also welcomed Microsoft and PsiQuantum. They finally were not selected in this program in February 2025 but were later selected as part of the first phase of the DARPA QBI program announced in April 2025. In July 2025, Atom Computing and Microsoft sold a QPU to QuNorth in Denmark (Novo Nordisk Foundation) as part of the Magne project, Microsoft handling the software part of the project, error correction and FTQC included. The system with 1,205 atoms is to be delivered by the end of 2026 and operational by mid-2027. Il should support 40 logical qubits, but the supported circuit size is undisclosed since depending on the physical qubit fidelities which could improve over time. The total project budget is of €80M, including half of that for the hardware. A similar configuration was sold to the Amaravati Quantum Valley in India in 2025, but for a total of $186M. Why this cost difference? Probably because it contains other elements. The city also acquired an IBM quantum computer in July 2026. At last, they also got a funding from $100 from the US Department of Commerce (in exchange of stocks) to fund their industrialization effort.

Partners. On the technology side, they announced a software partnership with Entropica Labs in June 2023, with the National Renewable Energy Laboratory (NREL, USA, now NLR) to work on electric grid optimization use cases, as well as in 2026, with Nu Quantum (UK) and Cisco (USA) on quantum computing interconnect, including on transduction.

Pasqal

France, 2019, €253M

Pasqal was cofounded by George-Olivier Reymond (CEO) and Antoine Browaeys (CSO), with the help of Alain Aspect (Nobel Prize in Physics laureate in 2022) who was one of their first business angels and is a scientific advisor for the company.

Company. Pasqal initial funding came through a round of €2.5M led by Quantonation, then a €4.5M grant from the European Union EIC Accelerator [2347], and a second round of funding of €25M announced in April 2021. In January 2023, Pasqal raised an additional €100M. In February 2024, Wasiq Bokhari joined the startup as Chairman of the Board after many stints as entrepreneur and advanced projects executive at Amazon and Google. Loic Henriet became a co-CEO, leading the hardware, software, and product divisions. In July 2024,

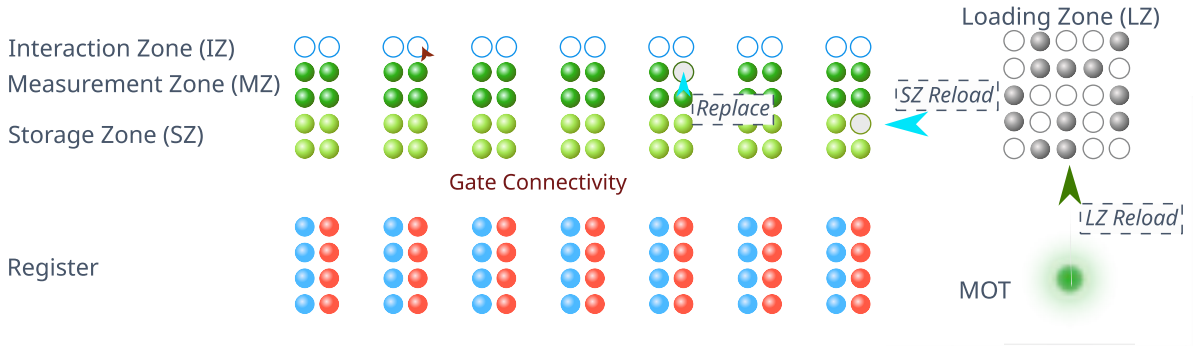

Figure 259: Atom Computing atom arrangement as of mid-2026, with an atom loading zone, a storage zone for replenishment, a measurement zone for qubit readout, an interaction zone for the implementation of two-qubit gates with global control, and a register zone. This was using a total of 96 physical qubits. Source: [74].

the French shipping company CGA-CGM announced an undisclosed amount investment in Pasqal. They opened an office in Boston (USA) and in Sherbrooke (Canada) in June 2022. In March 2025, Wasiq Bokhari became Executive Chairman and Loic Henriet the sole CEO, Georges-Olivier Reymond becoming Chief Strategic Alliances Officer. In June 2025, Pasqal acquired Aeponyx (Canada) to develop its silicon-nitride based photonic integrated circuit technology using laser micro-arrays. Early 2026, Bokhari became the company CEO and Henriet moved back to his former CTO position. As of May 2026, they had about 300 employees. In March 2026, the company announced a SPAC funding led by Bleichroeder Acquisition Corp and an upcoming Nasdaq IPO [2348], valuing the company at $2.6B. The SPAC fueled the company with about $600M in cash.

Pasqal made three acquisitions. It started in January 2022 with Qu&Co (The Netherlands), creating an integrated hardware/software company. But they closed it in 2025. Pasqal also acquired MyCryoFirm, which enabled it to create its customized 4K cryostat for future generations QPUs. In June 2025, it acquired Aeponyx, a Canadian startup creating photonic integrated circuits (PICs) specialized chips enabling precise light control and manipulation.

In 2023, they inaugurated an assembly line for their QPU based in the newly built "Espace Quantique 1" established in Sherbrooke, Québec, Canada, with a $90M 5-year investment plan.

Technology. Their current offer as of Summer 2025 was the Orion QPU (formerly Fresnel), an analog quantum simulator with between 100 and 200 controllable atoms (about half of that in practice depending on the use cases). It is completed by many developer tools stacks including Pulser. They currently use rubidium atoms first cooled in a MOT (magneto-optical trap) using the Doppler laser to reach mK-level temperature and with a variant of the atomic Sisyphus cooling to reach 30 μK. This method also uses lasers emitting orthogonally polarized photons. The method was invented by Claude Cohen-Tannoudji who was awarded the Nobel Prize in physics in 1997.

The atoms are trapped in 2D arrays with a spacing of a few microns thanks to the use of tweezers driven by a laser and an SLM chip controlling the phase of the laser photons reaching the atoms. Qubit states are managed with various modes depending on the use case: ground-Rydberg levels (for Ising quantum simulation models, where the atoms are arranged in a graph with specific distances between atoms that match the problem to be solved [2349]), two levels of Rydberg-level energy (for XY quantum simulation model using resonant dipole-dipole interactions), and with ground-ground states (for gate-based model, in future versions). The various XX, XY and XYZ models are adapted to different physics simulations, Ising models being fit for ferromagnetism and XY models for organic compounds and atoms in lattices simulations. XYZ models can be created using the so-called Floquet engineering in XY mode [2350, 2351].

For the standard Rydberg ground-Rydberg encoding, the programmable analog Hamiltonian can be written as

$$\widehat{H} = \sum_i \left(\frac{\hbar\Omega_i}{2}\sigma_i^x - \hbar\Delta_i n_i \right) + \sum_{i<j} V_{ij} n_i n_j,$$

with $n_i = (1+\sigma_i^z)/2$ up to the chosen sign convention and $V_{ij} \simeq C_6/r_{ij}^6$. In a two-Rydberg-state exchange encoding, an XY Hamiltonian takes the form

$$\widehat{H} = \sum_{i<j} \frac{J_{ij}}{2}(\sigma_i^x\sigma_j^x + \sigma_i^y\sigma_j^y),$$

possibly supplemented by local fields. The previous expression labelled "Ising model (XX)" was therefore an XX interaction rather than the standard driven Rydberg Ising Hamiltonian [2352, 2353].

In 2026, Pasqal reported an early error-detection demonstration with a $[\![4,2,2]\!]$ code and post-selection [2243]. The reported median physical values of 98.7% for two-qubit operations and 99.96% for single-qubit operations are *fidelities*, not error rates.

Roadmap. In March 2024, the company announced a roadmap toward gate-based computing and FTQC [2354]. Gate-based qubits use two hyperfine ground states with Rydberg excitation for entangling gates. Ising-like analog Hamiltonians use a ground and Rydberg state, while XY exchange can use two Rydberg states [2355]. Neutral-atom QPUs do not require a qubit-bearing solid-state chip, but scalable systems still rely on specialized optical, photonic, RF and electronic components.

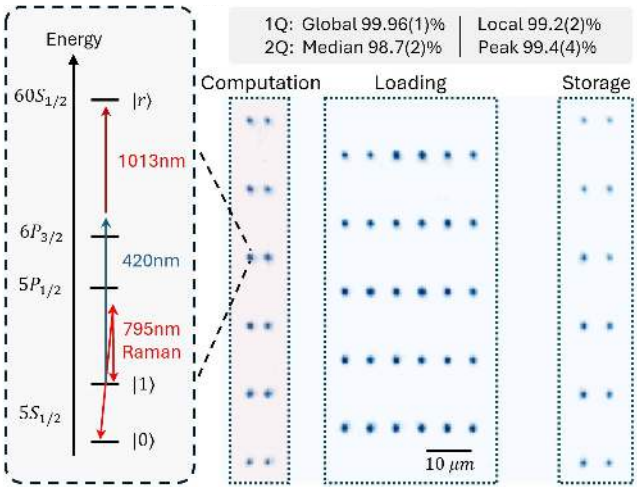

Figure 260: Pasqal's early logical-qubit experiment used error detection together with single- and two-qubit gates in a zoned architecture, with atom shuttling between storage and computation zones and a loading zone used for replenishment. Source: [2243].

In June 2025, Pasqal updated its roadmap with a little more details, without changing much its key milestones, with 200 logical qubits by 2029 and support for 100K operations [13] (Figure 265).

Scientific milestones from Pasqal and the IOGS team include a 196-atom 2D array [2356], parallel gate operations [2357, 2358], and cryogenic optical-tweezer platforms. Cooling surfaces near 4 K improves vacuum through cryopumping and suppresses blackbody radiation, thereby extending atom-trap and Rydberg lifetimes. It does not directly imply the same increase in computational-qubit T_2. A 2026 peer-reviewed Pasqal experiment reported trapping lifetimes around 5,000 s and defect-free arrays of up to 1,024 atoms [2359].

In May 2024, Pasqal and IOGS beat a record by manipulating 828 atoms in their Humber QPU using optical tweezers and two lasers with slightly different wavelengths [2360]. It was extended to the loading and trapping of 1,110 atoms in June 2024 [2361].

In October 2023, the company announced its participation in the PANDA research consortium with the LKB lab at Sorbonne Université, Pixel Photonics (Germany), ICFO (Spain), IOTA (France), to building the foundations for a photonic quantum computer powered by neutral atom technology [2362]. The project is funded by thePathfinder-2023 challenge grant of the EIC. Several research avenues are investigated around the interface between cold atom arrays and photons. One consists of generating photon squeezed states in a deterministic way with cold atoms and the other, to emit photons for QPU interconnect.

Software tools. Pasqal created its own low-level programming environment that interfaces with high-level programming tools, including support for development platforms such as Google's **Cirq** that is supported in emulation mode, in digital gate-based programming mode [2363], **TensorFlow Quantum** and IBM's **Qiskit**.

In April 2023, the company launched **Quantum Discovery** to provide access to its emulators and 100-atom QPU through the cloud. The platform contains three modules: a first one for on-boarding with video tutorials, demos, and a VR Tour of the QPU hardware, a second to interact with the QPU for running and tuning precoded algorithm templates on the QPU or its emulator in Jupyter notebooks and a third one to identify and prioritize use cases through a questionnaire [2364].

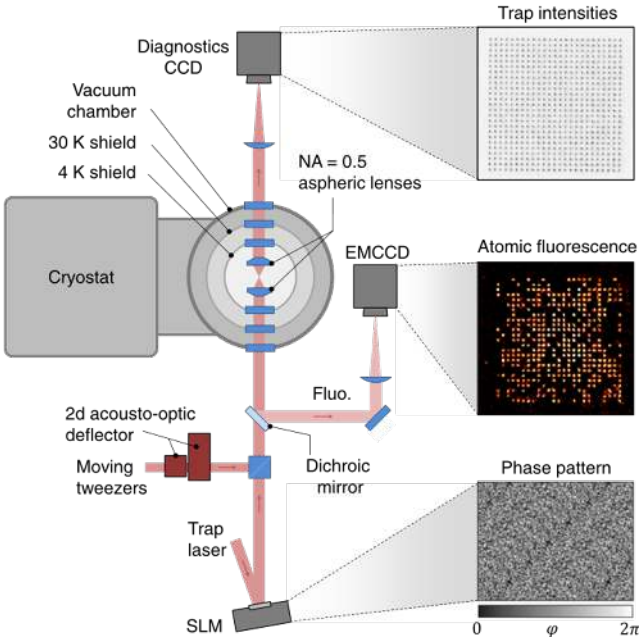

Figure 262: Pasqal's future QPU key components with the cryostat, SLMs, AOD and CCD. Source: Pasqal.

Pasqal's control stack combines SLMs, AODs, polarization optics and fluorescence imaging. In its cryogenic architecture, the 4 K environment improves vacuum and suppresses blackbody radiation. Reported lifetimes of thousands of seconds in such systems refer primarily to atom trapping or survival, not directly to coherent qubit T_2 [2359].

In January 2023, PASQAL launched **Pulser Studio**, a no-code development environment that enables users to graphically build quantum registers and design pulse sequences without coding knowledge (Figure 266). The software platform is open and free to corporate and academic users. It still requires some knowledge on how to run a quantum simulation on PASQAL hardware!

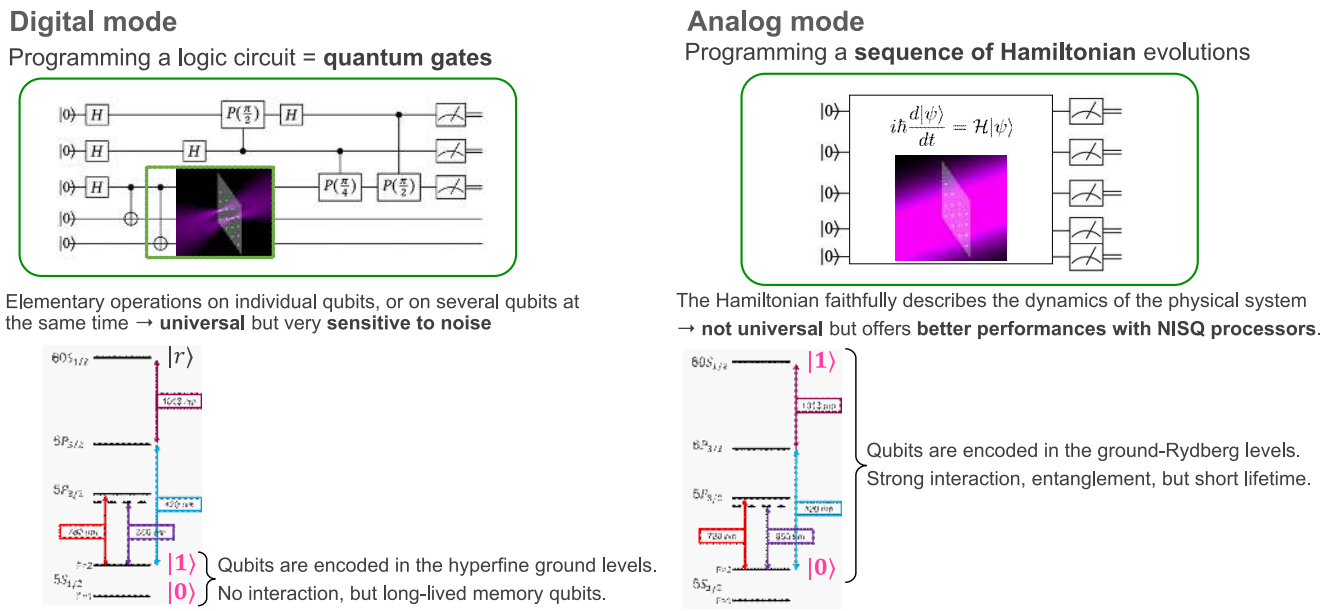

Figure 261: Explanation of the difference between a digital gate-based mode and an analog, quantum simulation mode. Source: Pasqal. 2023.

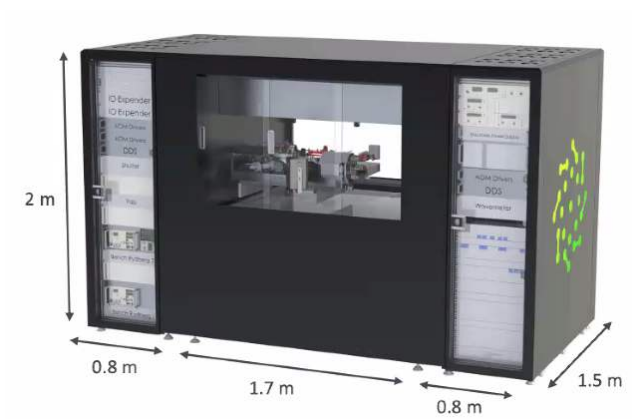

Figure 263: Pasqal QPU Fresnel dimensions. Their visual hasn't changed much with new versions of Pasqal systems (Orion, ...). Whatever, it's a black box surrounding the same optical table with racks of control electronics driving the lasers and other elements in the quantum computer.Source: Pasqal.

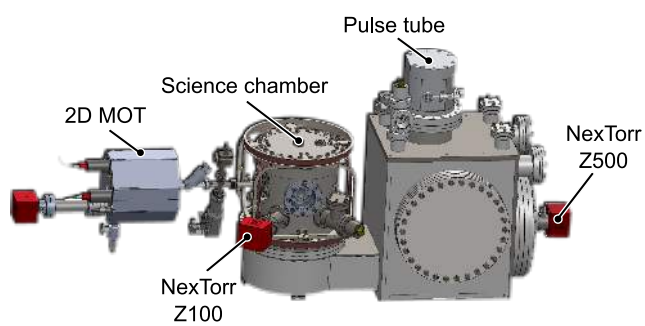

Figure 264: Detailed setup of Pasqal's 4 K cryogenic platform, which demonstrated defect-free arrays of up to 1,024 atoms and atom-trapping lifetimes around 5,000 s. The lifetime quoted here is a trap-survival metric, not a qubit T_2. Source: [2359]. Added in 2026.

At last, they also developed **Qadence**, a high-level programming interface for building complex digital-analog quantum programs mixing quantum gates and quantum simulations [2189].

Use cases. Pasqal published many papers with several research partners and customers, many of them being implemented in classical emulation mode. At this point, as of September 2024, these case studies did not yet demonstrate any quantum advantage although near-term future generation of Pasqal analog quantum simulators with above 300 controllable atoms could potentially change the picture.

Some generic cases are about:

- Solving Minimum Vertex Coloring problems [2365].
- Solving nonlinear differential equations with differentiable quantum circuits [2366].
- Various quantum machine learning tasks [2367–2370], including graph machine learning [2371], graph neural network [2372] and quantum reservoir computing algorithms [2373].
- Benchmarking and resource estimates to obtain some quantum advantage with solving MIS (maximum independent set) combinatorial problems [2374]. They found out in 2025 that they need 1,000 atoms and a 1 kHz repetition rate to demonstrate a computational advantage given their actual repetition rate is currently 1 Hz. They also presented a heuristic to solve

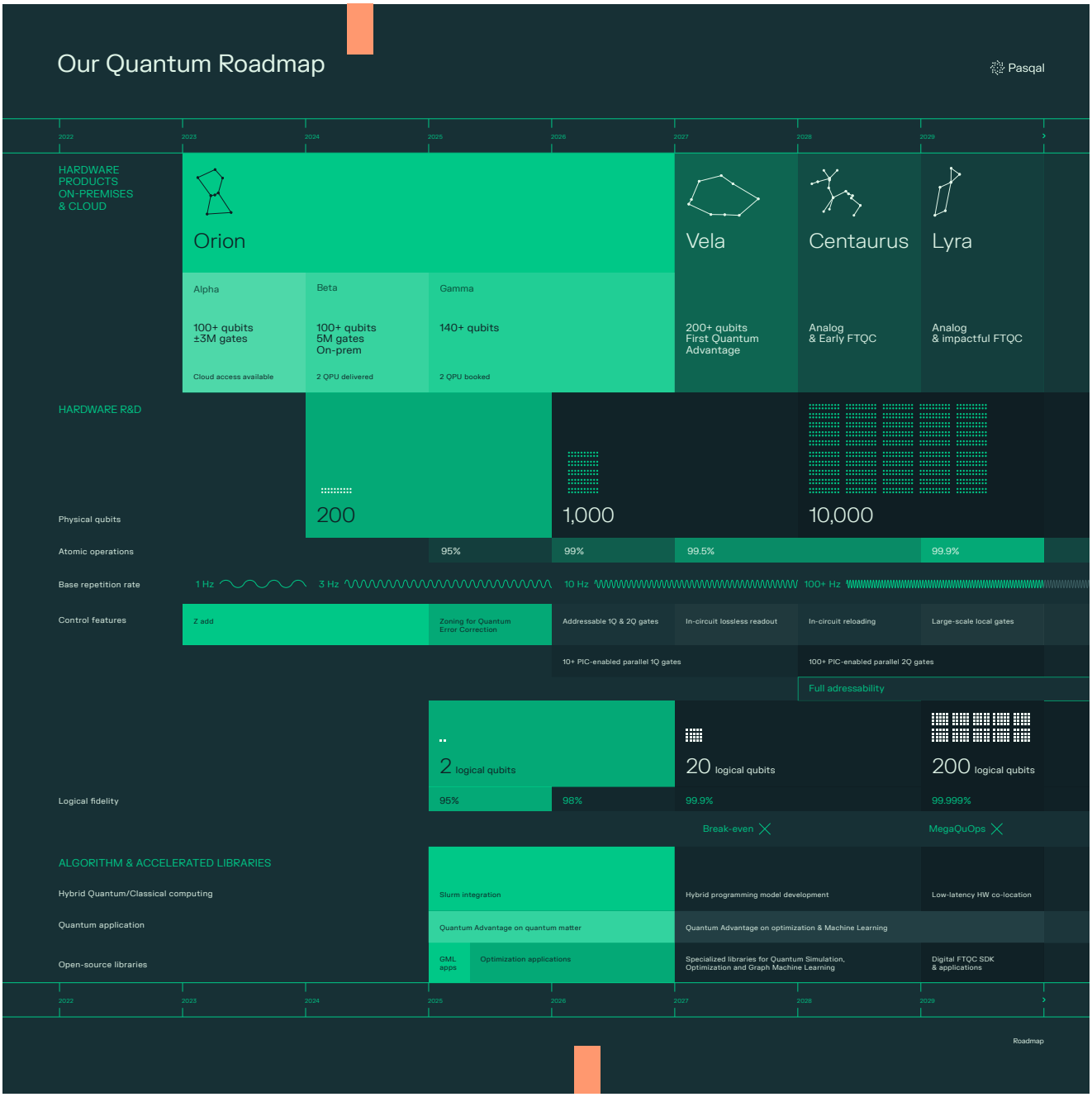

Figure 265: Pasqal roadmap announced in June 2025. Pasqal plans an FTQC QPU using up to 10K atoms by 2028, with an intermediate 1,000-atom milestone. In 2026, a Pasqal-IOGS team including Antoine Browaeys demonstrated defect-free arrays of up to 1,024 atoms in a 4 K platform [2359]; this is an experimental hardware milestone, not by itself a commercial 1,000-qubit QPU. Pasqal also plans to increase the repetition rate by roughly two orders of magnitude between 2025 and 2030. The roadmap target of 99.9% two-qubit fidelity by 2029 remains a forward-looking engineering target rather than a demonstrated value. Source: [13].

Maximum Weighted Independent Set problems which could in some circumstances be faster and more energy efficient than the classical CPLEX solver [2375]. In 2026, a MIS-based benchmark using a variational QAOA approach and a QAA one compared Pasqal Fresnel with 100 qubits running at the Jülich center and a QuEra Aquila 256 qubit system running on AWS with up to 85 qubits for QAA. None could obtain a better result than a classical simulation and the Pasqal system fared lower than the QuEra Aquila system [2261].

Then, we have prototype solutions in various fields and industries:

- A graph machine learning problem to predict products toxicity in 2022 [2376, 2377] and a multi-agent reinforcement learning (MARL) task using PASQAL QEK to optimize semiconductor manufacturing pro-

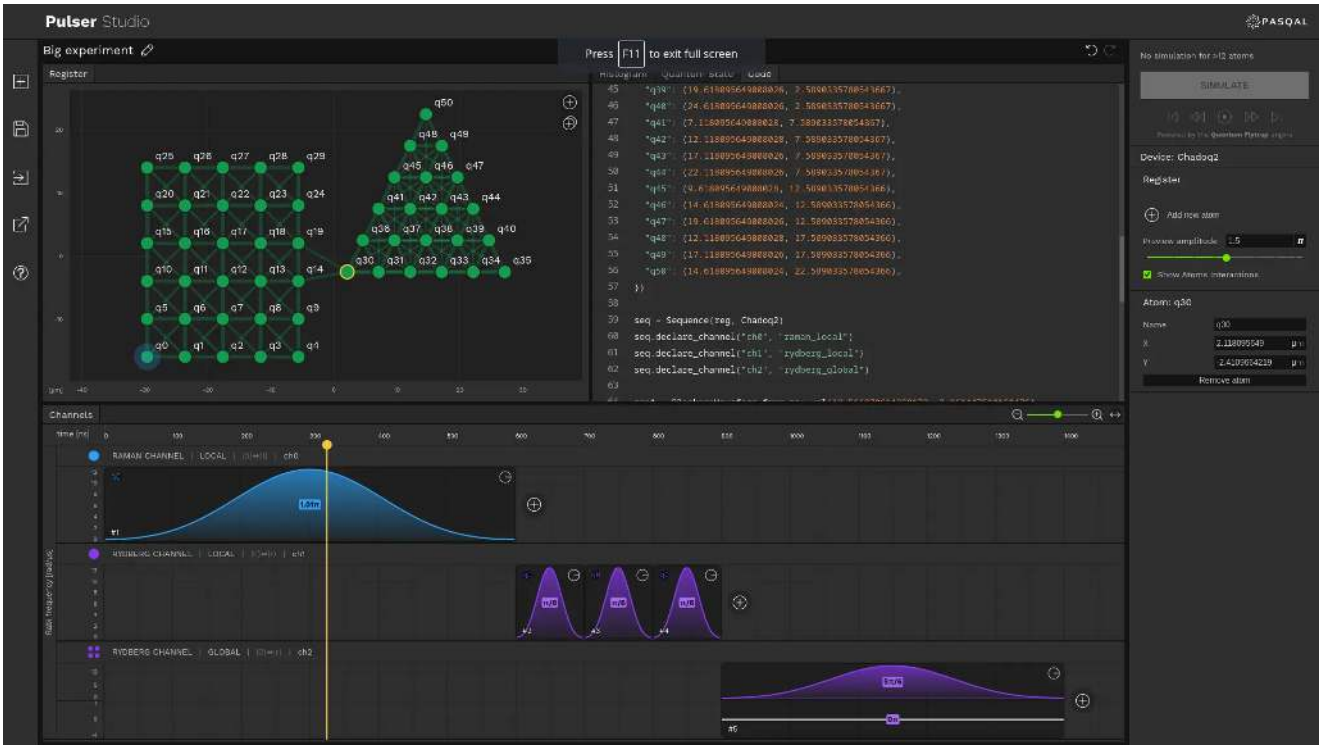

Figure 266: Pasqal Pulser studio user interface showing atoms 2D arrangement and pulse controls. Source: Pasqal. 2023.

cesses [2378], solving graph classification problems also using QEK in toxicity screening of chemical compounds and in the identification of optimal chemical reaction pathways.

- A protein classification using unit-disk graphs in Italy [2379].
- Solving an Ising model simulating ferromagnetism with a 196 cold atoms setup in 2021 [2380], then a larger two-dimensional transverse-field Ising model late 2025 with 324 atoms [2381], a frustrated triangular-lattice magnet $TmMgGaO_4$ with 256 atoms in 2026 [2382], computed the spectral functions of doped magnets in 2026 [2383] and studying the relaxation landscape of the two-dimensional transverse-field Ising model (TFIM) with 256 atoms and configuring a 2D XY model with dipolar Rydberg states in 2026 as well [2384, 2385].
- An analog simulation of two-dimensional Fermi-Hubbard models using 36 atoms, realized in partnership with Eviden and EDF in 2025 [2386].
- Analog simulations for Tomonaga-Luttinger liquid (TLL), a critical phase of matter in 2025 [2387], then of some anti-ferromagnetic Mott insulator that may help in developing high-temperature superconductors [2388], and on some atomic spectroscopy in 2024 [2389].
- A hybrid quantum-classical method to investigate the equilibrium physics and the dynamics of strongly correlated fermionic models using a spin model with Eviden in 2024 [2390].
- Optimizing electrical vehicles smart charging co-developed with EDF, using a QAOA hybrid algorithm and classical emulators of Pasqal systems and the Eviden/Atos Qaptiva emulator in 2021 [2391].
- Enabling robot navigation with Laplace harmonic equations with LG in 2022 and 2023 [2392, 2393].
- Determining the ground state of the usual suspects H_2, LiH and BeH_2 molecules, using an "analog VQE" method and single qubit gates for ansatz initialization and Pauli string readouts with 2 to 6 qubits and 36,500 shots lasting 3.5 hours using a digital simulation, in 2023 [2394].
- A differentiable quantum circuit algorithm (DQC) to simulate a parallel-plate capacitor in a grounded box. It was calculating the potential and the electric field in the box for different distances separating the plates and using the vacuum as the insulator between them, in 2022 [2395]. Another DQC use case concerned weather modeling, developed with BASF in 2024 [2396].
- A fallen angel classification task with CA-CIB and Multiverse in France with real-world customer data, with a qualitative advantage expected to be obtained with 2,800 atoms in analog mode, in 2022 [2397].
- As part of the PASQuanS European flagship project, Eviden/Atos researchers evaluated the specifications of a cold atom simulator needed to reach some quantum advantage to solve an optimization task, the UD-MIS problem (Unit-Disk Maximum Independent

Set problem). A MIS problem is about determining the size of the largest possible independent set in a graph and returning an example of such a set. The Unit-Disk MIS (UD-MIS) problem is the MIS problem restricted to unit-disk graphs. A graph is a unit-disk graph if one can associate a position in the 2D plane to every vertex such that two vertices share an edge if and only if their distance is smaller than unity. They found out that over 1,000 qubits were required with a time budget of 0.2 seconds, if and when the system coherence could be improved by a factor ten [2398].

- In October 2023, Pasqal announced a partnership with the Quantum Transformation Project (QX-PJ) in Japan to develop "Quantum Sky", a 3D aerial traffic management system able to handle hundreds of drones and other low-altitude flying objects.

- Sampling equilibrium water solvent molecules configurations within proteins, with two proposed methods to solve the problem reformulated into a quantum Ising model: a Quantum Adiabatic Evolution (QAE) slowly evolving the system from a known initial ground state to the ground state of the problem Hamiltonian which was implemented in the Pulser classical emulator given individual atoms can't be yet addressed, and a Variational Quantum Algorithm (VQA) using global control fields on the atoms and a classical Bayesian optimization routine looking for the optimal laser parameters minimizing the expectation value of the problem Hamiltonian (Figure 267).

- Contributing to solving a fleet assignment combinatorial optimization problem with improving the quality and diversity of the samples generated, with a hybrid solution competing favorably with a classical Gurobi-based solution in 2025 [2399].

- A low-earth orbit satellite fleet mission planning trial developed with Thales in 2026 [2400]. It solves the so-called Agile Earth Observation Satellite Scheduling Problem (AEOSSP). It was reformulated into a graph problem in analog mode with a QPU supporting 100 atoms. The time to solution (TTS) is still longer than with classical methods but could be improved by at least an order of magnitude to compete efficiently with classical naive MIS methods.

Partners. In July 2020, **Cambridge Quantum Computing** (CQC) announced their support of Pasqal's qubits with their development tool t|ket⟩. Pasqal added a partnership with **ParityQC** with a 3-year collaboration to advance quantum optimization and parallelization [2401, 2402] and released the open-source library **Pulser**, co-developed with the **Unitary Fund** enabling the control of their processor at the level of laser pulses [2403]. It was extended in 2025 with PulserDiff, for the optimization of pulse sequences over a well-defined set of control parameters that drive the quantum computation [2404].

Pasqal also announced a partnership with **Atos/Eviden** in November 2020 to integrate a Pasqal accelerator with Atos supercomputers. Pasqal also works with **Rahko** as well as with **Multiverse Computing**, in association with Crédit Agricole CIB.

They started a two-year R&D partnership with **Kipu Quantum** in June 2023 to optimize quantum algorithmic and use Kipu's algorithmic compression technology that reduces the length of quantum algorithms. Their first 100-qubit quantum simulator went online with **OVHcloud** in May 2022 (in private beta) and, in 2025, on **Microsoft Azure Quantum** and **Google Cloud Marketplace**.

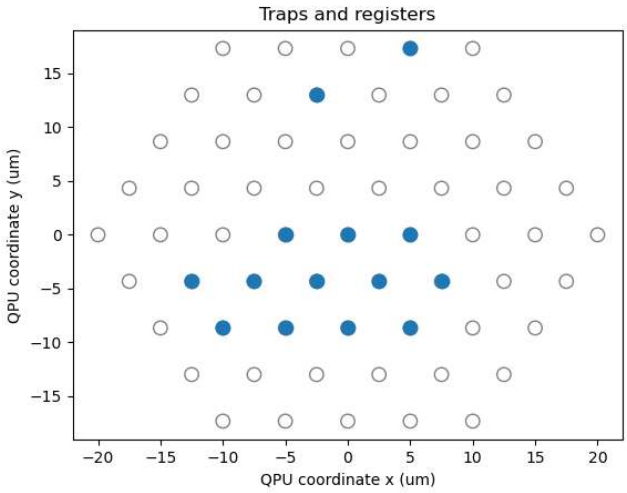

Figure 267: The water placement problem aims to determine the most likely positions of water molecules within a protein cavity. It is reformulated as finding the ground state of a constrained Ising model, where the binary variables represent the presence or absence of a water molecule at a particular lattice point. Rubidium atoms are trapped in a two-dimensional array of 60 optical traps. The algorithm uses a 3D Reference Interaction Site Model (3D-RISM) which generates a continuous 3D density map of oxygen atom distribution within a protein cavity. This map is then sliced into 2D planes. For each plane, a qubit register consists of atoms placed in specific locations in the optical traps, with a number of qubits per slice ranging from 4 to 14, this last case being shown in the chart. Atoms are spaced by 5 μm. Source: [2405].

Pasqal announced a collaboration with **IBM** in June 2024 to study how analog, gate-based quantum computing and HPCs could be complementary for the development of new materials. This is a scientific collaboration. It led to the publication of a 2025 preprint on hybrid analog+gate-based + HPC computing [972].

Pasqal has a technology partnership with KAIST in South Korea on atom control, completed in 2025 by funding from LG Electronics and the Korean Ministry of Trade, Industry and Energy (MOTIE) and the Seoul Metropolitan Government, with **MILA** in Montreal [2406] and with the **University of Calgary** [2407]. They work with Welinq as part of the €4M InterQo project to study the interconnect of Pasqal QPU us-

ing Welinq quantum memory. They are part of the EU PANDA Pathfinder project which is about building a photonic quantum computer using an array of strontium atoms implementing lossless, deterministic photon-photon interactions, with the goal to implement continuous-variable and MBQC architecture. It associates Pixel Photonics, ICFO and Sorbonne Université (Valentina Parigi, also, from Qluster). And at last, in April 2026, they started the €4M CoPaNA project funded by the European Defense Fund to de-velop concatenated parity codes with ParityQC and Thales.

Customers. On hardware side, in January 2021, the Italian HPC consortium **CINECA** announced that they would use Pasqal's Fresnel 100-qubits processor [2408]. It led in 2025 to its selection as part of the EuroHPC joint undertaking, for 140 qubits. It was inaugurated in June 2026. Pasqal was also selected as part of the project EuroHPC HPC-QS to provide two analog QPUs to HPC public datacenters, one in Germany (Jülich Supercomputing Centre at **FZ Julich** *aka* Jülich Research Centre) and one in France (CEA **TGCC** with GENCI). Both Pasqal systems are connected to a Bull Qaptiva server appliance for emulation and quantum system drive. The first was delivered to TGCC in June 2024 and is operational since mid-2025. The Jülich system is operational as well. Pasqal sold one 200 atoms QPU in May 2024 to **Aramco** for implementing QML algorithms in the energy business, and was up and running as of mid-2026. At last, one QPU was also sold to **DISTRIQ** in Canada in 2025.

On the software side, Pasqal has various customer partnerships in place with **EDF**, **Thales** [2409], **GENCI**, **Siemens** (for computer-aided-design and engineering, simulation and testing), **BASF** (fluid dynamic problem solving algorithm), **BMW** (material science and material deformation algorithms). Other engaged customers are Sumitomo, Panasonic, Airbus, Rolls-Royce, Safran, LG, Posco, Fraunhofer and True Nexus (from Saudi Arabia, in pharmaceutical).

QuEra

USA, 2018, $247M

QuEra develops cold atom quantum computer, their first generation being named Aquila [2410].

Company. QuEra was created by researchers from Harvard University and MIT with Nathan Gemelke, Alexei Bylinskii, Shengtao Wang and Mikhail D. Lukin, who is one of their scientific advisors and works on gate-based cold-atom computing [2411]. They had a staff of over 150 people as of mid-2026. Google announced an undisclosed investment in the company in October 2024. It was part of the $235M funding round formally announced in February 2025, along with Softbank and other investors.

Analog simulations. QuEra started with developing and selling cold-atoms analog quantum simulators in 2021 and then quickly shifted gears on the development of gate-based FTQC systems. Their first analog system supported a 2D array of 256 cold atoms was announced in November 2021 [2412]. It became available on Amazon Braket in November 2022. What they branded "programmable quantum computers" were not gate-based systems but analog quantum simulators where they encode graph problems into a layout of cold atoms [2413, 2414]. Typical graph problems are expressed as a "maximum weight independent set" (MWIS) problems that are then turned into several unit-disk graph sets (UDG) which are assemblies of nearby neutral atoms. These sets are connected to each other with Rydberg-based entanglement at their edge. Various problems like QUBO formulations, Ising models and even integer factorization can be mapped onto MWIS problems. This work was completed by the creation of a dedicated compiler by AWS and JPMorganChase in 2025 [2415]. Starting in August 2023, QuEra's Aquila-class 256 qubits quantum simulator became available in three forms: through AWS (48 hours per week), directly through QuEra's Premium Access and leased on-premises. In 2026, QuEra and its academic partners were still investigating analog simulations, and with material design applications [2416].

Gate based. QuEra then focused on gate-based operation with a zoned architecture. Coherent atom transport is used to bring selected qubits into dedicated entangling and readout regions, allowing global or highly parallel control in those zones while retaining programmable many-to-many effective connectivity. This is an architectural trade-off rather than a consequence of local two-qubit control being impossible. After entangling operations, atoms can be transported back to storage or computation zones. Early demonstrations in 2022 prepared logical-code states and hybrid digital-analog circuits with dynamically reconfigurable arrays and CZ gates, but did not yet constitute repeated fault-tolerant QEC [2242, 2417, 2418].

QuEra is also working on non-demolition qubit measurement (QND), a key feature to implement full QEC and FTQC, based on moving selected atoms "*into a readout zone where their qubit state can be rapidly detected via fast, resonant photon scattering on a cycling transition*". They could also use arrays with two atomic species such as two isotopes of the same element or two different elements, with the data atoms being encoded in one atomic species and ancilla atoms encoded in another species that can be easily measured [2419–2421].

In 2023, they implemented a gate-based model with reaching two-qubit CZ gate fidelities of 99.5% with 60 atoms [107]. They beat this record in 2026 with 99.85% fidelities without post-selection (and 99.94% with post-selection), using a reservoir of 374 atoms and bringing up to 20 atoms into the entangling zone [117] (see the related noise budget in Table 11).

Error source	Smooth-amplitude gate in this work
Scattering $\|1\rangle$	0.028%
Scattering $\|0\rangle$	0.018%
Rydberg T_1	0.046%
1015-nm T_2^*	0.008%
420-nm T_2^*	0.001%
Doppler T_2^*	0.007%
Rydberg blockade	0.001%
Rydberg $m_{J=\frac{1}{2}}$	0.002–0.030%
Total fidelity	**99.861–99.889%**

Table 11: decomposition of the two-qubit gate error budget for the 2026 smooth-amplitude CZ gate. It is dominated by the finite lifetime decay of the Rydberg state ($T_1 \approx 80$ µs) and off-resonant scattering from the intermediate excited state, particularly from the 420-nm laser for the $|0\rangle$ state. Additional decoherence channels (T_2^* and T_2) are driven by laser pointing noise that causes time-dependent light shifts, as well as thermal decoherence from the atoms' finite temperature (≈ 12 µK). Position errors come from thermal motional spread and tweezer misalignments leading to variations in interatomic spacing, which induces detuning errors in the Rydberg blockade. Finally, increasing the Rabi frequency introduces phase-dependent off-resonant coupling to the secondary Rydberg level. Source and details in: [117].

Logical qubits. In December 2023, the Harvard-MIT team reported a logical processor using up to 280 ^{87}Rb atoms and circuits involving up to 48 encoded logical qubits [69]. The zoned architecture explicitly included a readout zone for mid-circuit measurement and feedforward while preserving computation qubits. The work explored color codes, surface-code states, transversal logical gates, non-Clifford CCZ operations and fault-tolerant primitives. Some sampling and logical benchmarks used error detection and post-selection, so those numbers can't be extrapolated as deterministic FTQC performance. However, the experiment was not limited to a single QEC round because of destructive readout. The paper's main significance is the combination of programmable logical encoding, atom transport, mid-circuit readout and transversal operations at unprecedented neutral-atom scale.

In 2026, they did a digital simulation of their logical qubits using an encoding rate of 2:1, which exhibited a 1.3×10^{-13} logical error rate using a $[\![2304, 1156, \leq 14]\!]$ code [2423]. This astonishing result came from using a noise model that doesn't account for idle noise and atom losses, the usual assumption of 99.9% gate and readout fidelities, 32 rounds of syndrome extraction per shot, and a stack of three error syndrome decoders one of which using a Gurobi solver but all having seemingly the capability to run in real-time with GPUs. A related benchmarking technique proposed by Harvard/NIST researchers shows that both physical and logical error rates of a fault-tolerant Clifford circuit can be extracted directly from syndrome data with only polynomial sample complexity in the code distance, an exponential improvement over the direct shot-counting approach used above. This method was validated against QuEra's own 2023 logical GHZ-state experimental data [2424].

In September 2026, QuEra and Harvard unveiled their "phantom codes" QEC codes that support entangling logical gates through physical qubits relabeling during compilation [2425]. The main cost is therefore concentrated on generating and using magic states.

Roadmaps. In January 2024, QuEra announced an industrial FTQC roadmap targeting 100 logical qubits by 2026 with more than 10,000 physical qubits and logical error rates of 10^{-6} to 10^{-8} [14]. Separately, a theoretical framework for low-overhead transversal algorithmic fault tolerance was posted in 2024 and published in Nature in 2025 [2426].

After the seminal 2023 paper, QuEra and Harvard/MIT published a flurry of paper paving the road toward FTQC: methods to run qLDPC codes efficiently between August 2023 and October 2025 [2428–2430], the use of a "network" landing zone for atoms, for interconnecting two QPUs in August 2024 [75], the capability to handle magic state distillation in December 2024 [2431] and August 2025 with the tricycle codes, a variant of qLDPC to generate logical CCZ states [2432], an improved way to correct atom loss errors in February 2025 [2433], and a more efficient error syndrome decoder for transversal Clifford gates in June 2025 [2434].

As of mid-2026, their record number of controlled atoms was 3,000 with continuous reloading, or replenishment, of missing loading in their storage zone [72, 73]. This deals only with loading and keeping atoms in place, not yet with handling some analog simulation or gate-based computing (Figure 271). Another atoms replacement technique was developed in 2025 at Princeton by Jeff D. Thompson's team although being slower (500 atoms/s vs 300,000 atoms/s in the case of QuEra) [2435].

In 2025, Harvard and QuEra reported a 448-atom experimental platform demonstrating several ingredients of a universal fault-tolerant architecture [2422]. The work included repeated surface-code error correction with below-threshold scaling, logical entangling operations, magic-state-related primitives, nondestructive readout and reinitialization. The reported error-suppression factor was about 2.14 per increase in code distance for the characterized surface-code regime. The result is a major neutral-atom QEC milestone, but statements such as "largest ever for any platform" are not scientifically robust because scale depends on whether one counts physical qubits, simultaneously controlled qubits, encoded qubits or active gate sites.

The peer-reviewed 2025 work on "transversal algorithmic fault tolerance" combines transversal logical operations with correlated decoding and shows that a constant number of syndrome-extraction rounds can suffice for a broad class of codes, rather than the $O(d)$ rounds required by standard constructions in the analyzed settings [2426]. Circuit-level simulations indicate that this

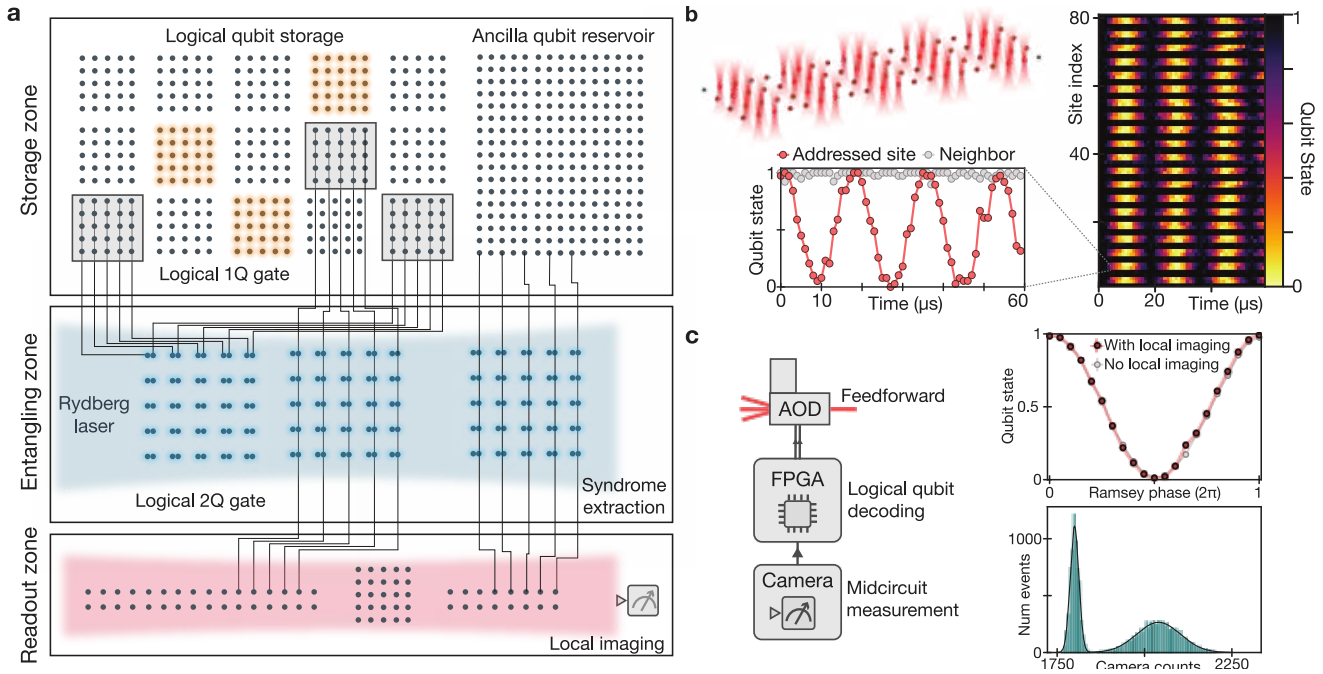

Figure 268: QuEra's logical qubits 2023 experiment relied on moving the atoms around to implement two-qubit gates and mid-circuit measurement. There is a fourth "reservoir" zone at the bottom, not shown in the picture, where spare atoms are loaded to fill space in the storage zone at initialization or when atoms get lost (*aka* erasure error). Sources: [69, 2422].

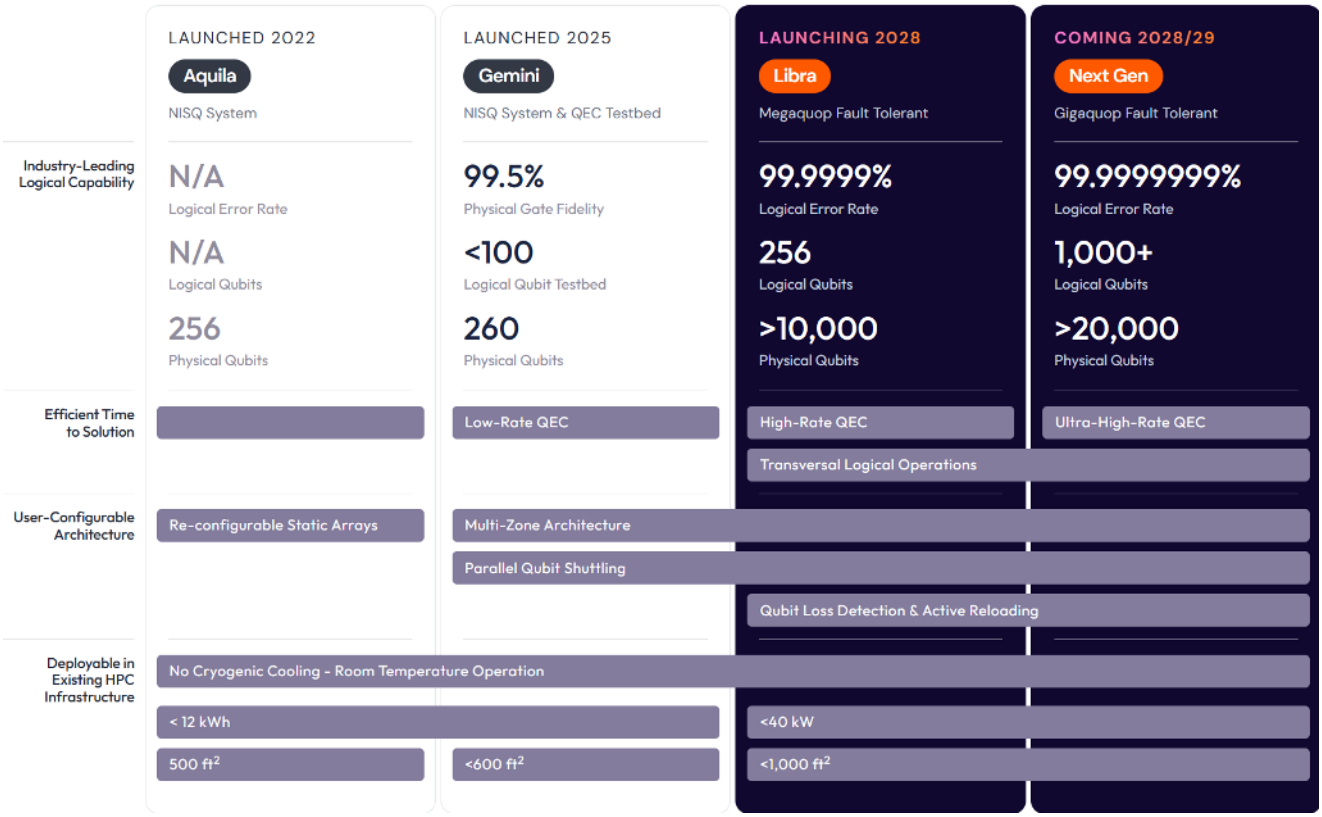

Figure 269: QuEra FTQC roadmap as published in June 2026. It updated the previous roadmap published in 2024 [14]. The difference between the two roadmaps show a delay of about 2 years in the delivery of a 10K atoms system. It was planned in 2026 and is delayed until 2028, although with a larger supported FTQC circuit. Source: [2427].

can reduce space-time cost by more than an order of magnitude in favorable regimes. This is a theoretical and simulation-based result, not an experimentally demonstrated 10–100× speed-up.

Gemini is the name of QuEra gate-based system, introduced late 2025. With 256 atoms, it supports the basic components of QEC and FTQC including magic-state generation and injection, mid-circuit measurement, teleportation-based operations and flexible entanglement routing. It is an experimental platform for researchers.

In June 2026, the company updated its roadmap and announced the Libra system with 256 logical qubits and a megaquop support to be made available on AWS and Amazon Braket in 2028, with a next-generation system coming shortly after with over 1,000 logical qubits and a gigaquop support (Figure 269).

DQC. QuEra is looking at ways to interconnect multiple QPUs for the implementation of future Distributed Quantum Computing networks. They published a paper on this, related to the creation of fault-tolerant Bell pairs distillation with qLDPC codes in 2025 [35] (Figure 270).

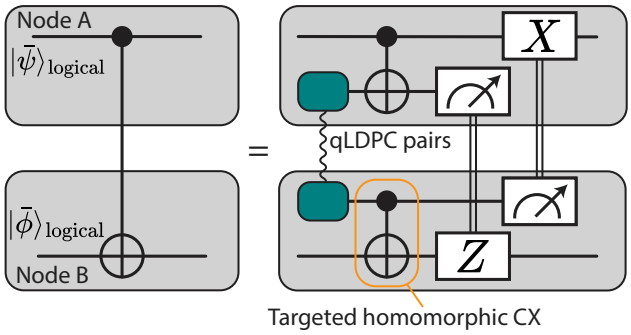

Figure 270: How QuEra would implement a distributed CNOT between two gate-based cold-atoms QPUs using qLDPC-distilled Bell pairs. Source: [35].

Software. QuEra quantum emulation Bloqade software package is available on GitHub as a Julia package since July 2022. It emulates atom-based quantum simulations on classical computers. This is akin to Pulser from Pasqal. They got help for this from AWS and the Perimeter Institute. In 2026, QuEra open-sourced Tsim, a GPU-accelerated quantum circuit simulator simulating non-Clifford gate operations including T-gates at about 600 ns per shot for 85-qubit circuits on NVIDIA GH200 hardware.

In 2025, QuEra and academic partners published models to do resource estimates using their full-stack FTQC architecture to factor RSA 2048-bit key using Shor's algorithm [2436]. It could be done with 19 million physical qubits in 5.6 days assuming a 1 ms QEC cycle times. However, QuEra's current roadmap stops at 10K physical qubits, and various stretch scaling estimates for cold atoms reach between 40K and 100K physical qubits. It means that in the best case scenario, breaking an RSA 2048-bit key would require connecting 190 QPUs with 100K qubits. Photonic based interconnect would have to connect with good fidelities a critical mass of atoms from each QPU and avoid creating significant bottleneck, and some code compiling and optimization overhead would have to be considered.

In August 2026, QuEra and its academic partners presented their ONEX compilation pipeline which is optimized for their high encoding rate error correction codes [2437]. It compared favorably with Enola, a similar compiler created by UCLA in 2024 [2438]. It also provided insights on the compilation cost. With 4,225 data qubits, the total compilation would last 18 hours on a 192-core AMD-based server. This could be somewhat parallelized on a multi-server configuration. But you then need to add the cost of logical gate implementation and magic states generation and teleportation. In September 2026, QuEra researchers presented FT-Weave in a preprint, a stage-aware real-time FTQC compilation framework that handles resource preparation and assignment, atom teleportation routing, and QEC. It supports transversal the STAR architecture (where arbitrary rotations are analog) and a T-state cultivation based-architecture [2439].

Partners. In September 2023, QuEra announced a partnership with KAIST and the Sejong Special Autonomous City in South Korea. It is mostly about putting in place an educational program, international academic exchanges, and work on government projects. QuEra also partners with Wolfram Research to integrate their QPU into the Mathematica software environment. In October 2023, QuEra was awarded with two grants from DARPA as part of the IMPAQT (Imagining Practical Applications for a Quantum Tomorrow) program for "Quantum Reservoir Learning using Neutral Atoms and its Applications" (using MNIST handwritten digit data sets) and "Error-Corrected Quantum Architectures Based on Transversal Logical Gates" (improving QEC overhead with surface code in a FTQC regime). They are partnering here with Moody's, BlueQubit, Polaris Quantum Biotech and the University of Padova. In June 2024, QuEra announced a partnership with QPerfect (France) in order to use their tensor network based emulator MIMIQ to model quantum error correction. In July 2024, QuEra announced that Classiq would support its QPU, seemingly in gate-based mode. In August 2024, the company launched its formal partner program, *aka* the QuEra Quantum Alliance Partner Program with an initial batch of 19 industry vendor partners. In February 2025, it launched a services oriented partnership with Deloitte Tohmatsu Group. In March 2025, QuEra established a technology partnership with NanoQT (Japan) for the development of QPU interconnect. NanoQT develops such a technology that is based on fiber.

Case studies. QuEra and its research partners have published some very theoretical case studies in chemistry and material sciences simulations [2440, 2441], on the study of Ising quantum phase transitions [2442], on neutron scattering simulation [2443], on quantum reservoir learning for handwritten letters recognition using 108 atoms [2444] and credit card default prediction [2445], on graph classification [2446], on preparing ground states of quantum Hamiltonians via adiabatic protocols using quench dynamics (a quantum quench referring to a sudden change in the parameters of a

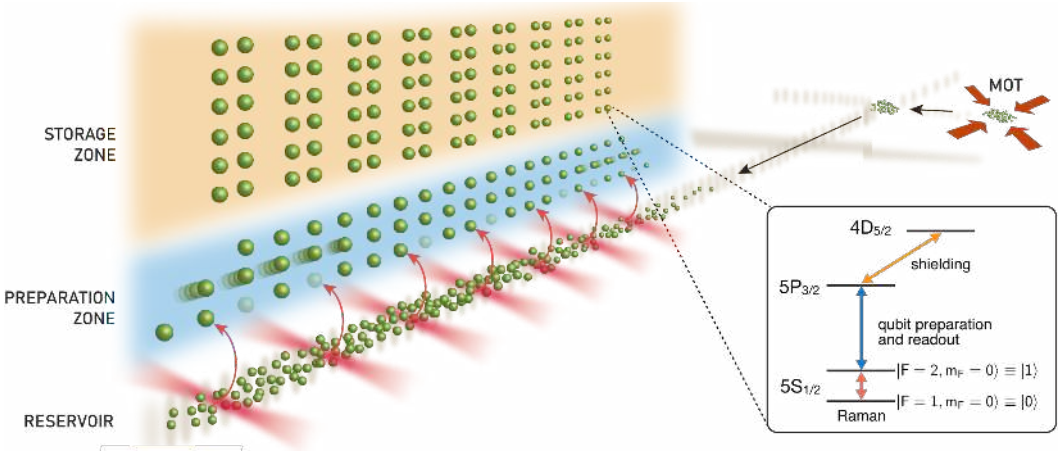

Figure 271: A simple view of how atoms are prepared in a MOT and then put in a preparation zone before landing in the storage zone. Source: [72].

quantum system, altering its Hamiltonian and driving the system out of equilibrium. It can help understanding non-equilibrium quantum physics and thermalization processes [2447]), an Out-of-time-order simulation (OTOC) probing information propagation, scrambling dynamics, and quantum chaos [2448], similar to the one realized by Google with superconducting qubits in 2025, and on adversarial autoencoders to solve some optimization problems [2449]. Most other published papers are about lower level cases related to error handling and compiler optimizations [2417, 2450–2452]. Building on their QND readout and atom reservoir techniques, QuEra/Harvard researchers combined analog Rydberg dynamics with digital hyperfine qubit control to simulate some non-equilibrium quantum spin liquid [2453]. It was heavily based on loss-based postselection, keeping between 55% and 96% of shots depending on the results.

Customers. QuEra partners since 2023 with the DoE **NERSC** (National Energy Research Scientific Computing Center). In 2024, QuEra announced having sold one of its QPU to **AIST** in Japan for $41M [2454]. It was up and running in May 2025, next to the AIST Nvidia-based ABCI-Q supercomputer and be part of a cloud-based platform for remote access to the supercomputer and the QuEra QPU. QuEra also sold one QPU to **NQCC** in the UK [2455]. They also have a partnership with **Pawsey Supercomputing center** in Australia, for accessing remotely their QPU and classical emulator. They are partnering with **Quantum Intelligence Corp** (South Korea) since August 2024, on drug discovery applications. In October 2024, QuEra announced the creation of a Quantum Computing Complex at the Massachusetts Green High Performance Computing Center (MGHPCC) in Holyoke, funded by $11M from QuEra and $5M by the Massachusetts government.

Planqc

Germany, 2022, €54.6M

Company. Planqc is a startup created in Garching near Munich by Alexander Glätzle (CEO, a former researcher at the University of Oxford in the UK), Sebastian Blatt (CTO), a researcher at Ludwig-Maximilians-University Munich (and is a son of Rainer Blatt) and Johannes Zeiher (a researcher at MPQ). The startup had 100 people onboard as of June 2026. Immanuel Bloch and Jose Ignacio Cirac from MPQ and Dieter Jaksch, Professor of Physics at the University of Oxford and the University of Hamburg are their scientific advisors.

Technology. Unlike Pasqal and QuEra, their neutral-atom-based QPU is mainly focused on gate-based computing and FTQC although they could also implement analog simulations. They plan to scale it to thousands of physical qubits. Their Diacqs QPU will host 100 qubits and then, Maqcs with 1,000 qubits in a "multicore" approach using cold atoms multiple zones, meaning 100×10 qubits, parallelizing 100-atoms circuits shots in NISQ fashion. The system total power consumption is of about 10 kW.

The company publishes work on measurement-free fault-tolerant architectures [2456], large atom arrays [2457] and fast Rydberg entangling gates [2458]. Strontium and ytterbium are two-valence-electron atoms, not "two free electron" atoms. Specific isotopes and encodings can provide optical-clock, fine-structure or nuclear-spin qubits and can support erasure detection, but that capability is not automatic for every Sr or Yb encoding.

After preparation in 2D and 3D MOT stages, strontium atoms are transferred to optical traps in a compact vacuum cell. planqc explores microlens arrays and optical lattices/tweezers for parallel trap generation [112]. Rydberg-mediated two-qubit gates act between selected nearby atoms. Gate speed is protocol-dependent, so a blanket statement that two-qubit gates are faster than single-qubit gates and take 1 ms is not appropriate. Cryogenic operation can extend atom trapping lifetime, as demonstrated in recent strontium systems [153].

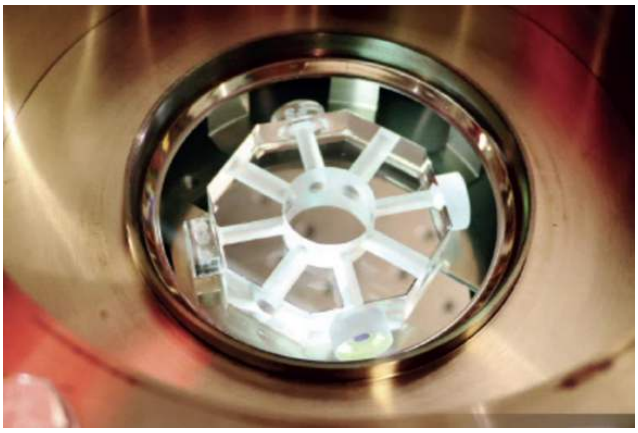

Figure 272: Planqc atom glass cell. Source: Planqc, 2025.

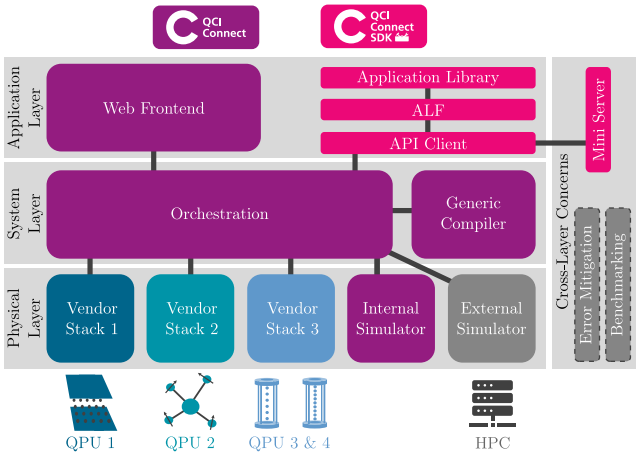

Figure 273: The PlanQc/d-fine QCI Connect platform connects end-users to multiple quantum computing backends. Source: [2459].

Software. In June 2026, Planqc presented along with d-fine (Germany) the project QCI Connect funded by DLR, a modular layered quantum computing platform, with open interfaces and an open-source SDK, with a physical layer, a system layer, and an application layer [2459]. It serves as a multi-hardware vendor quantum computing gateway for end-users (Figure 273).

Customers. In May 2023, DLR (Germany) ordered the DiNAQC 100 qubits gate-based quantum computer as part of a €29 M contract that also involves ParityQC and MenloSystems (laser and frequency combs) [2460]. In November 2023, it was complemented by another contract along with d-fine and MQS to develop simulation of water molecules in the QuantiCoM H2Q project. And in November 2024, Planqc was awarded a $21M contract to create the MACQS 1,000-qubit quantum computer to be installed at the LRZ HPC computing center in Garching near Munich. On the application side, they team up with duisport, TriCon, DB RegioBus, and Rnv on logistics, Engsys for computational fluid dynamics, Airbus, Exomatter and MQS for material simulations, and ESA for image regognition.

Atom Quantum Labs

Slovenia, 2021, €2M

Atom Quantum Labs is developing an atom-based quantum simulator with the stated goal of supporting thousands of atoms. The founders are Marjan Beltram (CEO), Erik Zupanič and Peter Jeglič from the Jožef Stefan Institute [2461], Dušan Babič and Igor Poberaj from Aresis (2004, Slovenia), a small company producing tweezers for biological applications. The company also works with **NKT Photonics** (Denmark, part of Hamamatsu since May 2024).

The company plans to use a hybrid atom-source architecture that use trapped-ion techniques to create and position cold neutral atoms on demand before transfer to optical trapping. The company also seems to work on cold-atom-based RF sensors [2462].

GDQLABS

India, 2022

GDQLABS is building a neutral atom-based quantum computer using 2D array. They are based out of IISER Pune and incubated by I-Hub QTF. They also build cold atom based atomic clocks and gravimeters!

Logiqal

USA, 2025

Logiqal is a startup based in Princeton, New Jersey, created by Jeff Thompson with Sebastian Horvath, Jahan Claes, Elmer Guardado Sanchez and Jared Rovny who are alumni from Princeton, Harvard, Yale, the MIT and Google Quantum.

Technology. They plan to create a scalable QPU supporting millions of qubits using ^{171}Yb or ^{133}Cs. The technology was developed at Princeton, based on using CMOS optoelectronics modules. Among other things, they developed a replacement technique for missing cold atoms [2435] and they seem to use ytterbium atoms (^{171}Yb). One researcher from the company also proposed a way to implement magic state cultivation efficiently with cold atoms using surface codes instead of color codes as proposed by Craig Gidney from Google [2463]. Recent work by Jeff Thompson, which are not mentioning Logiqal, cover atom replenishment [2464], Rydberg state life extension thanks to using 4K cryogenics [163] with a grid of 7×7 atoms, and a two-qubit CZ gate with 99.59% fidelity [2465].

YaQumo

Japan, 2025

YaQumo is a startup created by Kazuhiro Nakashoji, Yuma Nakamura and Takafumi Tomita and linked to the Kyoto University and IMS neutral-atom programs. Its technical direction includes dual-isotope ytterbium arrays, with ^{171}Yb for computation and ^{174}Yb for auxiliary functions [2466]. The cited 6.5-ns result [2288] is ultrafast coherent Rydberg energy exchange, not by itself a benchmarked universal two-qubit gate. The group is also investigating fast readout and high-spin cat-like encodings [2467, 2468].

MatriQ

China, 2025

MatriQ (*aka* Atomic Matrix or Hangzhou Atomic Matrix Computing Co) is a stealth startup that spun out of USTC and is developing cold atom quantum computers. In early 2026, they reportedly achieved the trapping and sorting of an array of 2,048 physical qubits.

CAS Cold Atom Technology

China, 2020, $14M

The company is a spinout of the Chinese Academy of Sciences' Innovation Academy for Precision Measurement Science and Technology in Wuhan, created by Tang Biao (Chairman). The scientific roots are from the cold-atom group of Mingsheng Zhan and Xiaodong He.

The company built the Hanyuan-1 with 100 qubits and released June 2024, with the first commercial deployment in October 2025 to Pakistan and to China Mobile, and the "dual-core" Hanyuan-2 with 200 qubits, announced in May 2026, plus a quantum computing cloud platform for algorithm development. For the Hanyuan-2, they demonstrated defect-free assembly of mixed-species atom arrays using ^{85}Rb and ^{87}Rb isotopes where one array does computing while the other stores is used for error correction [2469]. Dual-core means that the systems contains two processors with 100 physical qubits each. The Hanyuan-2 consumes 7 kW. They claim to obtain 99.9% single qubit gate fidelities, which probably means it is the highest fidelity, and not the average. They sell customized version with between 200 and 500 atoms (Figure 274). They are also investing the field of quantum error correction with cold atoms with an eye on the cost of error syndrome decoders [2470].

They also create and sell quantum sensors like absolute quantum gravimeters, gravity gradiometers, atom-interferometry instruments like ultra-vacuum cavities and compact MOTs, lasers, AOM drivers, pulse-delay generators, and mechanical shutters.

Taiyi Quantum

China, 2026, $72M

Taiyi Quantum *aka* Taiyi Liangsheng is building a quantum computer based on ytterbium-171, created by Fang Zhenghao (CEO) and Hongbin Liu (CTO, formerly from Microsoft), and based in Shanghai where it has a 1,000 m^2 cleanroom. The company aims to assemble 50,000 physical qubits supporting about 300 logical qubits. ^{171}Yb offers long-lived nuclear-spin qubits and access to telecom-band optical transitions. Atom-photon entanglement at telecom wavelengths has been demonstrated experimentally with ^{171}Yb arrays [2471]. Rydberg-mediated multiqubit operations in ytterbium remain an active research direction.

Oratomic

USA, 2026, $300M

Oratomic was created by Dolev Bluvstein (CEO), Robert Huang and John Preskill [2472]. Dolev Bluvstein is the first author of several Harvard/Mikhail Lukin and QuEra papers on neutral-atom logical processing and FTQC between 2022 and 2025 [69, 2242, 2422]. He was a visiting associate in physics at Caltech. Other company founders came from Manuel Endres's Caltech team, which in 2025 reported more than 6,100 ^{133}Cs atomic qubits [2162].

In July 2026, they raised $300M in a Series A round. You find Infleqtion among their investors. That's interesting to say the least.

The company got the attention with an FTQC architecture paper making new resource estimates for breaking RSA-2048 and ECC keys with a rather small number of atoms, down to 10K, but with very long computing times [2473]. And then, with a preprint describing a method for loading data more efficiently for quantum machine learning applications [2474].

In August 2026, they published a paper describing a new QEC and FTQC architecture constructed around the high encoding rate *mitten codes*, a variant of qLDPC [2475]. The key figures of merit in this paper are a $[\![300, 60, 14]\!]$ code with a block logical error rate of $\sim 10^{-11}$ per round and the $[\![975, 195, \leq 24]\!]$ with a $\sim 10^{-8}$ error rate, with a physical error rate of respectively 0.1% and 0.4%, this last one being reasonable. They estimate that this architecture would support $\sim 10^{10}$ logical operations, fueled by an error syndrome decoder with sub-millisecond average latency per logical cycle. They designed their QEC pipeline with sQetch, a GPU-powered distance estimator machine learning based toolkit. The paper mentioned cold atoms and superconducting implementations, as if they were working for Google! The cold atom implementation would need fast squeezers, which could be implemented with fast SLMs operating in the MHz scale. Also in August 2026, they proposed a new protocol to run more robust two-qubit gates [2476].

In April 2026, the startup established a partnership with Monarch Quantum for the development and sales of their upcoming FTQC system. Monarch Quantum is a company also created in 2026. They will provide advanced photonics-based control systems to Oratomic.

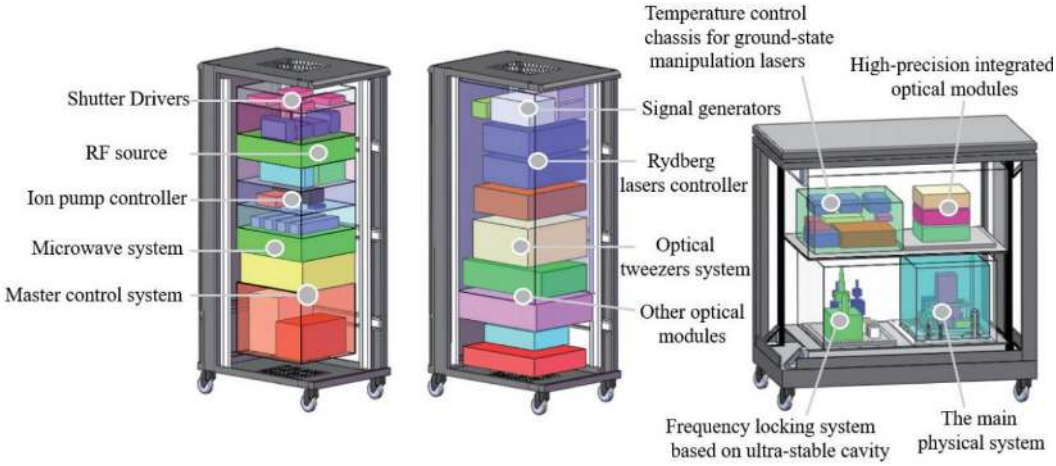

Figure 274: The internal packaging of the Hanyuan-1 from CAS Cold Atom. Source: CAS Cold Atom website as of July 2026.

Together, they plan to support thousands of logical qubits by 2030.

Google

USA, 1998

Google announced a neutral-atom quantum-computing research effort in March 2026 [2477] and recruited Adam M. Kaufman from JILA. A key JILA result cited here is a cryogenic ^{87}Rb tweezer array with a 3,000-s atom-trap lifetime [2195]. It is not a demonstration of controlling 3,000 atoms in a 4 K chamber.

Google's 2026 neutral-atom effort is evidence of a broadened hardware research portfolio, not evidence by itself that the company has lost confidence in superconducting qubits. The public announcement supports only the narrower conclusion that Google considers neutral-atom scalability and control sufficiently promising to justify a dedicated research effort.

Q-Factor

Israel, 2025

Q-Factor's existence was unveiled in April 2026 with their funding round of $24M with Intel Capital and Korea Investment Partners as investors.

Based in Tel Aviv, the company was created by four physicists from the Weizmann Institute and the Technion, Nir Davidson, Ofer Firstenberg, Yoav Sagi and Guy Raz. They ambition to create a cold-atom quantum computer supporting a million physical qubits.

Based on the published work [2478–2485], some technology choices can be inferred. The papers point to optical-tweezer transfer, Rydberg-mediated gates, zoned architectures and scalable readout concepts, but vendor implementation details are undisclosed.

Key neutral-atom quantum computing reviews

Here is a selection of neutral-atom scientific reviews to dig into the concepts presented in this section:

Quantum information with Rydberg atoms by Saffman *et al.*, August 2010 (51 pages): the founding review, Rydberg blockade, gate protocols and their error budgets, atom trapping and the ensemble versus single-atom encodings [2138].

Strategic Plan for Neutral Atom Quantum Computation by Menssen *et al.*, July 2026 (135 pages): what practical quantum advantage would mean and how to verify a claim of it, hardware directions to get there, system scaling, qubit encodings and atomic species, going below threshold, continuous reloading, fast readout, integrated photonic control, error correction, compilation and processor networking [2197].

Neutral atom quantum computing by Saffman, August 2026 (39 pages): pedagogical survey of the physics, current capabilities including logical qubits and fault tolerance, and an outlook [2199].

Many-Body Physics with Individually-Controlled Rydberg Atoms by Browaeys and Lahaye, February 2020 (11 pages): the analog side, tweezer array assembly, Ising and XY spin models, and what programmable arrays reveal about quantum magnetism [2176].

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This **Cold atoms qubits** subsection contains 384 bibliographical references and notes containing at least 6,041 pages.

1.9 NMR qubits

1.9.1 History and science

Nuclear magnetic resonance was an early technique investigated to create quantum computers [2486]. Qubit states are the spin of nuclei within large ensembles of up to 10^{15} molecules. The qubit states are readout using nuclear magnetic resonances, implementing a variant of nuclear magnetic resonance spectroscopy. The NMR phenomenon was discovered in 1945 by **Edward Mills Purcell** (1912-1997, American) for which he was awarded the Nobel prize in physics in 1952, shared with Felix Bloch. Using nuclear spins for quantum computing was first proposed in 1993 by **Seth Lloyd** from the MIT [2487] and refined in 1994 by **David DiVincenzo**, then at IBM Research, for the implementation of perfluorobutadienyl two-qubit gates [2488] [2489].

It was perfected by various proposals coming from the MIT, UCSB and Stanford researchers in 1997 with a computing method using liquid state NMR (molecules in a liquid) and enabling the measurement of the expectation value of quantum observables, ensuring an exponential computing speedup [2490]. An expectation value of an observable is the average value of the observable and not a random value obtained by a projective measurement, the type of qubit readout measurement usually implemented with other techniques. Using another explanation, this measures a statistical mixture of pure states.

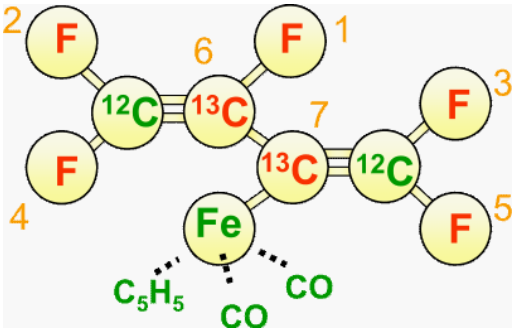

Figure 275: NMR can rely on complex molecules like perfluorobutadienyl. Source: IBM.

In 2001, **IBM** researchers even implemented Shor's algorithm with the number 15 on a 7-qubit NMR quantum processor using a perfluorobutadienyl iron complex where the spins come from the nuclear spins of fluor and carbon atoms (in red in Figure 275 [2491]. It is still the record to date! In these systems, qubit states where the ensemble nuclear spins ½ in a magnetic field, quantum gates were operated by radiofrequency pulses and qubit readout was done with detecting spin states with a radiofrequency coil [2492, 2493].

Afterwards, there were some developments with "Solid state NMR" (SSNMR) using nitrogen vacancies and interactions between carbon atomic spins and vacancies electron spins or nuclear spins of ^{29}Si in silicon structures [2494]. NMR was a prominent experimental platform in early quantum computing, particularly in the late 1990s and early 2000s. Liquid-state NMR generally relies on ensemble measurements and pseudo-pure-state preparation, so the effective qubit count reported in these experiments is not equivalent to a number of individually addressable and scalable physical qubits. IBM was even planning for the existence of NMR-based tabletop quantum computers [2495]. 22 years ahead, their (superconducting qubits) quantum computers are 3-meter wide cubes consuming in excess of 25 kW.

Still, research is still ongoing on NMR quantum computing. It goes on in Europe in the Europe 2020 project **FATMOLS** run by a research consortium led by Spain. Its ambition is to create a molecular spin quantum processor using artificial magnetic molecules implementing spin qudits controlled, read-out and linked with some superconducting circuits.

Quantum features are implemented with nuclear spins, electronic spins and circuits. Programming models range from quantum simulations to gate-based FTQC. The FATMOLS project's goals is to create a proof-of-concept of one of the repetition unit cells of this platform with at least two molecules with multiple and fully addressable levels and related algorithms. The end-goal is to reach 100 to 1,000 physical qubits [2496].

The project runs from March 2020 to August 2023 with a total cost of €3.2M, entirely funded by the EU.

1.9.2 Research

Various NMR variants are still investigated like the use of large molecular spins [2497, 2498], europium molecules with nuclear spins that can interact with luminescent photons carrying the nuclear spin information [2499], water protons [2500], with molecular ensembles [2501] and optically addressable molecular spins [2502].

DQC1 (Deterministic Quantum Computation with 1 quantum bit) is a curious quantum computing model created in1998 by Emanuel Knill and Raymond Laflamme (Figure 276). It was designed for NMR qubits which we were commonly developed in the late 1990s and were very noisy. It is described as a deterministic quantum computation using one qubit and a classical computer [2503]. It computes deterministic functions on one bit and a classical computer is performing probabilistic computing.

But there's more than one qubit in the story: the input is indeed constrained to a single qubit in a pure state, but a set of n other qubits is prepared in an identity state and subject to a random unitary transformation U_n and in a completely mixed state. These systems use noise as a resource which is formalized with **quantum discord** mathematical tools [2504, 2505].

At the end of the circuit execution, a measurement takes place on the first qubit. It is not a universal quantum computing model, doesn't use massive entanglement and

has a narrow set of use cases although it is supposed to bring some exponential speedups in some circumstances [2506].

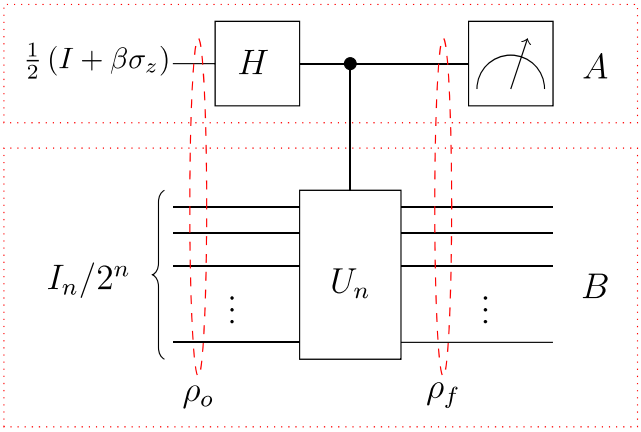

Figure 276: Description of the DQC1 model. A qubit at the top is the only input. It is prepared then subject to an Hadamard gate and the result controls the application of the U_n unitary transformation to n other qubits. At the end of this processing, the first qubit is the only one measured, with the process being repeated several times. The output yields a trace of the unitary U_n. Source: [2507].

1.9.3 Vendors

NMR quantum computers don't scale well due to noise affecting qubits and poor entanglement. It did not prevent one company from China to manufacture and sell and NMR-based quantum computer. And fulfilling IBM's 2000 dream, it is a desktop product.

SpinQ

China, Year2018, $252.3M

SpinQ is creating NMS and superconducting qubit QPU for the educational and research markets [2508]. They started with announcing in January 2021 their Gemini $5K 2-qubit desktop quantum computer and their cloud quantum computing platform Taurus [2509].

It followed an initial version launched in 2020 and sold at $55K. The quantum computer weighed 55 kg and works at ambient temperature. They planned to increase the number of qubits of this device in upcoming versions, up to a maximum of 15 qubits. It would be nice since 2 qubits are totally useless even for quantum programming learning tasks. Meanwhile, you can test *for free* 127 real superconducting qubits on IBM Quantum Experience cloud systems. In August 2024, SpinQ announced Gemini Lab, a new 2-qubit NMR QPU targeting the education and research markets in Europe and North America (Figure 277).

The SpinQ computers use liquid dimethyl-phosphite molecules with two OCH_3 groups associated with a phosphorus atom plus one oxygen and one hydrogen atom. These molecules are controlled with permanent magnets and an RF pulse generation system. They followed-on with the Gemini mini version (also with two qubits) and the Triangulum (with a hefty three qubits). The computer is used for educational purposes [2510].

Figure 277: SpinQ Gemini Lab introduced in August 2024. Source: SpinQ.

Bei Zeng from the USTC in Hong Kong is the chief scientific advisor to the company which is based in Shanghai. In 2026, they published a preprint on using their system for solving some TSP problem. With 2 qubits, they won't travel for long [2511]!

1.9.4 Bibliography and notes

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This **NMR qubits** subsection contains 26 bibliographical references and notes containing at least 596 pages.

1.10 Photon qubits

Unlike the previously discussed qubit modalities, photons have no mass and move at about the speed of light, modulo the optical refractive index of the physical media they pass through. While photons are used everywhere in solid qubits in control and readout features with microwaves or laser beams, they can be used to create qubits exploiting polarization or other physical characteristics such as frequency, amplitude, phase, mode, path, or photon number. These are called "degrees of freedom" (DOF). They can even be combined to enrich the information supported by single photons.

This is the vast field of linear and nonlinear optics [2512]. It is found in both the generation of qubits for quantum computation or simulation and with their application in telecommunications and quantum cryptography which we study in another part of this book.

Photonics is both an interesting solution for creating qubits as well as a transversal technology that is indispensable to other types of qubits because it is the only one that allows long-distance communications between quantum sensors, quantum networks and quantum computers. Photons are also used directly in quantum sensing, particularly for precision time measurement and even for pressure measurement.

The advantages of photonics are that it supports quite stable qubits with a very low error rate at the quantum gate level thanks to their weak coupling with the environment. The main source of decoherence is related to the optical losses happening with photons propagation.

Photons also operate at any temperature, do not require expensive nanoscopic manufacturing techniques and can be based on nanophotonic CMOS manufacturing processes [101, 2513]. In general, solid-state single photon light sources must be cooled down to 4K to 10K and the photon detectors to about 2K to 4K. At least, one avoids going below 1K, which allows the use of cryogenic systems that are satisfied with helium 4 and do not require helium 3. These cryogenic systems are miniaturizable and require much less energy than the dilution systems used for superconducting and silicon qubits.

Their disadvantage lies in the fact that photons are even more probabilistic beasts than any of the other qubits. You trade fidelity issues vs loss issues. Scalability issues make it difficult to assemble more than a few dozens of qubits, at least for the moment. Photon sources must be more powerful to accommodate a larger number of entangled qubits (Figure 279).

Current technology developments are based on advances made with more efficient single photon sources, better photon detectors, nonlinear optics, advanced quantum states preparation (multimode, spatial or spectral multiplexing, non-Gaussian states) with a larger computing space than traditional two-states qubits, using cluster-states measurement-based techniques (MBQC) to work around the limitations imposed by finite quantum-gate depth and the overhead of quantum error correction.

1.10.1 History

The roots of quantum photonics date back from 1963 with the introduction of Glauber states by Roy J. Glauber which created the notion of coherent states of light explained by the quantization of the electromagnetic field. This corresponded to the beginnings of the laser era which led, among many things, to its broad industry impact, including fiber optics in the telecom realm.

While the first physical qubits were experimented in the mid-1990s (trapped ions, NMR) and in 1999 (the first superconducting charge qubit), photon qubits used for computation saw the light much later. Starting in the mid-1980s, quantum photonics was envisioned for implementing quantum key distribution protocols. 2001 was a foundational year with the creation of the dual-rail KLM scheme by Emanuel Knill and Raymond Laflamme (then at the Los Alamos National Lab) and Gerald Milburn (University of Queensland, Australia) [2514]. Its operations are well described in [2515].

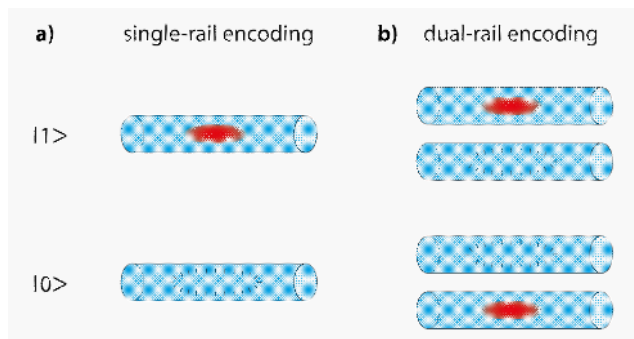


Figure 278: How dual rail encoding works in the KLM model. Source: [2516].

This model could theoretically implement quantum computing without relying on some sort of nonlinearity for creating entangling quantum gates [2526]. Implementing for example a CNOT gate with photons is not easy since photons do not easily interact with each other.

The KLM model made it possible to implement two-qubit gates using photon sources, beam splitters and photon detectors, using a dual rail encoding, represented by the presence of a single photon in one of two spatial optical modes [2516] (Figure 278).

It circumvented the need for nonlinear interactions between photons with the use of post-selection using ancilla photons, many executions and iterations being required [2527]. It creates significant overhead which makes the model impractical. It does not scale well and can't bring a quantum advantage [57, 2528].

There were then many "firsts" with the first universal optical quantum computer in 2015 using a chip handling

photon qubits key takeaways

highlights

- **stable qubits** with very low gate error rates and near-absence of decoherence thanks to weak coupling to the environment, the dominant loss channel being optical losses [101].
- **ambient-temperature processing**, only photon sources and detectors needing cooling, although not true in practice [2513].
- **emerging nanophotonic manufacturing** techniques leveraging CMOS foundries and enabling scalability [52, 53].
- **easy scale-out** through inter-qubit communication and quantum telecommunications, photons being natural flying qubits.
- **MBQC/FBQC** circumventing the NISQ gate-depth limit and the difficulty of building deterministic multi-qubit photonic gates [55, 100].
- **circuit clock rate** which could be a source of speed advantage vs other quantum computing technologies once full-stack comparisons can be made.
- **boson-sampling advantage** becoming programmable, though practical quantum advantage remains to be demonstrated [2517, 2518].

challenges

- photon sources and detectors must be cooled, but at relatively mild temperatures between 2K and 10K that allow lightweight helium-4 cryogenics, unless the whole photonic circuit is also cooled [166, 167].
- not yet scalable in the number of operations, because of the probabilistic nature of the gates and the limited efficiency of photon sources in most paradigms [57].
- cluster-state generation and two-photon interactions are non-deterministic [55].
- delay lines and optical switches are required, in particular to synchronize resource states [103].
- phase shifters generate heat that increases the cooling budget [111].
- photon-detector efficiency is still too low, at about 89% for PsiQuantum [53].
- photon losses must be contained within the nanophotonic circuits [51, 52].

variations

- **encoding**: discrete-variable (DV), continuous-variable (CV) and multimode photon encodings [2519, 2520].
- **MBQC and FBQC**, measurement-based and fusion-based quantum computing [55, 100].
- **BS/GBS**: programmable Boson Sampling and Gaussian Boson Sampling [2517, 2521].
- **hybrid approaches**: spin-optical quantum computing (SPOQC) with quantum-dot spin qubits (Quandela) and hybrid atom-photon qubits [2522].
- **classical photonic models**: coherent Ising machines, photonic waveguide arrays and interferometric systems [2523–2525].

path to scalability

- **efficiency**: raise photon-source efficiency, determinism and indistinguishability, and improve detector efficiency (SNSPD and PNRD) [54, 98].
- **cluster states**: generate large cluster states, with or without heralding [56, 99].
- **interactions**: improve fusion efficiency in FBQC [55, 102].
- **losses**: large-scale, low-loss optical switches and waveguides, and lower nanophotonic-circuit losses through higher-precision manufacturing and new materials [52].
- **energy**: develop low-heating phase shifters to minimize power consumption [111].
- **nanophotonics**: heterogeneous nanophotonic circuits combining III-V and silicon [52, 101].
- **classical control speed**, particularly demanding for FBQC models [104].

Figure 279: Highlights, challenges, variations and path to scalability of photon qubits. 🅭 Olivier Ezratty, 2022-2026.

6 photons with 15 Mach-Zehnder interferometers and 30 thermo-optic phase shifters and a 12-single-photon detector system [2529], a programmable photonic quantum computer created by Xanadu in 2021 with 8 photons [2518] and a first quantum computational advantage using gaussian boson sampling in China [2517]. Boson sampling was based on an idea from Scott Aaronson and Alex Arkhipov elaborated in 2010 [2521]. It led in 2022 to a similar experiment achieved by Xanadu with a programmable gaussian boson sampler.

Many fundamental research advances were also achieved:

- **MBQC** was created in 2000 by Robert Raussendorf and Hans Briegel. It circumvented some limitations of photon qubits beyond the nonlinearity already discussed, like the finite number of gates that could be executed, the photons being "flying qubits". We'll describe this in a dedicated subsection. The key figure of merit of this architecture is the ability to create large cluster states of entangled photons.
- **FBQC**, for fusion based quantum computing, is a variation of MBQC adopted among others by PsiQuantum. It is kind of a mix of KLM and MBQC. Cluster states are small (4 qubits in the case of PsiQuantum) and they are connected with each other with fusion gates which are sort of probabilistic 2-qubit gates like in the KLM model.
- **Quality photon sources**, like single and deterministic photon sources, and better, entangled photon sources. Two entangled photons can be created with a photon source and a polarizing crystal. More entangled photons can be created with a single deterministic indistinguishable photon sources and delay lines.
- **Silicon or III-V-based** Quantum Photonic Integrated Circuits (QPICs) that implement quantum gates with waveguides and electronically controllable optical elements like beam splitters and polarizing filters as well as photon sources and photons detectors. They enable miniaturization of these components.

Their figures of merit are miniaturization and low photon losses [52].

Then, since about 2017, a wealth of startups have been created that are all pursuing the goal of creating photon qubits quantum computers, first in the NISQ and then the FTQC realms: **PsiQuantum**, **Xanadu**, **Quandela**, **Orca Computing**, **QuiX**, etc. They all adopt very diverse technological choices as we will see in the vendor section.

1.10.2 Science

To understand photons in quantum information systems, one needs to get a bit deeper in quantum optics and statistical optics. You can look at the related subsection in the Quantum Physics 101 section from this book, which will help you understand some of the vocabulary used in photon-based quantum computing. It can also help us segment the various kinds of photonic qubits like discrete variables and continuous variables qubits.

We now look at the sheer diversity of quantum computing paradigms using photons. Photons are "flying qubits". They are the only ones having this characteristic with flying electrons, which are investigated at the fundamental research level.

There are two main classes of photon qubits: discrete variable and continuous variable qubits [2519, 2530, 2531] (Figure 280).

- **Discrete Variable** qubits use single photons and use a two-dimensional space like orthogonal polarizations, the absence and presence of single photons or even time-bin encoding, where information is encoded in the time of arrival of photons, with a superposition of a photon arriving in one of two distinct time bins, referred to as the "early" bin and the "late" bin [2532, 2533].

  DV systems can even be based on qudits using more than one degree of liberty [2534, 2535]. DV qubits rely on highly efficient, deterministic, and indistinguishable single photon sources. They are using the "particle" side of photons.

  Their indistinguishability must exceed 95%, meaning this percentage of photons must be indistinguishable. The photon sources must also be efficiently connected to dynamically controllable photonic computing chips. Efforts are also undertaken to create cluster states of entangled photons used in MBQC and to create multi-qubit gates using spin-photon interactions like in NV centers or other silicon spin defects [2536].

- **Continuous Variable** qubits encode information in the fluctuations of the electromagnetic field, in their quadrature components, in qubits that are sometimes baptized qumodes [2537]. We are playing here with the wave nature of photons.

With CV photons qubits, readout can be done with a Gaussian measurement comprising homodyne detection for one of the two quadrature components and heterodyne detection on one of these [2538], and a non-Gaussian measurement implementing photon counting returning an integer. There, you hear about Wigner function amplitude, phase encoding, Gaussian states [2539], including squeezed states generated with nonlinear media and non-Gaussian gates to execute non-Clifford group gates bringing a real exponential speedup for quantum computing. Quantum gates can be deterministic, homodyne detectors are cheaper than single-photon detectors, and quantum states are more robust.

CV qubits require the ability to generate single-mode squeezed-vacuum (SMSV) states with squeezing levels expressed in dB. It is critical for FTQC architectures like those using GKP codes, which require a minimum squeezing level of 10 dB, and at 1546 nm, right in the C-telecom band. In 2026, Christine Silberhorn's team at Paderborn University (Germany) demonstrated an efficient and bright single-mode SMSV source whose modeling predicts squeezing levels approaching 20 dB [2540]. This is a simulated figure obtained under idealized assumptions that do not yet account for loss and high-gain operation. It can't be interpreted as a measured value. The experimental record for directly detected squeezing remains 15 dB, obtained at 1064 nm in 2016 [2541].

All these optical components can be embedded in photonic integrated circuits (PICs), which is route chosen by all commercial vendors [2542, 2543].

CV qubits enable larger cluster states for MBQC, using a large number of photon modes, in the thousands [2520]. CV qubits can also be implemented with cat-qubits and GKP states [2544–2549], including hybrid DV/CV qubits approaches [2550–2554] and for MBQC architectures [2555, 2556]. CV computing can be used with universal gates quantum computing as well as with quantum simulations. Finally, CV qubits are also proposed to implement quantum Boltzmann machines (QBM) to solve specific machine learning computational problems [2557].

PhotoQ (Denmark) is a collaborative project implementing CV architecture using surface codes for fault-tolerance [2520, 2558]. The project is built around research from DTU with participating organizations being AMCS Group, Aarhus University, Kvantify and NKT Photonics (lasers, part of Hamamatsu since May 2024) with a public funding of €3M from Innovation Fund Denmark. They are focused on solving logistics and pharmaceutical industries problems.

PANDA consortium is another European CV photonic quantum computing project, funded by the EIC Pathfinder-2023 challenge grant. The project led by Sorbonne Université (Nicolas Treps and Valentina Parigi, LKB) also gathers Pixel Photonics (photonic

	discrete variables	continous variables	boson sampling
quantum information	**discrete degree of freedom of a photon** Fock states: $\|0\rangle, \|1\rangle, \|2\rangle$ ... single or many photon properties	**quadrature of a light field** coherent states, qumodes, spectral and time modes	**multimode photons**
photon sources	**single indistinguishable photon sources or heralded photon sources**	**entangled photons sources** **squeezed states, heralded photon sources**	**unique photons source**
representation	**density matrix**	**Wigner function**	**permanent**
gates	**KLM model, MZI (Mach-Zehnder Interferometer) gates**	**determinist gates** modes measurement gaussian and non gaussian gates	**MZI and interferometer**
photon detectors	**photon counters /detectors** APD, SNSPD, VLPC, TES	**homodyne and heterodyne detectors**	**single photons detectors**
computing architecture	**gate-model** **variational circuits** **optical neural networks** **measurement based (MBQC, FBQC)**	**gate-model** **measurement based (MBQC, FBQC)**	**programmable boson sampling**
main industry vendors	PsiQuantum QUANDELA, QuiX Quantum aegiq, OptiQC	ORCA Computing, XANADU Qluster	XANADU QUANDELA

Figure 280: Comparison of the main models of photon-based quantum computing. Olivier Ezratty, 2021-September 2026.

detectors), ICFO (Spain), IOGS (Paris) and Pasqal (France).

Beyond the DV/CV split, and the KLM and MBQC/FBQC paradigms already mentioned, there are several other variations of photon qubit platforms.

- **Quantum Walks based simulation** where you have two classes of systems: discrete-time quantum walks with discrete steps evolutions [2559] and continuous-time quantum walks with a continuous evolution of a Hamiltonian coupling different sites [2560]. A research team in China created a CV-quantum walk system handling a Hilbert space of dimension 400. It even takes the form of a seemingly packaged and designed product despite coming out of a public research lab and not a startup. There are even hybrid fermion/bosons approaches that are proposed but that are very theoretical and with very few hardware implementation details [2561, 2562].

Figure 281: The continuous-variable quantum walk system YH QUANTA QW2020 from China. Source: [2563].

- **Boson sampling** is a separate technique we will cover later in a dedicated subsection. It is a research field that is starting to bring to life programmable quantum computing with some interesting results coming mostly from China.

- **Coherent Ising Machines** is a technique based on using optical neural networks that can solve combinatorial optimization problems by mapping them onto NP-hard Ising problems [2564]. Ising models can solve many problems: planning and scheduling, financial portfolio optimizations, graph problems and even material and molecular design. These problems are defined by couplings between a set of spins. The solution is the spin orientation that minimizes the energy function of the system. CIM systems use single-mode photon squeezing, oscillation at degenerate frequency, Optical Parametric Amplifiers in a Cavity (OPO) and a measurement feedback technique (Figure 283). Leveraging delay lines, time division multiplexing and measurement feedback, CIM can implement many-to-many connectivity. The largest CIM system was built in Japan in 2021 with 100,000 spins [2523]. It competed with quantum annealing (from D-Wave) and classical CMOS-based annealing (from Fujitsu).

A bit like the difference we discovered between (D-Wave) quantum annealing solving Ising "Z" problems [226, 2565–2569] and quantum simulation models implementing XY qubits connectivity, there are also photonic based coherent XY models that compete with CIM [2570].

In 2025, a benchmark was done by US and Canadian academics that compared the efficiency of a CIM model vs gate-based DAQC and a Grover-based search to solve a MaxCut combinatorial problem [2571]. It seems that the time to solution (TTS) is better with CIM, although the gate-based solutions could not be tested on problems as large as those handled by the CIM, which weakens the comparison. It also seems that CIM's computational advantage is mitigated by the cost of data conversion [2572].

- **Interferometric systems**. Let's also mention a theoretical proposal of a Hong-Ou-Mandel interferometric setup to be used for images classification with single photon states encoding, providing a potential superexponential advantage in comparison to classical neuron network [2525].

- **Photonic waveguide arrays** which could be electro-optically programmable and solve various Hamiltonian continuous-time evolutions [2524], quantum machine learning problems, or quantum walks [2573]. They could potentially execute arbitrary unitary transformations [2574].

- **Hybrid atoms-photons qubits**. Stanford University researchers devised a new hybrid quantum photonic approach using a single atom that modifies photons states via quantum teleportation and implement quantum gates and qubit readout [2575]. It reduces the need for multiple photon emitters and greatly simplifies the hardware setting that makes use of a photons storage ring made of a fiber loop, optical switches in the loop, a beam splitter, a phase shifter, a photon scattering unit and a cavity containing a single atom controlled by a laser, the atom getting entangled with the photon (Figure 282).

  The photon source is a single photon train source. But this is not a perfect solution. It has some requirements on the cavity quality, on low fiber attenuation, on very low insertion losses optical switches and can't implement quantum gates in parallel.

1.10.3 Qubit operations

The general principle of quantum computing systems using photon qubits is as follows:

Quantum states are based on a single or several degrees of freedom (DOF), or physical properties, of the photons. The most common is their polarization with a computational basis based on horizontal and vertical polarization. Other parameters of photons are also explored to create qubits. It can be their phase, amplitude, frequency [2576], path, photon number (*aka* Fock states) and spin orbital momentum. It can even be their orbital angular momentum. This multiplicity of parameters also makes it possible to encode not only qubits but also qudits, with a greater number of states. But it is quite complex to manage and, if only to manage two-qubit quantum gates, we are happy with qubits instead of using qudits [2577, 2578]. This potentially allows the creation of qutrits or qudits managing more than two exclusive values.

Photons are "flying qubits" because they move in space and are not static or quasi-static at the macroscopic scale unlike most other types of qubits. The other qubits are "non-flying": spin-controlled electrons trapped in a cavity, cold atoms (which are stabilized in space) and trapped ions (which can move, but in a limited space), NV centers (cavities do not move) and superconducting circuits (which are fixed in space even if they use pairs of circulating Cooper electrons). One such implementation was achieved in 2022 by a China-international team using ququarts states, which are quantum objects with four dimensions instead of the two dimensions of qubits [2579]. The experiment shown below in Figure 285 was implemented in a programmable silicon CMOS photonic integrated chip of 15 x 1.5 mm implementing linear optics and enhancing parallelism. It was tested with a QFT, Deutsch-Jozsa and Bernstein-Vazirani, quaternary phase estimation and factorization algorithms.

The system creates four-level entangled state in an array of four integrated identical SFWM (spontaneous four-wave mixing) sources. The photons then traverse wavelength-division multiplexing filters (WDM), Mach-Zehnder interferometers (MZI). thermal-optic phase shifters (TOPSs), multimode interferometer beamsplitters (MMI) and qudit states measurement. In 2024, a team on China demonstrated photon qudits using 4 dimensions with orbital angular momentum encoding [2580].

Photon sources use lasers associated with single and indistinguishable photon generators [2581]. They are critical to generate simultaneously a large number of indistinguishable photons that will feed in parallel several photonic waveguides, thanks to delay lines. These are well time-isolated, unique and indistinguishable photons and well-spaced in time series. These single photons are individually detectable at the end of processing with single or multiple photon detectors (when computing Fock states with additions of single identical photons).

The key figures of merit of these photon sources are photon indistinguishability (they must all have the same quantum properties), the source brightness (how many photons are emitted per unit time), the system efficiency (probability that at least one photon is created per pulse), single photon purity (probability of getting a maximum of one photon per pulse), photon rate (rate of photon generation) and antibunching (measured with the second-order coherence $g^2(0)$ value, which corresponds to the probability of emitting two photons simultaneously, ideally at zero). Other operational aspects include stability and coherence time (consistency of source over time), spectral properties and tunability (ability to control the emitted photons wavelength) and temperature of operations (usually at 4K).

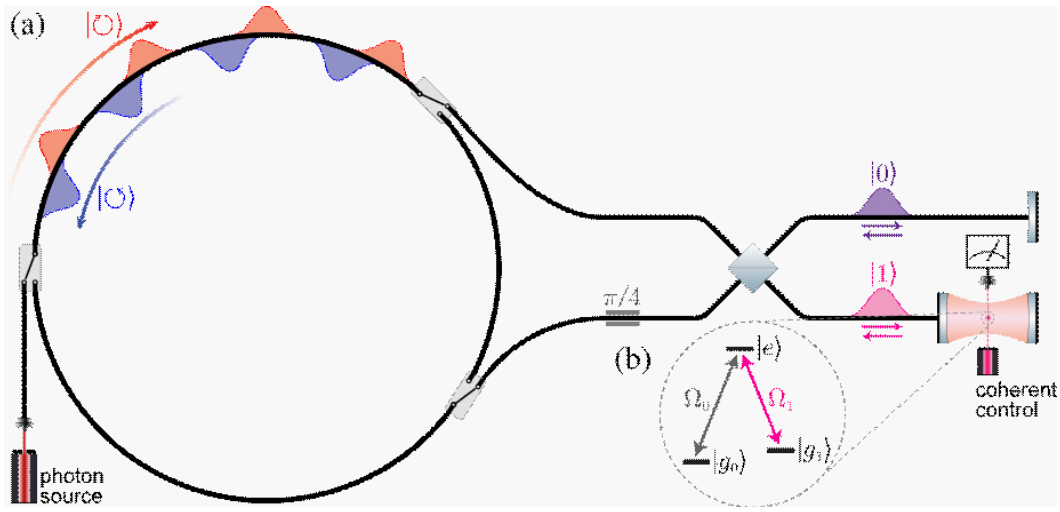


Figure 282: Example of a hybrid atoms-photons system. Source: [2575].

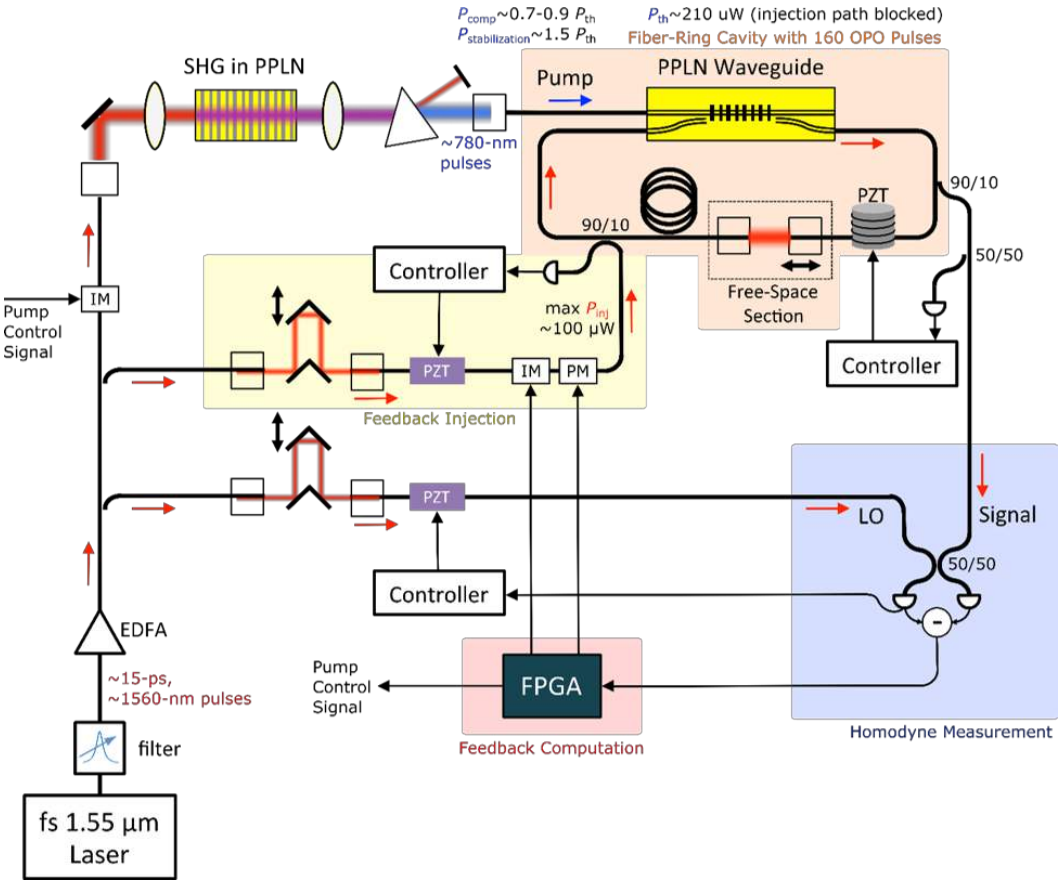


Figure 283: Example of realization of a coherent Ising Machine. Source: [2564].

Figure 284: The various properties or observables of photons that can be used to create a qubit. You have many more solutions than the old-fashioned polarization! Compilation ⓒ Olivier Ezratty, 2021.

The purity and high probability to get a photon per clock cycle are the enabler of quantum interferences based multiple qubit gates with discrete variable qubits.

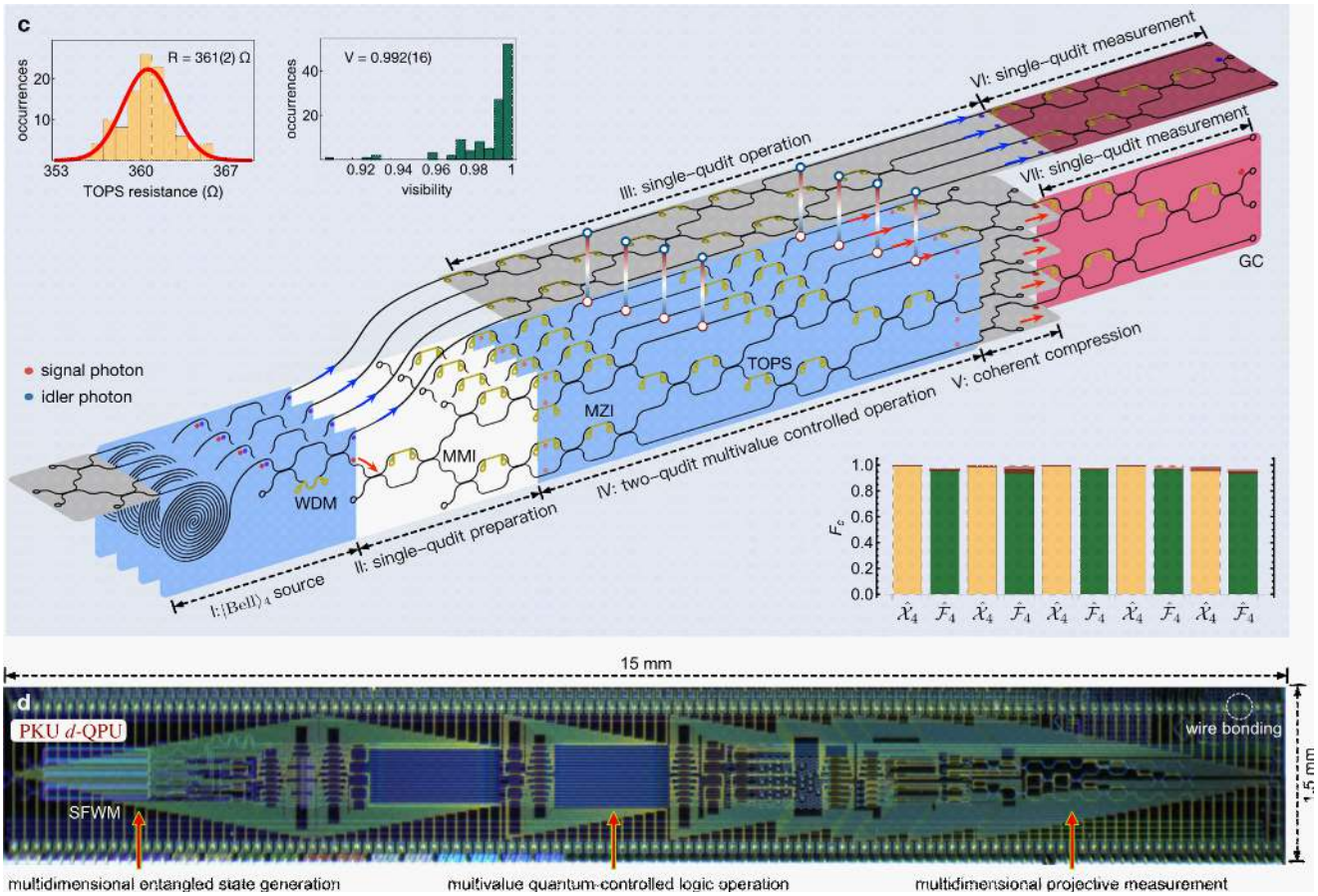


Figure 285: A ququart photons processor created in China. Source: [2579].

High-efficiency sources are qualified as "on-demand" or "deterministic" with the alternatives of heralded sources, where photon emission time can be accurately evaluated.

There are two main types of single photons sources (SPSs) [2519, 2582, 2583]:

- **Quantum dot single-photon source** are the best-in-class devices, able to generate photons with a 99.7% single-photon purity, and over 65% extraction efficiency, which could potentially reach 80% (meaning, 4 photons generated out of 5 clock cycles). See in Figure 286 how these efficiencies are improved. These sources also have an over 99% photon indistinguishability. In the second quantization formalism, they create a single Fock state with a photon number equal to one [2584].

  The leaders in this domain are **Quandela** [2585–2587] and **Sparrow Quantum** [2588]. And many research labs are working on other varieties of quantum dots [2589], including nanowire quantum dots [2590] and graphene quantum dots [2591]. These photon sources must be cooled at about 3K to 4K. In their Prometheus indistinguishable photon source, Quandela directly couples the quantum dot to a fiber, avoiding the use of cumbersome confocal microscopes and significantly increasing the photon generation yield. It creates a path to reaching a combined source–detector efficiency closer to the 2/3 threshold that is mandatory for scalable discrete variable optical quantum computing. Jian-Wei Pan's lab is advancing the field, having reached a system efficiency of over 70% in 2025 [98].

  Others are trying to operate these quantum dots at hotter or even ambient temperatures. That's the case with the quantum dots single photon emitters developed at EPFL, with a mix of gallium nitride and aluminum nitride (GaN/AlN) on silicon substrate, or with solid-state emitters operating at 28.8K instead of 4K that are studies in the UK [2592]. The UK results show a single-photon purity of 95% below 50K [2592], while the GaN/AlN emitters grown at EPFL reach photon emission rates of about 1 MHz with a single-photon purity exceeding 50% at room temperature [2593].

  Quantum dots can also be integrated into silicon wafers PIC (photonic integrated circuits). PICs so-called heterostructures combine InP microchiplets with embedded InAs quantum dots onto SOI wafers (silicon-on-insulator) where high-efficiency silicon waveguides are added [2594].

- **Parametric photon-pair sources** are laser pumping nonlinear optical waveguides or cavities that create photon-pairs. It can be integrated in nanophotonic circuits. They are using either spontaneous four-wave mixing (SFWM), or spontaneous paramet-

ric down-conversion (SPDC [2595], including three-wave-mixing [2596]) processes in nonlinear crystals.

The efficiency is lower than with quantum dots, reaching about 50% with a 95% photon indistinguishability from separated SPSs. Photons are created non-deterministically with a rather low 5% to 10% probability, which can be increased to above 60% with time and spatial domains multiplexing. Such solutions are embedded in hybrid nanophotonic chips like with PsiQuantum and others who consolidate photon sources, waveguides and circuits and then photon detectors [2597]. SPDC sources work at room temperature but for efficient multiplexing (>95%), it is necessary to use SNSPD detectors running at low temperature.

Progress is made with nanophotonic-based single photons generation, although their performance still lags behind quantum-dots sources [2598–2600]. Figure 287 shows a SPDC method to create pairs of entangled photons. The conversion creates pairs of orthogonally polarized photons in two light cones with entangled photons at their intersection.

- **Trumpet microwires** are single photon sources, studied in Grenoble, France and in Denmark at DTU [2601, 2602] with potential use cases both in quantum computing and quantum communications.

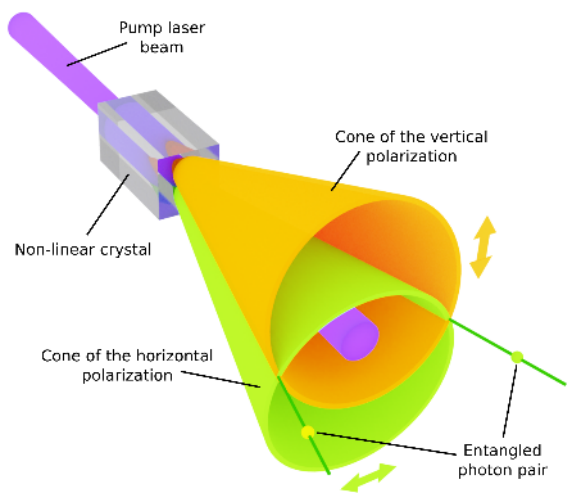


Figure 287: How entangled photons are generated with SPDC method. Source: Wikipedia.

- **Rydberg atoms single-photon sources** with excitation blockade creating efficient preparation of single atomic excitation, which are converted into high-quality single photons with high indistinguishability [2603]. They can create photon pairs that are dephased by π, enabling two photon quantum gates [2604, 2605]. Researchers in China reported an array of 50 individually addressable ^{87}Rb atoms to generate single photons in August 2026 [2606], although with a rather high antibunching ratio, with a $g^2(0)= 0.29$ when Quandela's quantum-dots based single photon sources had a $g^2(0)= 0.0028$ in 2022 [2607].

- **Metasurface materials** which can control multiple degrees of freedom of light such as phase distribution, frequency, and polarization [2608, 2609].

One key challenge with implementing MBQC, one dominant photonic quantum computing architecture that we'll cover later, is the ability to create large cluster-states of entangled photons. There are many options to implement it. Quantum dots source can be tailored for this need. Good indistinguishable and deterministic photon sources can be coupled with delay lines and mixers to create these cluster states.

There are even solutions to create hundreds of pairs of entangled photons, as investigated by the University of Virginia, using frequency combs. Here, the photon source is a continuous laser emitting a single continuous wave, a small 3 mm Kerr microcavity creates a frequency comb generating pairs of entangled photons around the pump frequency as described below. This could lead to massive multimode photonic quantum computing [2610] (Figure 290).

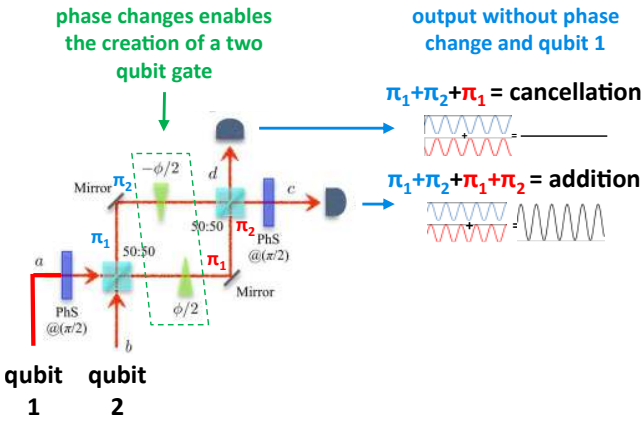


Figure 288: How a Mach-Zehnder Interferometer works. It creates an interference between two photons with introducing a dephasing linked to the number of mirrors reflections (the πs) and phase changers. ⓒ Olivier Ezratty, inspired by [2611].

Two-qubit quantum gates are difficult to realize because it is not easy to have photons interact with each other, particularly when they are not perfectly indistinguishable. They use optical circuits based on beamsplitters or Mach-Zehnder Interferometers with two inputs integrating phase changes on the optical paths, based on the KLM method already quoted in footnote (MZI, Figure 288). This does not work well when the photons are uneven, such as those coming from lasers. Namely, in only a few % of the cases. With indistinguishable photons, gates are more than 95% efficient since photons can interfere with each other. It facilitates Mach-Zehnder interferometry operations. These sources have the additional advantage of being very bright, which allows them to multiply the incoming photons and then to pass through many quantum gates. There are also solutions based on cavities. Research is also active on the creation of nonlinearities to improve the reliability of these quan-

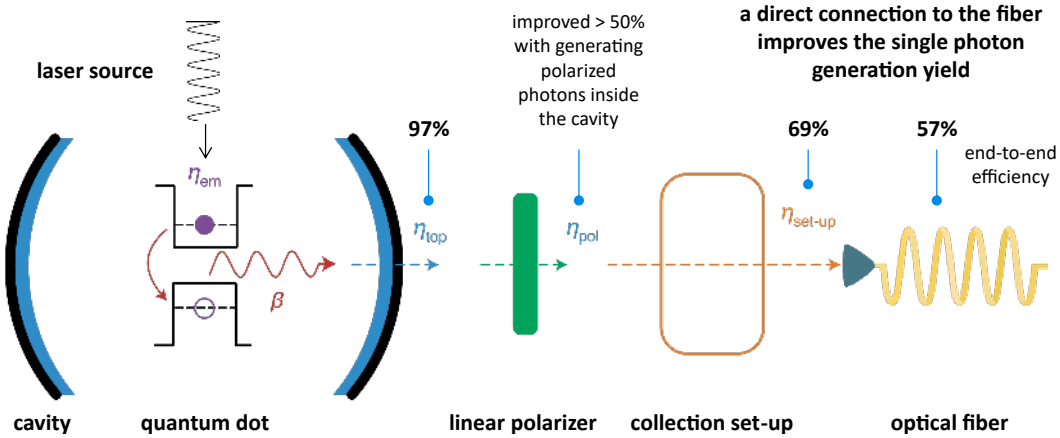


Figure 286: What characterizes the efficiency of a quantum dots photon generator. Source: [2585] and comments by Olivier Ezratty, 2021.

tum gates [2612, 2613]. Ideally, nonlinear separating cubes should be used. Loop-based settings using only linear optics are also proposed [2614, 2615].

Quantum Logic Gate	Unitary Matrix	Relation for MZI implementation	Elements
Beam Splitter(B(θ))	$\begin{matrix} cos\theta & -sin\theta \\ sin\theta & cos\theta \end{matrix}$		
50-50 Beam Splitter(B)	$\frac{1}{\sqrt{2}} \begin{matrix} 1 & -1 \\ 1 & 1 \end{matrix}$		
Hadamard(H)	$\frac{1}{\sqrt{2}} \begin{matrix} 1 & 1 \\ 1 & -1 \end{matrix}$	H=BZ	50-50 Beam splitter
Phase flip gate (Z)	$\begin{matrix} 1 & 0 \\ 0 & -1 \end{matrix}$	Z=HB	π Phase shifter
Bit Flip gate (X)	$\begin{matrix} 0 & 1 \\ 1 & 0 \end{matrix}$	X=BH	Beam Splitter, Hadamard
T gate	$\begin{matrix} 1 & 0 \\ 0 & \exp(i\pi/4) \end{matrix}$		$\pi/4$ phase shifter
S gate	$\begin{matrix} 1 & 0 \\ 0 & i \end{matrix}$		Quarter wave plate
Pauli Y gate	$\begin{matrix} 0 & -i \\ i & 0 \end{matrix}$		
CNOT gate	$\begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 \end{bmatrix}$	(I⊗H)×K×(I⊗H)	Kerr Media(K) Hadamard(H) Identity(I)

Figure 289: How photonic gates are implemented with phasers and MZIs. Source: [2611].

Single-qubit quantum gates use simple optical circuitry, including beamsplitters, waveplates, mirrors and semi-reflective mirrors, and phase shifters [2514]. For example, a Hadamard gate (H) uses a balanced beam splitter or a half-wave plate, a Pauli X gate (bit flip) is simply a swap of the two rails, implemented with a waveguide crossing or a mirror in path encoding and with a half-wave plate in polarization encoding, and a Pauli Z gate (phase flip) uses a phase shifter causing a 180° phase change (π) (Figure 289).

How about photonic gates execution times? It must be fast since photons traverse optical devices at nearly the speed of light in vacuum. Traversing a one-meter-long series of optical instruments would last only 3 ns. If the circuit is nanophotonic based, we'll get into the cm realm and reach tens of pico-seconds. But that's not the right way to evaluate the speed of quantum computing here, particularly when dealing with non-deterministic photon sources where computing must be repeated many times. Then, you may need to consider the speed of the electronics that define the various quantum gates along the photon route, and we may end-up adding milliseconds.

Qubit readout uses single photon detectors or photon number resolving detectors (PNRDs) that also capture their quantum state. This detection is still imperfect.

Several single-photons detection technologies are competing with each other:

- **SPADs**, avalanche photodiodes, which detect photon occurrences but not photon number) [2617, 2618]. Likewise, GeSi SPADs are proposed that could operate at room temperature [2619].
- **SNSPDs**, superconducting nanowire single photon detectors, which have good detection efficiency, low dark count rates and high timing accuracy in the near-infrared (NIR) and short-wave infrared (SWIR) wavelengths. Fully integrated SNSPDs are based on GaAs, Si and Si_3N_4 waveguides. In order to limit the dark count phenomenon coming from thermal effects [2620], these SNSPDs are usually cooled between 800 mK and 3K, a range reached with pulse-tube coolers and, for the sub-kelvin end, helium-3 sorption or adiabatic demagnetization stages [167, 2621, 2622]. NbTiN-based SNSPDs could work with higher-temperature cooling, between 2.5K to 7K [166] with some records reaching 25K [2623, 2624]. See Figure 291 for SNSPDs figures of merit evolution between 2016 and expected 2030 performance.
- **SWSPDs**, superconducting wide-strip photon detectors are variants of SNSPD with higher efficiency and operating in the convenient 1,550 nm telecom wavelength range [2625].
- **PNRDs** which can use arrays of SNSPDs and detect photon numbers [2626–2629]. Worth mentioning, PNRDs created in China in 2025 with an efficiency of 98% and with the ability to detect up to 32 photons (in that case, however, with very low fidelities given it's 21% for 6 photons) [54].

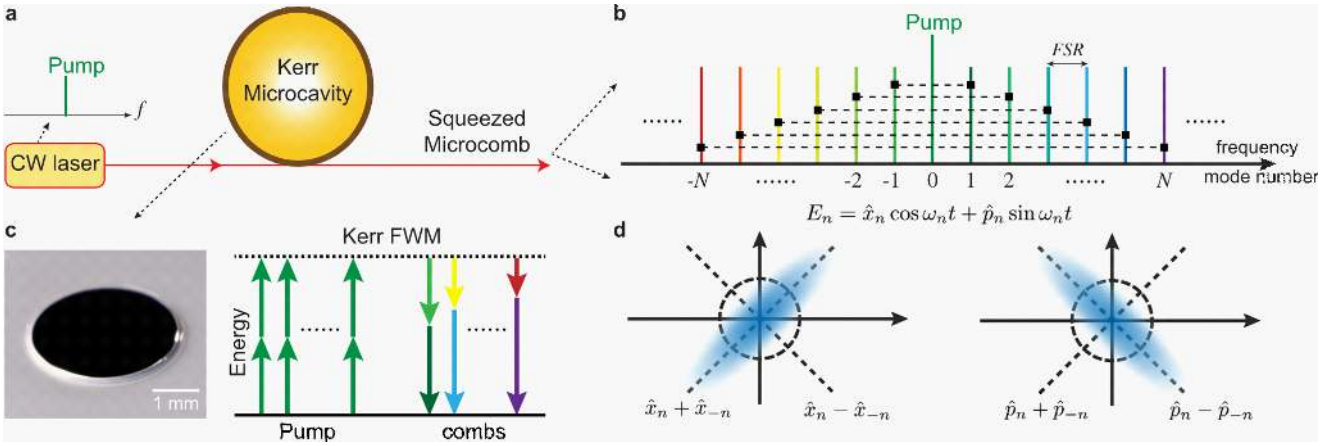


Figure 290: A frequency comb method to generate a large cluster state of entangled photons. Source: [2610].

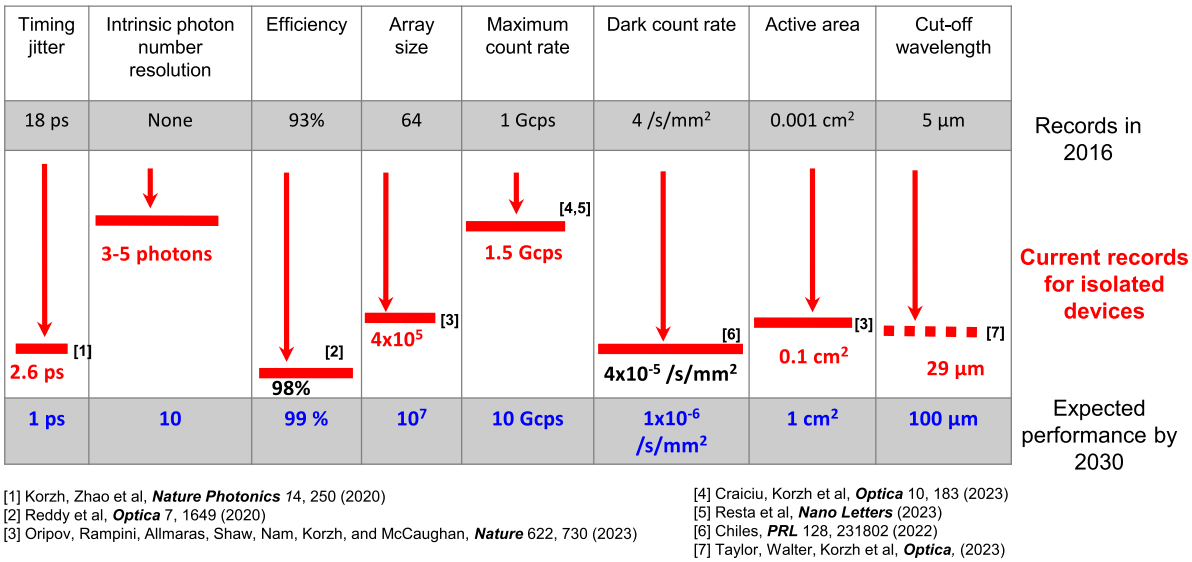


Figure 291: SNSPD progress between 2016 and expected figures of merit in 2030. Source: [2616].

- **TESs**, transition edge sensors, is a special breed of PNRDs [2630]. They are used by Xanadu in their PNRDs.

- **Homodyne and heterodyne detectors** are specialized for analyzing continuous variables qubits. Homodyne detectors such as optical parametric amplifiers (OPAs) detect the photon quadrature [2631]. Some SNSPDs can still support homodyne measurement to support continuous variable photon qubits [2632].

All these photon detectors implement destructive photon measurement. The photons are converted into some current, later amplified. It is still possible to detect photons without destroying them, like using the cross-Kerr nonlinear effect, with photon-atom coupling in cavities [2633] or with Rydberg atoms [2634]. But these non-destructive or non-demolition (QND) measurement methods are seemingly not widely used in quantum computing.

One key goal is to integrate these photon detectors directly in photonic computing circuits in heterostructure designs [2635]. There are even concepts of single photon detectors that can also detect their frequency with high precision [2636]. As another option, photon detectors operating at a relatively hot temperature of 20K, using cuprates who are known for their relatively high superconducting temperature [2637].

The key single photon detector vendors are **Single Quantum**, **Photon Spot**, **Quantum Opus** and **IDQ**, mostly using SNSPDs, but not all are operating at around 900 nm which is the usual wavelength of single photon source for photon qubits, while other are supporting telecom wavelengths around 1,550 nm which are more relevant for quantum key distribution.

From a physical point of view, these items are classical photonic components: single and identical photon sources, light guides, optical delay lines (optical fibers or voltage-controlled Pockels cells), Mach-Zehnder interferometers, beam splitters (splitters, which divide an optical beam into two beams, generally identical),

birefringent filters (which have two different refractive indices), phase shifters and single photon detectors [2638, 2639] (Figure 293).

To conduct experiments, these discrete and very affordable components are installed on carefully calibrated optical tables (like the ones from **Thorlabs**, Figure 292) of a few square meters with lots of instruments and photons that circulate largely in the free space of a darkened room.

Figure 292: A typical Thorlabs optical table on which discrete photonics elements are installed. The large table feet dampen ground vibrations. Source: Thorlabs.

1.10.4 Nanophotonics

Fortunately, the optical components used in photonic quantum computing are miniaturizable on photonic integrated circuits (PICs). This is part of the vast field of nanophotonics. Nanophotonics components are etched with feature sizes between 220 nm and 3 μm [2640, 2641]. In nanophotonics, quantum gates are dynamically programmed by the conditional routing of photons in optical circuits and/or with their modification (phase, polarization, frequency, ...) driven with electrical circuits.

These circuits are often etched on silicon CMOS platforms, on group IV materials such as germanium and SiGe, or on III-V compounds such as GaAs and InP. Their components can be assembled in a modular way as shown in the functional diagrams in Figure 294. Many semiconductor fabs in the world are helping in the design and prototyping of nanophotonic circuits to support photon qubits. We will mention here only a few of them.

PICs are manufactured using classical silicon-based CMOS processes [2642], hybrid CMOS with silicon nitride (SiN, for low-loss waveguides), lithium niobate ($LiNbO_3$) [2643, 2644], III/V materials (GaAs [2645], InP, ...), silicon nitride, barium titanate (BTO, to create phase shifters on silicon wafers), etc [2646].

In the case of a silicon integrated nanophotonic circuit, photon wave guides are in silicon, which is transparent for the used wavelengths, within silicon oxide, thus the use of SOI wafers which initially contain a silicon oxide layer. One key figure of merit of these circuits is to minimize photon losses. It involves precision etching of silicon waveguides but also different postselection and postprocessing techniques [2648]. One goal is to reach the low losses of the best optical fibers, which can be obtained with germano-silicate waveguides as prototyped by Caltech in 2026 on light ranging from violet to telecom wavelengths [2649] (Figure 295).

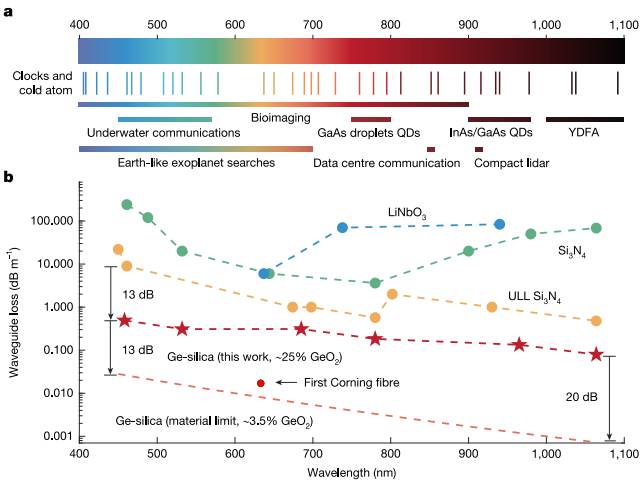


Figure 295: Low-loss germano-silicate waveguides prototyped by Caltech in 2026. Source: [2649].

Another challenge is the heat generated by phase shifters which can be problematic when the circuit is cooled when it also contains photon sources and detectors like with PsiQuantum's QPU. Also, these phase shifters require some expensive calibration that must be optimized [111]. The phase shifter electronic drive signals are usually generated at room temperature. But photon detectors (SNSPDs, PNRDs) generate analog signals that must be amplified. This can be done with cryo-CMOS running at the same 2K to 4K temperatures as the detectors [104].

Designing PIC is a process that is less mature than with classical electronics circuits. Challenges emerge as the circuit size is growing. Electronic-photonic design automation (EPDA) tools play a key role here, and can be improved with the help of classical machine learning and quantum algorithms [2650]. The end result is a PDK (process design kit) ready to be used by clean rooms. They contain the circuit design information, including device models, building blocks, design rules, verification deck and manufacturing process parameters.

Global Foundries is a key vendor in that space with its cleanroom in Malta, New York State, which produces thousands of silicon-based wafers for PsiQuantum.

CEA-Leti in France is building an integrated silicon photonic qubits platform including single photons sources, phase shifters and superconducting nanowire single-photon detectors (SNSPD) or CdHgTe avalanche photodiodes (APD), working at 2.5-4K that is compatible with single photon detectors. They are initially targeting secured QKD-based telecommunications.

ETRI and **KAIST** in South Korea are also engaged in manufacturing PICs. In 2024, they demonstrated a 4-qubit processor silicon PIC (SiPIC) [2651].

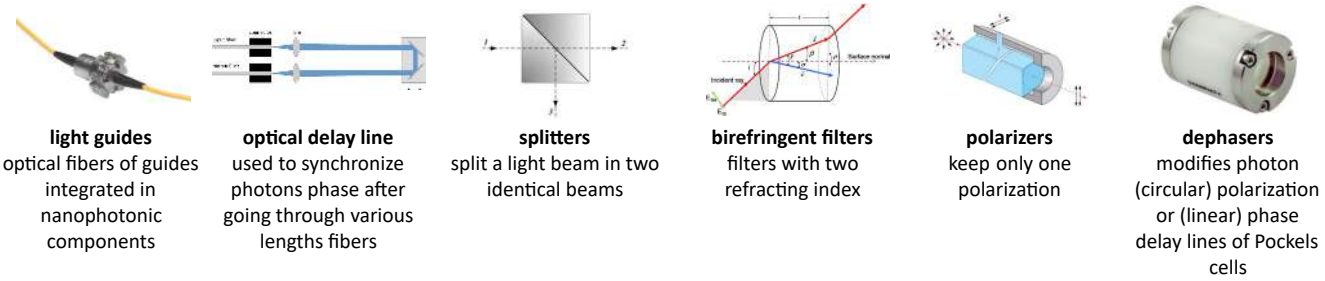


Figure 293: Various optical tools to control light in a quantum processor. These are made for experiments and can be miniaturized in nanophotonic circuits. Compilation ⓒ Olivier Ezratty, 2021-2025.

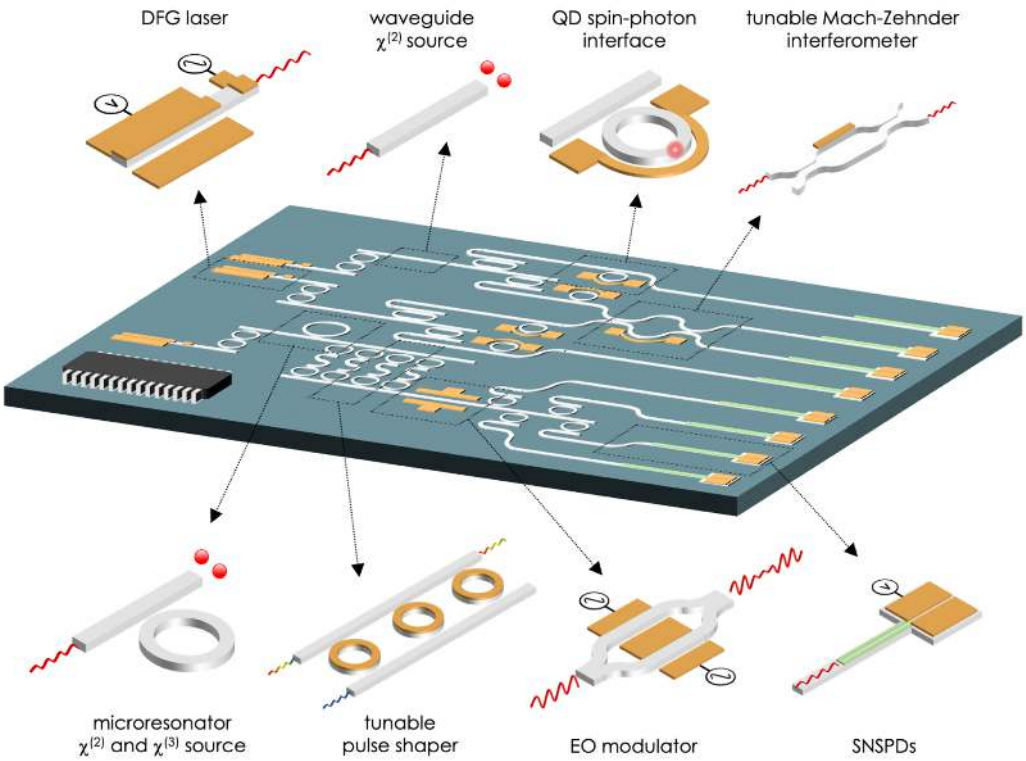


Figure 294: Examples of photonic functions embedded in a nanophotonic circuit, here in GaAs. Source: [2647].

Ultimately, photonic quantum computer would consolidate three key components as shown in Figure 296: a single photon generator, integrated photonic circuits and single photon detectors. The first and last ones are integrated with a cryogenic system operating at about 10K and 2K-4K respectively. But it seems also possible to integrate photon sources and detectors in a single photonic chip [2652, 2653].

The most active countries in the field seem to be China, the UK (particularly at the Universities of Oxford, Bristol, Cambridge and Southampton) [2654], France (C2N, LKB, ...), Italy [2655], Germany (Universities of Stuttgart and Paderborn), Austria, Australia, Japan and of course the USA.

Photon qubits are the specialty of some startups like **PsiQuantum**, **Orca Computing**, **Tundra Systems Global**, **QuiX**, **Quandela**, and **Xanadu** [2657].

1.10.5 Boson sampling

The idea of boson sampling was proposed by **Scott Aaronson** and **Alex Arkhipov** in a seminal paper published in 2010 [2521]. They devised a linear optics-based experiment that would be impossible to easily emulate on a classical supercomputer. In quantum computing, we rely on only one type of boson: the photon. The other bosons are elementary particles such as gluons or Higgs bosons that can only be observed in particle accelerators. There are also composite particles such as the Cooper pairs (double electron) which are at the origin of superconducting currents. But when we talk about boson sampling, we always mean "photon".

Boson sampling is about solving a problem of sampling the probability distributions of identical and indistinguishable photons being mixed in an interferometer and reaching photon detectors. This physical process is impossible to emulate above a certain threshold, which generates yet another so-called "quantum supremacy"

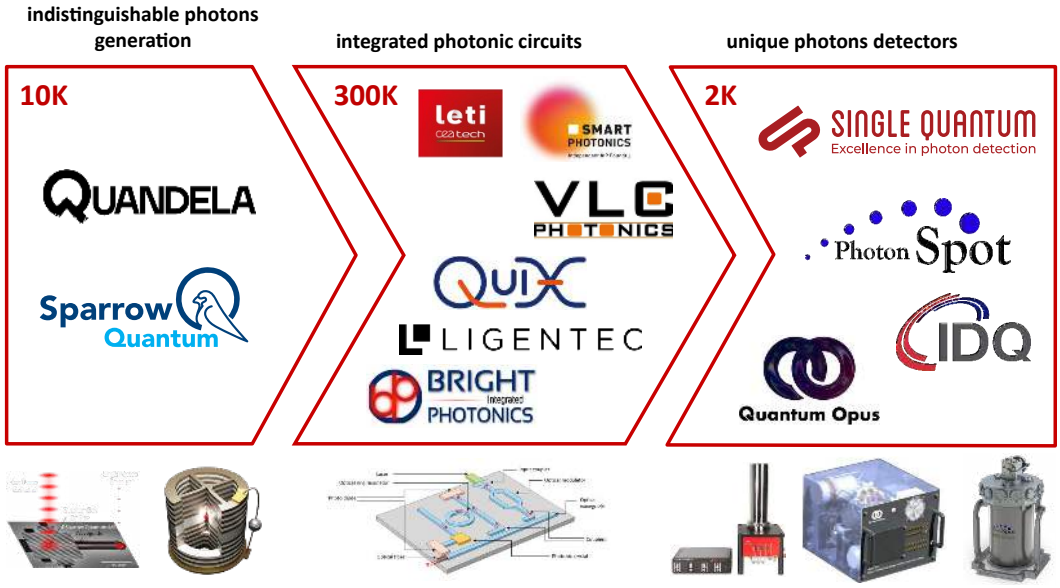


Figure 296: Key components of a photonic quantum computer: quality photon sources, preferably deterministic, nanophotonic circuits for processing, and photon detectors for readout. Source: adapted from [2656] in slide 11. Olivier Ezratty, 2023-2024.

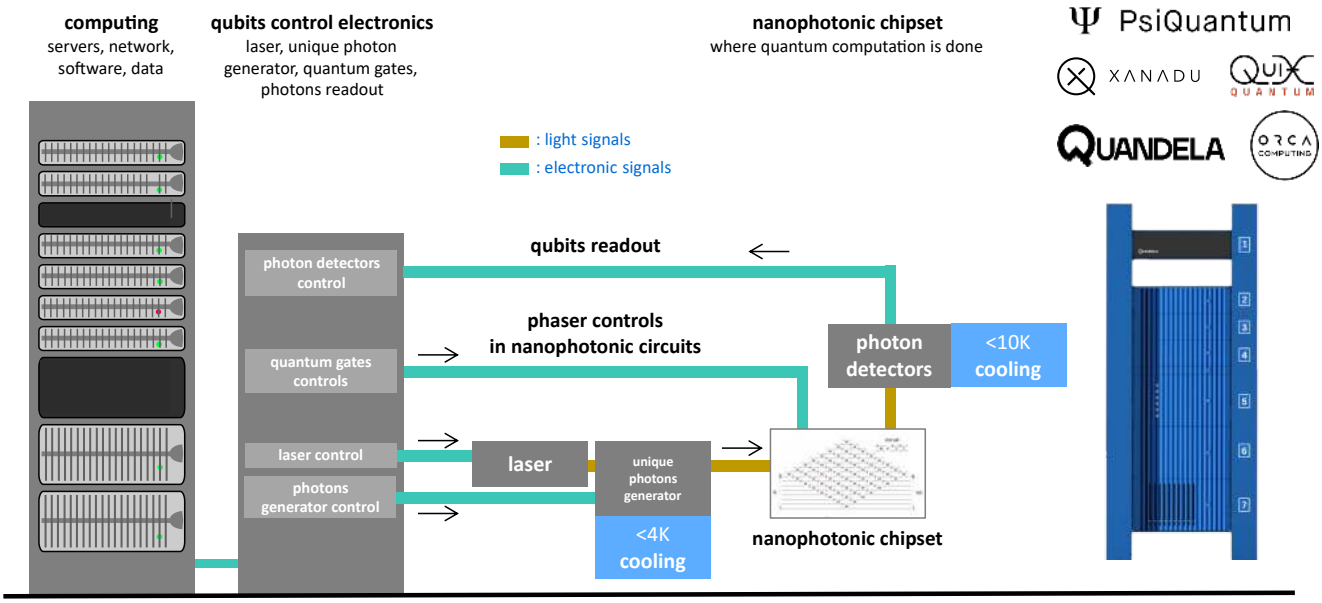


Figure 297: Typical architecture of a photon qubits quantum computer. Olivier Ezratty, 2022-2024.

or "advantage". It becomes an "advantage" only if the system can solve a particular problem with some input data and useful output data.

A classical emulation of a boson sampling experiment requires extremely heavy matrix computing, namely the evaluation of the permanents of square matrices [1005, 2658]. This sits in the "#P-hard" problem class of the complexity theories zoo, #P being the class of function problems that counts the number of solutions of NP problems. The verification of the obtained result can't even be carried out by a classical computer [2659].

Boson sampling is the quantum and photonic analogue of the famous **Galton** plate experiment where balls cross rows of nails in a random way and end up in columns, with a Gaussian distribution (Figure 298). This experiment is based on various probability concepts: convergence of a binomial distribution law towards a normal or Gaussian distribution, Moivre-Laplace theorem, etc. In the photon-based experiment, photons are injected into a series of interferometers combining them with their neighbor in a random way. On the other hand, the distribution at the end does not follow a Gaussian curve. It depends on the photons being sent upstream.

The appropriateness of the boson sampling style exercise is questionable. It implements a physical phenomenon with photons that is difficult to emulate in a classical way. But this is a valid reality for the simulation of many complex physical phenomena, such as the folding

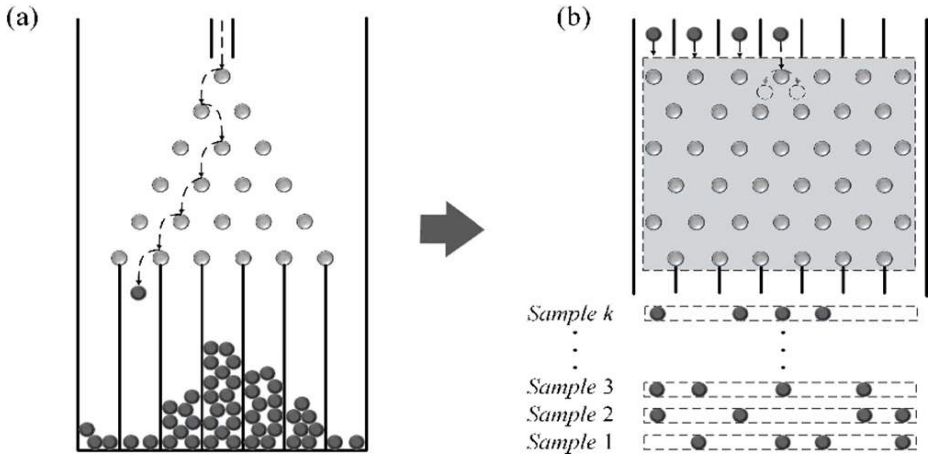


Figure 298: The Galton plate experiment that inspires Boson sampling. Source: [2660].

of a protein or the functioning of a living cell, except that these remain in the realm of the living and are not simulated in a machine.

However, it is not strictly a form of calculation with some problem input data. There is not even a real notion of qubits, quantum gates and programming, except in the choice of the photons we send into the system.

In the first boson sampling experiments, the used optical components were all passive and static, except for the photon generators and detectors [1006]. The experiment generates additive and subtractive photon interferences and superpositions of quantum states [2661, 2662].

Chinese researchers are particularly active in the field [2663], but they are not alone. Xanadu (Canada), and Fabio Sciarrino in Italy, Australian and French teams have also been conducting interesting boson sampling experiments for a while, using Fock states boson sampling settings [2664].

In June 2019, the **Hefei** laboratory created a boson sampling using six photons with three degrees of freedom, their traveled path, polarization, and orbital angular momentum [2665]. It had a reported error of 29% on the sampled distribution, there being no quantum gates as such in a boson sampler. In October 2019, they upgraded the feat to 20 photons with an experiment presented as reaching quantum supremacy, at the time of Google Sycamore supremacy announcement [2666]. In this experiment described in Figure 300, 20 indistinguishable photons were sent in a series of splitters and ended up in 60 photon detectors. The output Hilbert space was limited to 14 detectors, with a size of 3.7×10^{14} or 2^{48}. With the 60 activated detectors, this space was to reach a size of 60^{20} or 2^{118}.

The size of Hilbert's space of such a device is evaluated with the size of the Fock space of M modes occupied by N photons. The number of ways to distribute N indistinguishable bosons over M modes is $\binom{N+M-1}{N}$, so with $N = 20$ photons and $M = 60$ modes it is $\binom{79}{20} = \frac{79!}{20!\times59!} \approx 5.5 \times 10^{18}$ [2667].

The researchers in China indicated that they could use several hundred detectors in output and use some photons double encoding using polarization and spatial encoding to multiply the power of their system and thus make it able to create a NISQ (noisy intermediate scale quantum computer) system.

This represents the number of incoming photon detectors at the power of the incoming photon number. The previous record was 5 photons over 16 modes and the sampling was verifiable on a classical computer whereas with these 20 photons and 60 modes, it was no longer possible. The photon generator was realized with quantum dots in gallium and indium arsenide, placed in a 4K cryostat. The photon mixer used 396 beam splitters and 108 mirrors (Figure 299). For the experiment to work, one photon must arrive at the same time in all the inputs of the photon mixer. The corresponding probability is very low. They used active demultiplexers with Pockels cells to demultiplex and direct the photons.

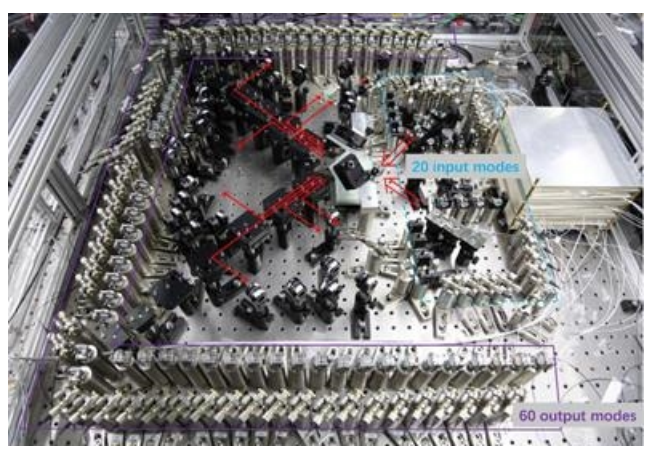


Figure 299: Optical table of the 20 photons/60 modes China experiment in 2019. Source: [2666].

While the first boson sampling experiments did not show any usefulness, this changed progressively. It was initially thought that boson sampling could eventually lead to applications in homomorphic encryption and blind computing [2514]. Some algorithms also exist for the

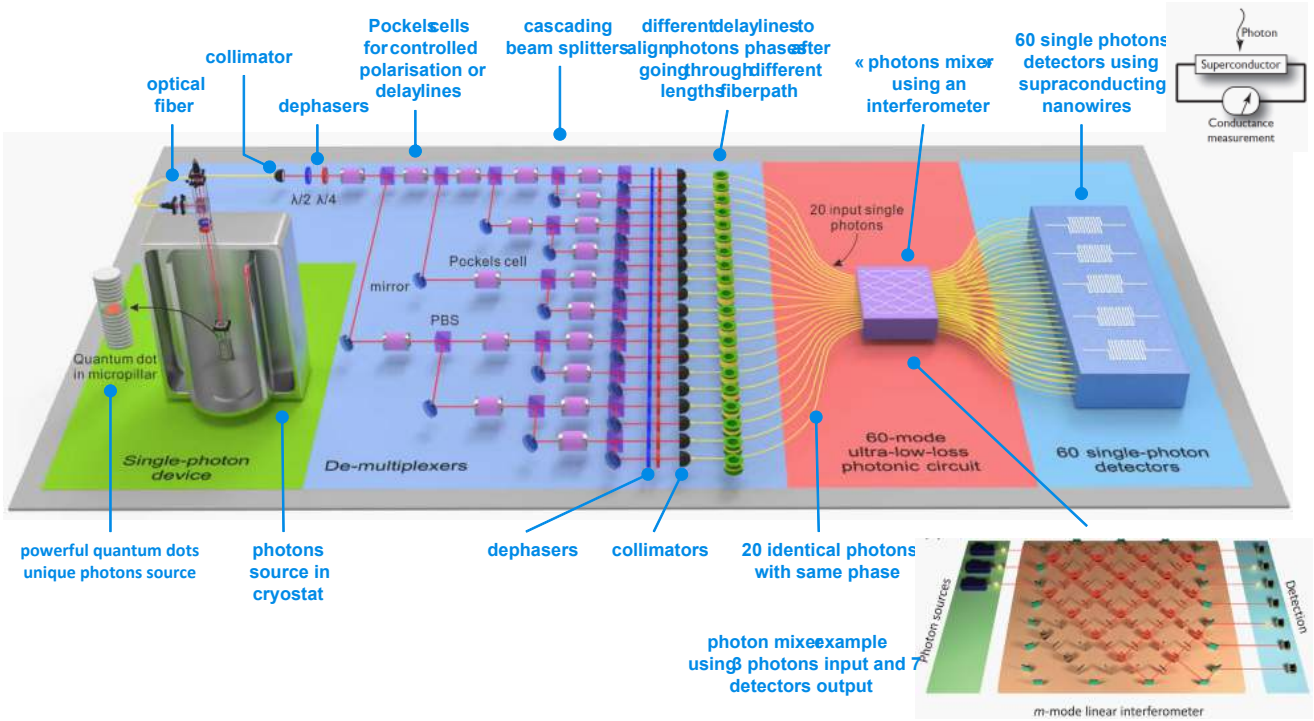


Figure 300: One of the first Boson sampling experiments made in China, in 2019, with 20 input photons in 60 modes. Source: [2666].

simulation of molecular vibration spectra [2668, 2669]. In 2020, a team in China conducted an experiment similar to boson sampling to play a variant of the Go game [2670].

In 2020, another China team used an optical quantum calculator to solve a useful problem, the subset-sum problem, which is complete NP. The system shown in Figure 301 uses a nanophotonic chip. The problem was to determine, apart from a set of signed integers, whether it is possible to add a subset of them together to obtain a given integer [2671]. The system used a laser as a source of photons. The benchmark was realized with N=4 integers. With some extrapolation, their system was to beat all other known methods of solving this kind of problem.

In 2024-2025, a team in Japan led by Kae Nemoto proposed to create a form quantum optical reservoir computing powered by a boson sampler for solving a MNIST image classification task [2672]. It fared better with regards to classification accuracy than a classical linear classifier (L-SVC). They were using a classical PCA (principal component analysis) to define the parameters of the boson sampler and a linear classifier at the exit of the sampler. They obtained classification error rates above 2%. It was not compared with the more efficient and standard classical CNN (convolutional neural networks) and capsule networks which generate error rates as low as 0.25% [2673], because the researchers found this to be "unfair".

Jiuzhang 1.0 was a **gaussian boson sampler** (GBS) setup implemented in December 2020, sending 50 single-mode squeezed states into a 100-mode interferometer and registering up to 76 photon clicks [2517, 2674]. The experiment was even more impressive than the previous ones and the publicized quantum advantage reached new heights. GBS output probabilities are given by hafnians, a matrix function that counts the perfect matchings of a general graph, where the permanent counts those of a bipartite graph. The two are related but distinct, with $\mathrm{per}(A) = \mathrm{haf}\begin{pmatrix} 0 & A \\ A^T & 0 \end{pmatrix}$ [2675]. The system, shown in Figure 302, was not more programmable than the previous ones. So, any computing advantage claim was still dubious.

Late 2020, a competing team in China implemented another form of boson sampling using "membosonsampling" for which an emulation requires even more complicated Haar-random unitary matrices [2676]. But it was not programmable.

Jiuzhang 2.0 came in June 2021 and was a somewhat programmable GBS, ramping it up to 113 detection events extracted from 144 photon modes circuit shown in Figure 303. The input squeezed photons are phase programmable before they enter the fixed part of the system in the interferometer that implements random unitary transformations. The experimenter still worked on some real-world algorithms and benchmarks to demonstrate some sort of quantum computing advantage [2677]. It was finally presented in 2023, using a 50 single mode squeezed states input to solve two graph problems, the Max-Haf problem and the dense k-subgraph problem [2678]. However, the research team wrote that it was still unsure whether the GBS could yield a real quantum advantage compared to improved classical, and quantum

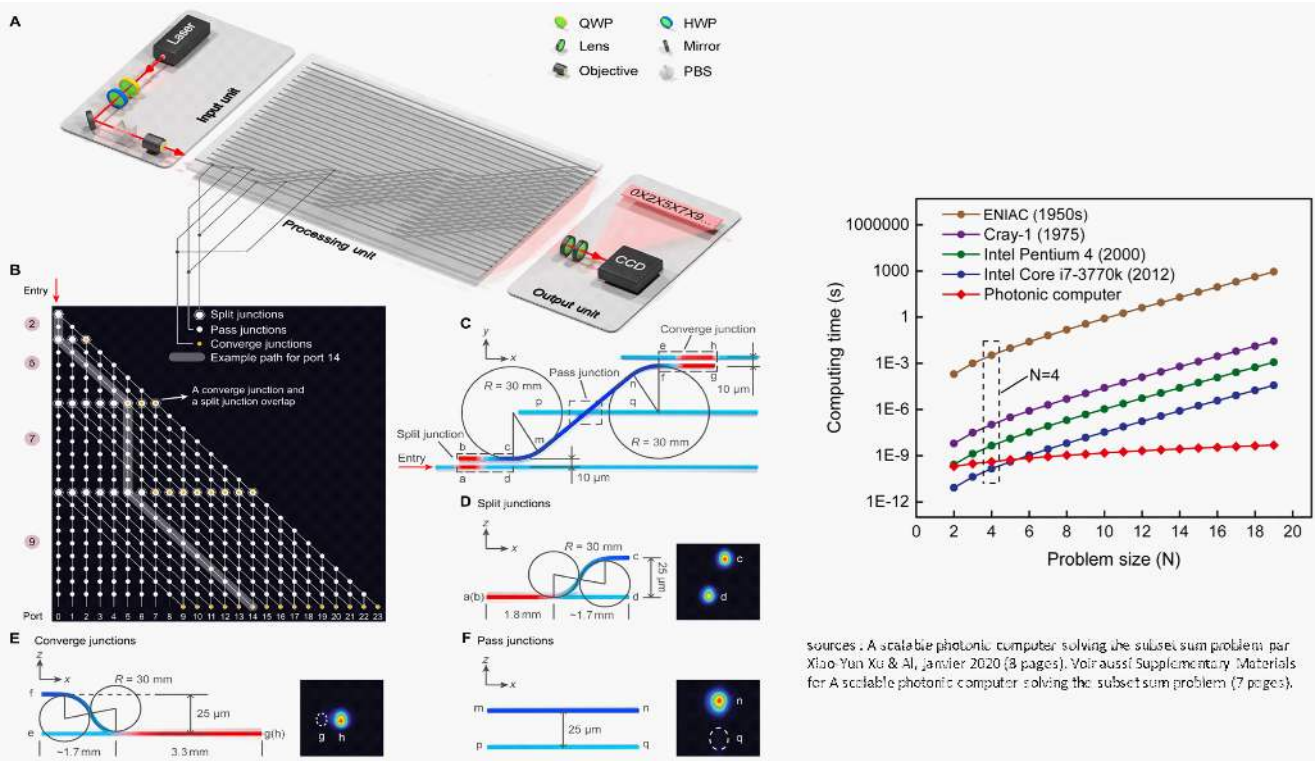


Figure 301: A first optical calculator to solve a useful problem created in 2020. Source: [2671].

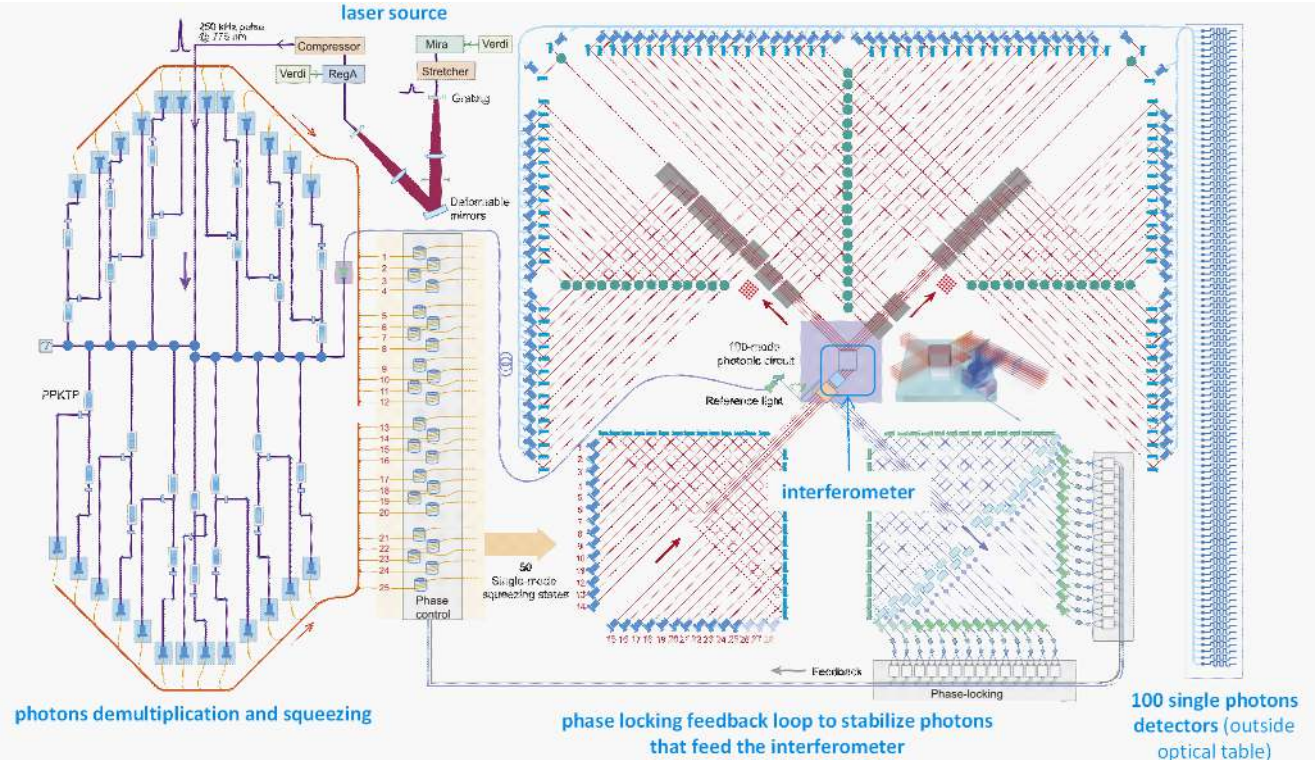


Figure 302: The Jiuzhang 1.0 gaussian boson sampler implemented in 2020 in China, with a 100-mode interferometer and up to 76 detected photon clicks. The physical setup was complicated and impressive, particularly with all the fibers and delay lines and their 100 single photon detectors. Source: [2517].

inspired algorithms. Also, like in many such advantage claims, the GBS advantage depends on the properties of the input graphs.

Jiuzhang 3.0 was introduced in 2023. It reuses the 144 spatial modes of Jiuzhang 2.0 and adds a 1×8 fiber-loop demultiplexer on the outputs, so that the Gaussian state facing the detectors effectively spans 1,152 modes.

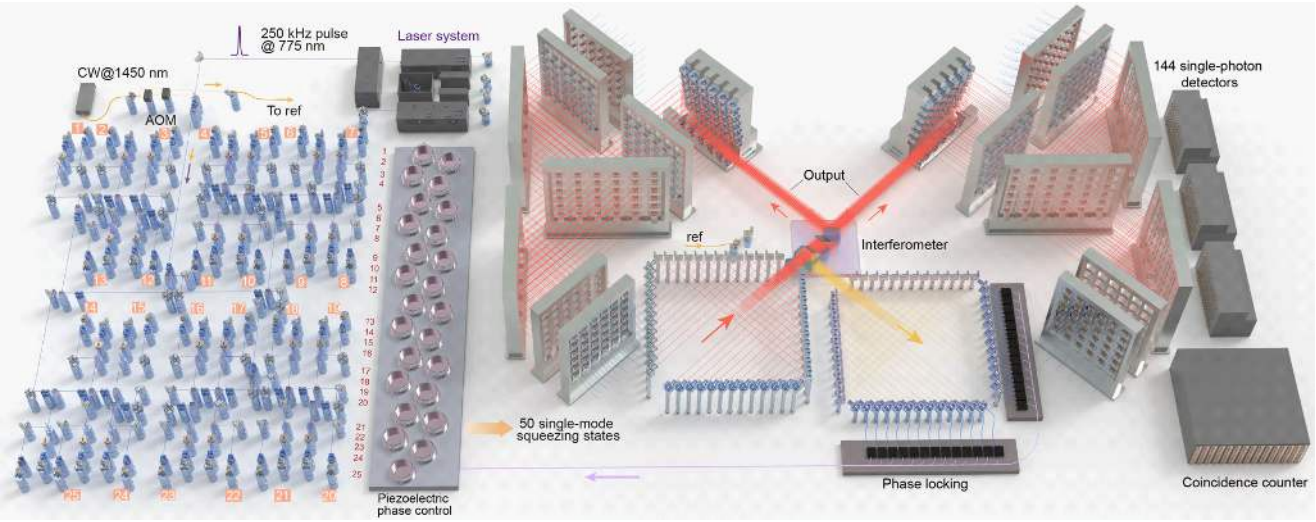


Figure 303: The Jiuzhang 2.0 boson sampling experiment achieved in China in 2021 with 144 photon modes. Source: [2677].

This pseudo photon-number resolving scheme raised the record to 255 click events [2679]. The team said that the DoE Frontier supercomputer would take about 600 years compared to 1.27 μs to produce a sample, with an extreme 3.1×10^{10} years to generate the hardest sample from the experiment which used temporal spatial demultiplexing *ala* Xanadu. It was however not linked to some practical use case and the interferometer did not seem to be anymore programmable than the one in Jiuzhang 2.0. Future experiments with some input data and a programmable interferometer may change that.

Jiuzhang 4.0 was presented in a preprint published in August 2025 and has since appeared in Nature. It is a new generation of a Gaussian Boson Sampler [2680]. It is generating 1,024 squeezed states that are injected into a hybrid spatial-temporal encoded, 8,176-mode programmable photonic quantum processor, which produces up to 3,050 photon detection events, with a 92% source efficiency and a 51% overall system efficiency (Figure 304). It enables the production of yet another supremacy experiment that is difficult to classically simulate, even with tensor networks. On the El Capitan supercomputer in the USA, the state-of-the-art MPS tensor-network algorithm would need more than 10^{42} years to do this. The Jiuzhang 4.0 takes 25.6 μs to produce a sample. The system uses a programmable spatial-temporal hybrid encoding circuit. In the future, they say it would enable them to control 3D qumodes cluster states for the implementation of some FTQC architecture.

In 2024, a distributed research team in China created another programmable GBS using time-bin photons encoding and implemented a drug discovery algorithm using some RNA folding technique [2681]. The same year, an NBI team in Copenhagen determined that a GBS could bring a quantum advantage using quantum emitters having an efficiency of 60%-70% and MZIs with a transmittance of 99.92% per component. Currently, MZI transmittance sits between 90% and 95% [2682]. In 2024, researchers demonstrated how a GBS could support specific machine-learning tasks [2683] and data-mining problems with grouping together rows and columns of a dataset according to certain criteria [2684]. In 2025, a Jiuzhang-class GBS was used for some MNIST image recognition (handwriting) task, but with no clearly demonstrated quantum advantage [2685].

In September 2026, a team in Shanghai along with TuringQ created a GBS supporting the detection of up to 11,059 photons which they used to modelize some physical dynamics [2686].

An academic team from Denmark explored the use of a GBS to solve a complex problem of approximating Gaussian expectations [2687]. Its input data is a covariance matrix which represents a Gaussian distribution that you need to sample. There is also a function to be integrated against the matrix. The GBS could be theoretically prepared to encode this matrix but the paper did only a classical simulation of the process. It seems the input unitary matrix must be diagonalized beforehand. Programming the covariance matrix into the GBS has a runtime complexity of $O(N^3)$, so it scales fast although not exponentially. The proposed algorithm is said to be better than a classical Monte Carlo sampling method.

In 2022, **Fabio Sciarrino** in Italy also demonstrated that it was possible to create a programmable interferometer in a boson sampler [2688, 2689]. In 2025, he expanded the idea with Adaptive Boson Sampling which is using post-selection and for some quantum machine learning use case [2690]. Other proposals have been made to implement GBS for quantum machine learning tasks [2691].

In 2022, **Xanadu** did create a programmable GBS using some simpler time-bin multiplexing. It was even made available in the cloud but with caveats we'll describe in the photonic qubits vendor section. It could be used to solve dense subgraph identification problems [2692]. In

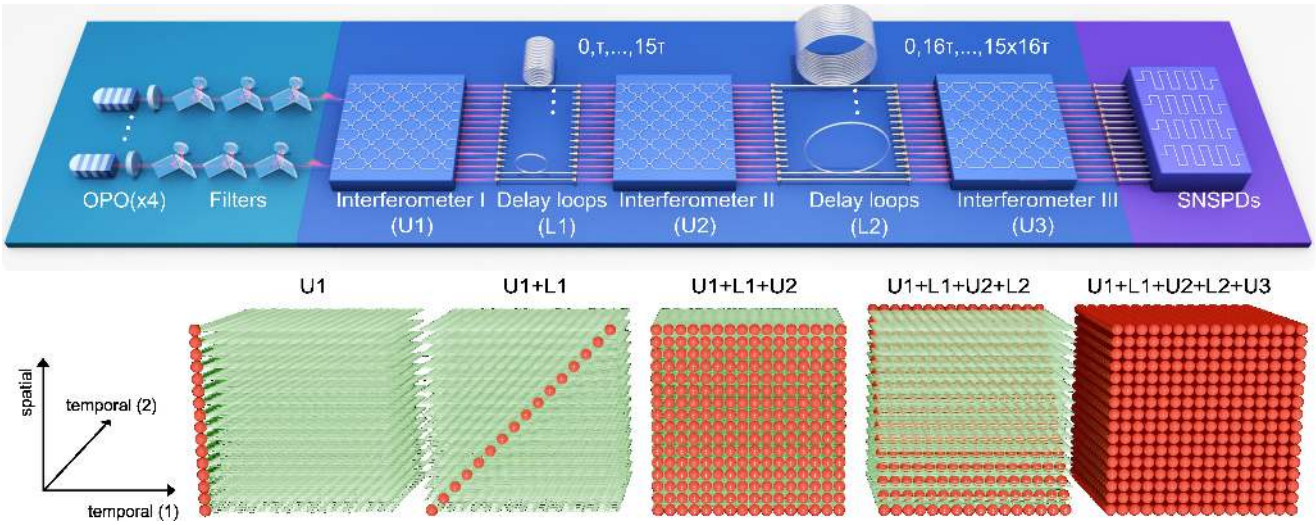


Figure 304: The Jiuzhang 4.0 gaussian boson sampler is simpler than previous GBS experiments. It uses 4 optical parametric oscillators (OPOs) that generate single-mode squeezed states which are sent into a spatial-temporal hybrid encoding circuit containing three 16-mode interferometers connected by two fiber-delay-loop arrays. They use two consecutive time-bin splitting in two interferometers. A cubic scaling of photon connectivity ($16^3 = 4096$) is shown, with one dimension being on the spatial domain and the two other dimensions being on the temporal domain. At the output, they use only 16 SNSPD photon detectors, having an efficiency of 93%. Source: [135].Added in 2025.

2023, a **South Korean** and US research team proposed a shallow-depth linear optics architecture implementing both Fock-state and Gaussian boson sampling with the capability to bring some computing advantage [2693]. A last note here: boson sampling experiments can also be implemented with cold atoms [2694].

However, Gaussian boson sampling can be classically simulated when accounting for the inevitable noise and photon losses [2695]. So, quantum supremacy or advantages in that paradigm may not be long lived [2696].

1.10.6 Measurement Based Quantum Computing

MBQC is a very particular approach to quantum computing. It exploits the initialization of entangled qubits and then performing step-by-step measurements on certain qubits to obtain a result on the last measured qubits at the end of the run [2697–2708].

There are several variants, the *one-way quantum computing* (1WQC [2709]) which uses two-dimensional qubits matrices to create cluster states and the *measurement-only QC* which only measures qubits, without prior entanglement. We will focus here on the first method which seems to be the most commonplace.

MBQC allows the execution of classical quantum algorithms with universal gates. Where is it relevant? It is particularly interesting in qubit-based quantum systems where it is difficult to create multi-qubit quantum gates exploiting entanglement and where the number of chained gates is limited for physical reasons. The model was initially created for cold atoms and trapped ions [2710] and is still studied for these environments [2711], but it later made more sense with photon qubits for which deterministic two-qubit gates are impossible to create. A 2025 proposal to use cold atoms to create cluster states and implement MBQC came out of MIT's Vladan Vuletić team and Harvard [2170]. Still, with a lot of heralding and clusters of 15 atoms, probably generating the need to implement a FBQC-like model with probabilistic fusion gates between the clusters (see how this works later with PsiQuantum's approach).

Photons are also indicated because they make it easy to manage rotation angles in the Bloch sphere that are used in the single-qubit quantum gates of the process, via a phase control of the photon qubits. It can also be implemented with other types of qubits like silicon carbide defects [1652].

With MBQC, things are done a bit backwards with respect to gate-based quantum computing: we first apply single-qubit gates and measure qubits progressively, whereas in gate-based quantum computing, we implement reversible unitaries (single and two-qubit quantum gates) and then make measurements at the end of the circuit.

A big warning here: understanding how MBQC works is not easy. You can easily get lost in how things are organized in space and time, particularly with the 3D [2712], 2D and 1D variants of MBQC that are using foliation [2713].

MBQC is **measurement-driven** and consumes its resource state. The measurement record is not reversed operationally, unlike in a circuit built from universal quantum gates, but the logical transformation implemented by the measurement pattern may itself be unitary and therefore mathematically invertible.

A quantum computation executed with universal gates is the equivalent of applying a unitary transformation embodied by a giant square matrix of dimension 2^N to a set of N qubits initialized in the state $|0\rangle$. This matrix can be inverted by scrolling backwards the quantum gates that were used to create it. With MBQC, this is not possible. This irreversibility of MBQC calculations explains why it is also called 1WQC for One Way Quantum Computing [2714]. There is no way of going back.

This model is also **probabilistic**, due to the probabilistic nature of the state measurement of qubits at each step of the calculation. The successive measurements provide information on the state of the qubits, which makes it possible to become determinist again in the rest of the computation by applying a kind of error correction on the fly. A bit like using 3-qubit error correction codes.

MBQC is a **hybrid** method since its implementation depends on interactions between quantum computing and the exploitation of qubits readout data by a classical computer controlling the system and in real time. This must happen very fast, at the scale of photon speed in photonic circuits.

Postselecting vs heralding

With postselection "*all photons are measured, and successful state generation events are determined by the measurement pattern across all modes. As a result, the state is generated and consumed at the same time, and it cannot be used for further processing. This technique is commonly referred to in literature as postselected entanglement generation*".

Heralding "*uses ancilla photons to indicate the circuit success without destroying the state. Measurement patterns are defined over a subset of the modes, and upon specific patterns being measured, the remaining photons in the remaining modes form a state that can be used for further processing, unlike in postselected approaches. This technique is called heralded entanglement generation and is the focus of this review*".

Source: [2715].

Qubits in cluster-state MBQC can play four roles: those that are prepared and measured (the ancilla qubits), those that are only measured during computing, those that are only prepared (but measured at the end of computing) and those that are neither prepared nor measured (and are used for the rest of computing).

The principle is based on the sequencing of so-called NEMC sequences with four steps [2716, 2717]:

- Using a set of **ancilla qubits** (step N), which are measured with Z projections.
- Creating **cluster-states of entangled qubits** (step E) [100]. With photons, there are many ways to generate these cluster states. It is one of the key scientific and technology challenges with MBQC. Theoretically, you could generate these cluster states with regular independent qubits and apply to these photons a series of single and entangling quantum gates (H, CNOT, etc) [2718, 2719]. These entangling gates are difficult to create with photons and MBQC is a method that gets rid of these in the first place. So, scientists are looking for ways to generate these cluster states with other means. There are many figures of merit here: the source must be as deterministic as possible and avoid so-called heralding and post-selection methods that reduce the chance to get a full cluster state at a given moment. There are also 1D, 2D and even 3D cluster states, the two latter being generated with delay lines [103]. They can use discrete variables (PsiQuantum) as well continuous variables encoding (Xanadu).
- A 2024 record with 60-mode continuous-variable cluster states was created in China in a chip-based optical microresonator pumped by chromatic lasers [56]. PsiQuantum is generating rather small photonic cluster states and connecting them with so-called "fusions", that implements probabilistic measurements. Another option creates cluster states with entangled photons using multiple properties (polarization, phase, etc.) [2720].

Photonic cluster states can be generated in many ways which have evolved over time with **SPDC** (spontaneous parametric down-conversion) using powerful laser single photons source heralding with a probabilistic outcome that is detected post-selectively and doesn't scale well beyond a dozen qubits [2722], atom based **cavity QED** generation [2723] with a record 14 qubits GHZ state [2721] (Figure 305) that was later extended to **ensemble of Rydberg atoms** [2724, 2725], with **diamond color centers** [2726], with connected **coupled cavity arrays** (CCAs) [2727], individual **neutral atoms**, **spin-photon entanglement** to deterministically generate linear cluster states aka the Lindner-Rudolph protocol [2728–2730] with improvements on high photon indistinguishability [2731] and three qubits cluster state generation [2732], with **quantum dots molecules** [2733], with the **entanglement of several single photon sources** [2734, 2735], **time-domain multiplexing** using indistinguishable photon sources which has the advantage to be theoretically unlimited [2586, 2736–2738], **2D spin-photon** cluster states [2536, 2739], creating **large GHZ states** using regular linear optics [2740], etc. You can also add **spectral domain multiplexing** on top of time-domain multiplexing as a complement to SPDC sources [2741] or with propagating modes generated in a nonlinear $\chi^{(2)}$ photonic lattice made of nonlinear

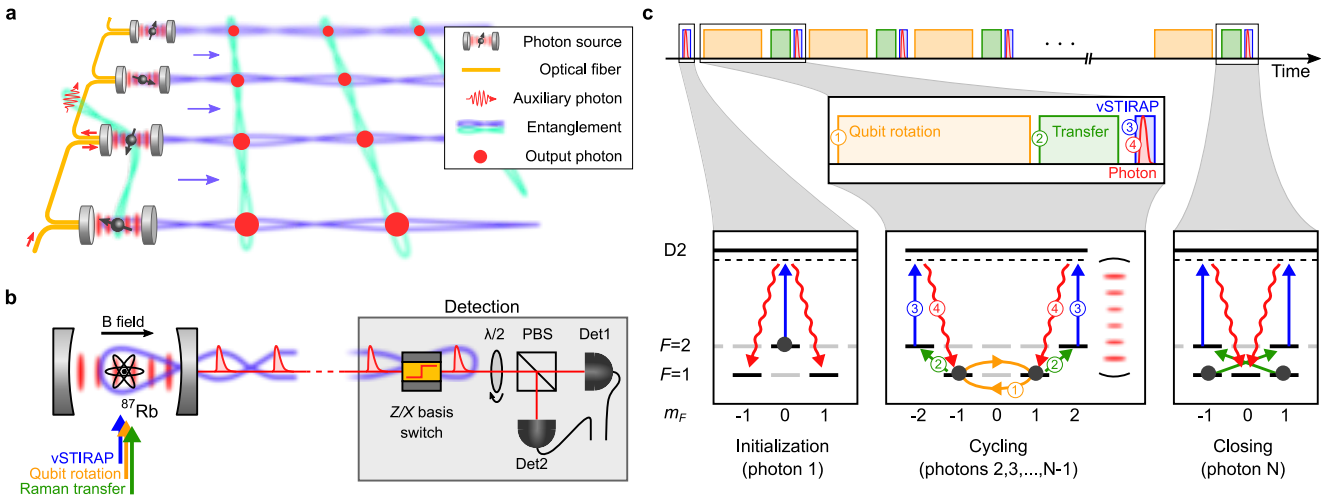


Figure 305: One solution to generate a cluster state of entangled photons for MBQC with a reported 12-photon entangled cluster state in 2022. The state generation and detection conditions should be stated alongside the photon count. Sources: [2721].

waveguide arrays in continuous variables for the creation of two and three dimensional cluster states [99]. You can also generate cluster states with superconducting qubits as Yasunobu Nakamura's team at RIKEN and the University of Tokyo did in 2025 [2742] and Jian-Wei Pan's teams did also in 2025 with the Zuchongzhi 3.0 105-qubit QPU, creating 95-qubit one-dimensional and 72-qubit two-dimensional entangled cluster states, although its applicability for actual MBQC computing remains elusive [2743].

- Measuring **state of intermediate qubits** during computing (M). It is carried out with a variation of projective measurement. It consists of first applying one or more X or Y gates to a qubit to create a rotation in their Bloch sphere and then measuring their state on the computational basis. It is a bit like rotating the Z ($|0\rangle/|1\rangle$) axis in the Bloch sphere to change the reference point.

$$|\pm\rangle = \frac{|0\rangle \pm |1\rangle}{\sqrt{2}} \qquad |\pm_\alpha\rangle = \frac{|0\rangle \pm e^{i\alpha}|1\rangle}{\sqrt{2}}$$

- The projective measurement basis is in the form of states of the type $|\pm_\alpha\rangle$, α being generally a half or quarter turn in Bloch's sphere. A measured qubit is always an intermediate resource and is not an output resource. This helps obtaining some information that can be used to manipulate the qubits afterwards to propagate computation. Projective Z measurements have the effect of removing the measured qubits from the cluster.

- These successive **corrections** make computing deterministic (step C) with X and Z gates. They are applied according to the result of the projective measurements made in (M). No correction gate acts here on a qubit already measured. This model makes it possible to apply any gate to a qubit which is in fact a combination of Rz(γ)Rx(β)Rz(α), i.e., rotations around the three axes of the Bloch sphere of angles γ, β and α.

What has just been described makes it possible to interpret the lower right-hand part of the illustration in Figure 306 which explains how the MBQC equivalents of the CNOT (two-qubit), H or S quantum gate equivalents are realized in MBQC. Each X or Y circle is an X and Y projective measurement that combines an X or Y gate followed by a qubit readout. The result conditions the type of projective measurement performed immediately afterwards in the order indicated (1 to 15 and 1 to 5).

Two forms of measurements affect the inner working of the qubit matrix: Z measurements separate the qubits by digging sort of grooves in the qubit matrix, a bit like Pacmans, then classical measurements along the "wires" or on the "bridges" between these wires simulate single-qubit gates like Hadamard's and the two-qubit CNOT gates. The sequence of operations depends on the result of each measurement along the wires. The computation result is located in the last qubits whose state is not yet measured and which will be measured last.

This combination of NEMC sequences allows the reproduction of the operation of one- and two-qubit quantum gates. A complete quantum computation is a sequence of multiple NEMCs that ends with the measurement of the state of the remaining qubits!

The consequences of what we have just seen are multiple:

- MBQC requires way **more qubits** than in a conventional circuit-based model. We've seen that a single X or Y gate results from the combination of four X and Y gates and as many measurements. This in turn creates some "pressure" on the classical part of the calculation, linked to the measurement.

- MBQC still requires **error correction codes** such as foliated quantum codes [2745, 2746]. They multiply

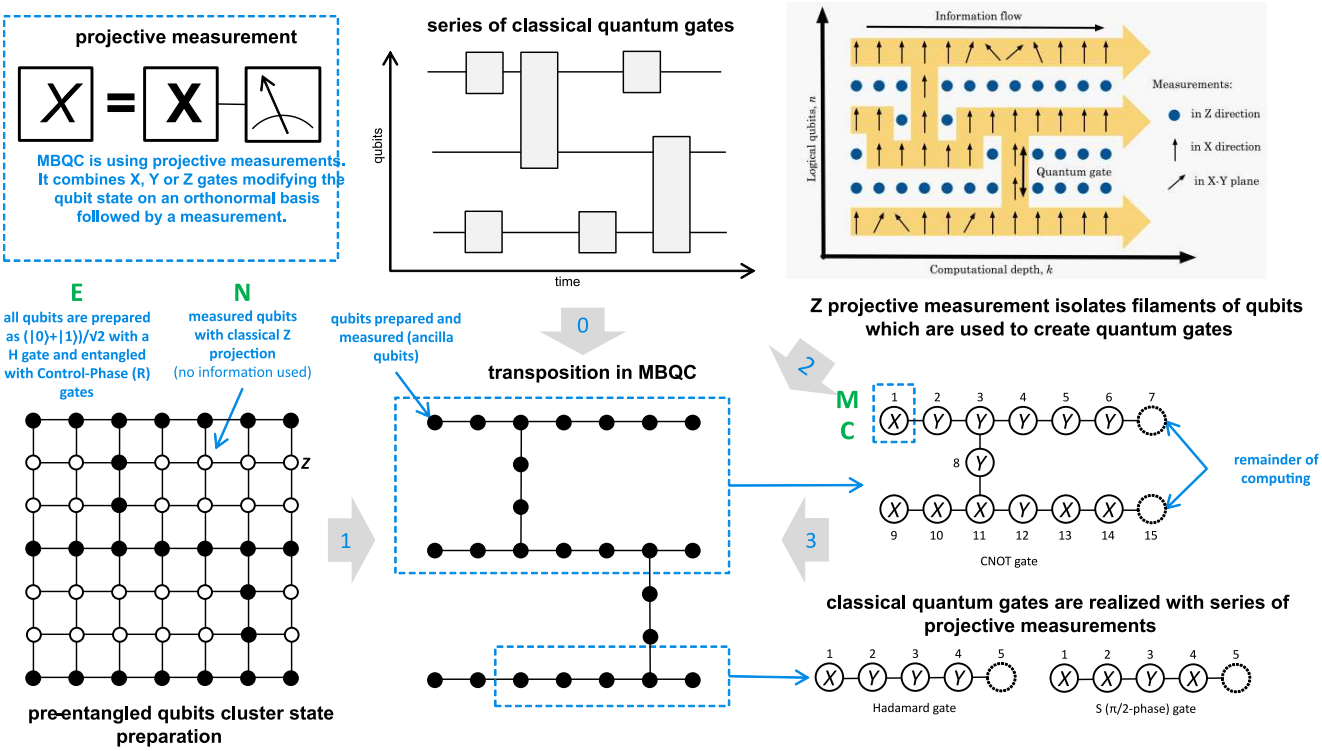


Figure 306: Tentative summary of how MBQC works. The resource state is progressively consumed by measurement and cannot be reused. Compilation, Olivier Ezratty, 2021, and [2744].

by several orders of magnitude the number of physical qubits necessary for computing any algorithm. It could be facilitated if we could organize the qubits in 3D matrices, the third dimension being used to align the qubits necessary for error correction, especially with surface codes. Since MBQC models contain their own error correction mechanisms, it may be less demanding in terms of additional qubits for error correction necessary for the creation of FTQC [2747].

- An MBQC model is easily exploitable to take advantage of teleportation and **distributed quantum computing** algorithms. Cluster states will be able to be linked together via remote optical links. It is also one of the tools of blind computing [2748].

- The **temporal dimension** of computing is modified compared to classical gate-based quantum computing. As we can parallelize operations coupling gates and measurements, MBQC is a bit like Nutella on the breadcrumbs: we can spread it out! The depth of the available computation is no longer linked to the ability to chain quantum gates in time as in the middle-high diagram in the previous illustration, but to execute a large number of them in parallel over a very large number of qubits (modulo the required error correction). The sequences of measurements labeled 1, 2 ... n will be carried out simultaneously in groups 1, 2 ... n, n being limited to 15. Therefore, the required physical calculation depth is defined by the maximum number of physical gates to execute to create a CNOT. An algorithm depth no longer depends on the ability to chain quantum gates with one and two qubits, but on the capacity to create large entanglement states. In short, sequential quantum computing is replaced by massively parallel quantum computing with a very shallow depth [2749].

- The **FBQC variant** associates a MQBC model with small cluster states and probabilistic gates, aka "fusion gates" between these clusters [102]. It is the PsiQuantum path and is also studied in several other places like at NBI in Denmark [2750, 2751], which published a full-fledged FBQC architecture in 2025 using quantum dot single photon sources [2752, 2753] (Peter Lodahl, Anders Søndberg Sørensen, and Stefano Paesani) (Figure 307), and in Russia [2754, 2755].

- There is some connection between the MBQC and the **ZX Calculus**. ZX Calculus is a graph model that helps formalize MBQC, its cluster states and the associated error corrections [2756]. ZX Calculus can also help convert regular gate-based algorithms in a version adapted to MBQC [2757].

- **Algorithms** are specific to this kind of architecture [2758]. It is not yet experimental because it requires a large number of qubits that are not yet practically available. Still, QAOA could easily be translated into the MBQC formalism [2759]. There is also a proposal for some variational generative model using MBQC [2760].

MBQC has a flavor developed by Dong-Sheng Wang in Beijing, China, himself a former collaborator of

Experimental error source	Error model	N	Maximum tolerable threshold	Required experimental benchmark
General loss	Uncorrelated loss	8	8% [Fig. 8b(i)]	$\eta > 92\%$
Branching (finite cyclicity)	Spin-photon X errors	6	0.174% [Fig. 8b(iii)]	$C > 574$
Emitter-emitter distinguishability (slow spectral diffusion)	Distinguishability	8	4% [Fig. 8b(v)]	$V_{\mathrm{HOM}}^{ee} > 96\%$
Single-emitter distinguishability (fast pure phonon dephasing)	Photon Z errors	8	0.57% [Fig. 8b(vi)]	$V_{\mathrm{HOM}}^{se} > 99.4\%$
Optical excitation errors	Distinguishability	8	4% [Fig. 8b(i)]	$V_{\mathrm{HOM}}^{ee} > 96\%$
Laser-induced spin-flips during spin control	Loss & spin depolarisation errors	7	0.6% [Fig. 8b(ii)]	$\bar{\kappa} < 1.08 \times 10^{-2}$
Finite T_2 (Markovian spin depolarisation)	Spin $X/Z/Y$ errors	7	0.36% [Fig. 8b(iv)]	$T_2 > 417\tau_{\mathrm{rep}}$
Markovian ground-state dephasing (Overhauser noise)	Spin Z errors	10	0.6% [Fig. 8b(ii)]	$T_2^* > 56\tau_{\mathrm{round}}$
Blinking	Correlated loss	8	6.1% [Fig. 8b(vii)]	$P_A/P_D > 15.4$

Figure 307: NBI and Sparrow Quantum made a full-fledged FBQC architecture proposal using single photon emitter quantum dots in 2025. It lists in this table various figures of merit that should be obtained to render the proposal viable. How do these numbers compare with state of the art? Most of them are attainable. Two are very difficult to obtain, particularly the first line which covers photon losses. Current coupling loss in optical fibers is about 3 dB while the total losses shouldn't exceed the required 0.362 dB threshold corresponding to η>92%. The second harder figure of merit is the branching error which is currently at about 36 and should reach 574. It is the number of correct excitation-emission cycles a quantum dot can undergo before a branching error or photon loss occurs. Also, NBI's architecture favors photon time-bin encoding instead of polarization encoding, the choice of Quandela, to avoid the need for very fast optical switching. Source: [2752]. Color code: Olivier Ezratty, based on the difficulty to reach these thresholds.

Raussendorf [2761, 2762], using different names like "quantum von Neumann architecture" [2763] and "transistor-based quantum computing" [2764]. It encodes operations rather than quantum states in hardware. Each elementary gate is a finite chain or ladder whose ground state lies in a $Z_2 \times Z_2$ symmetry-protected topological phase, with the two edge modes serving as input and output ports and the bulk as a control port, which justifies the transistor analogy. There are however so many conflicting hardware assumptions in the model that it's very hard to figure out on which physical substrate this model could be built on, besides it relying on matter qubits (cold atoms qubits, superconducting qubits, semiconductor spin qubits, Majorana qubits).

1.10.7 Vendors

PsiQuantum

USA, 2015, $2.32B

PsiQuantum is a startup which is developing photon-based FTQC systems using CMOS silicon technology.

Company. The company was created by Jeremy O'Brien, a former University of Queensland and Bristol University researcher, Pete Shadbolt (co-inventor of the VQE algorithm with Jeremy O'Brien and Alán Aspuru-Guzik), Mark Thompson and Terry Rudolph (who discovered when he finished his physics thesis that he was a grandson of Erwin Schrödinger). As of mid-2026, the company employed about 650 people scattered across Palo Alto and Chicago in the USA, in the UK, in Australia, with some of them working remotely all over the world, including a couple ones in Europe. In February 2026, Victor Peng, a former president at AMD, became interim CEO and was later confirmed in the role, while Jeremy O'Brien, who had been the CEO since the company creation, became Executive Chairman.

Funding. PsiQuantum is one of the best funded startups in the world in quantum computing, on par with IonQ and its 2021 SPAC. Originally from the United Kingdom, it moved part of the team to the USA [2765, 2766]. They even have Microsoft as investors as well as Pascal Cagni's investment fund, C4 Ventures. Their last funding round of $450M in July 2021 cemented this funding lead, followed by a $1B round in September 2025. Then, we have the amazing April 2024 deal in Australia, which we describe later. And in March 2025, there were unconfirmed rumors that PsiQuantum was raising an additional $750M. It became a new round of $1B announced in September 2025 at a valuation of $7B, led by BlackRock, Temasek and Baillie Gifford,

with Nvidia's NVentures among the new investors. A further $1.5B round at a $10.5B valuation was reported in May 2026 and is worth confirming.

FBQC. Early in 2021, the company started to describe its photonic-based technology [2767]. It published a paper describing their qubit architecture using an FBQC approach, *aka* fusion-based quantum computation, a variant of MBQC that we studied earlier in 1.10.6. It uses micro clusters states with groups of 4 qubits connected with each other and using Resource State Generators (RSGs) (Figure 308 and Figure 309). It is replacing measurement of entangled states by double measurement of non-connected adjacent qubits to create entanglements between them [2768]. Qubits are encoded in path, using dual rail encoding with lines for photon states $|0\rangle$ and $|1\rangle$.

The PsiQuantum architecture is full of non-deterministic operations, particularly at the cluster states generation level and in the fusion gates themselves. It makes it hard to assess its viability although many PsiQuantum's paper raw estimates tend to demonstrate it could operate efficiently [2768]. Two-qubit gates use XX nondeterministic and ZZ deterministic measurements (measuring two photons simultaneously with the same polarization basis), implemented with a beam splitter then combining fusions to create small cluster states. With that, the qubit computing depth is quite shallow, avoiding the pitfalls of qubits error rates. It is replaced by a large breadth of computing and commutative operations, replacing "depth-computing" by "breadth-computing" [55, 2769, 2770].

PsiQuantum's ambition is to produce one million physical qubits system supporting the equivalent of 100 logical qubits and an undisclosed number of gates. They need at least two types of silicon chips, one containing their photon sources, FBQC engine and photon detectors, which operate at a cryogenic temperature of 2K and the other using BTO, supporting photon routing between chips and operating at room temperature. Both chips are manufactured on 300 mm wafers by **GlobalFoundries** in their Luther Forest Technology Campus, upstate New York. They also rely on **Dolphin Semiconductor** (France) for the development of cryo-CMOS hybrid analog-digital electronic components used amplifying and converting the analog signals coming out of their PNRDs.

They announced the production of a first q1 chip sample in April 2021, integrating tens of thousands single (non-deterministic "spontaneous parametric downconversion" *aka* SPDC) photon sources and detectors [2772]. Their physical architecture is using sandwiches assembling a 22 nm CMOS electronic chip of 750M transistors using superconducting nanowires bonded with 100K connections to a photonic chip containing thousands of photon sources, detectors, and other optical devices. Each photonic chip has more than 1,000 electrical connections for the control of their phase shifters and 200 optical fiber entries and exits used to interconnect similar photonic chips together.

PsiQuantum published various papers on the practical implementation of their FBQC model, like on the ways to reduce its resources requirements [2773], to reduce the Shor 2048-bit algorithm circuit size and run-time using their Active Volume Architecture (AVA) [2774, 2775], with the creation of a scalable framework for decoding in real time the streams of classical data in the decoder, used in quantum error correction, using parallelizable real-time decoding [2776], and how to deal with probabilistic single photon sources and gates [2777, 2778]. Active Volume is an architectural and compilation framework introduced by Naomi Nickerson and Daniel Litinski which reduces the hardware resources and runtime required to execute large-scale quantum circuits by exploiting non-local connectivity.

In April 2024, PsiQuantum released an arXiv preprint which became a Nature paper in February 2025 [53], describing their chip manufacturing and characterization. It highlighted in its introduction very good fidelities for photon generation, single and two-qubit gates: "*99.98% ± 0.01% state preparation and measurement fidelity, Hong-Ou-Mandel quantum interference between independent photon sources with 99.50% ± 0.25% visibility, two-qubit fusion with 99.22% ± 0.12% fidelity, and a chip-to-chip qubit interconnect with 99.72% ± 0.04% fidelity*". Some shortcomings are with their photon detection rate of only 89% and with many losses in the waveguide circuits. The paper then listed their many scientific and technical challenges to overcome and elements of their roadmap including new cascaded resonator photon sources, low-loss silicon nitride waveguides and components (SiN), high-speed and low-loss barium titanate electro-optic phase shifters (BTO) which are built on strontium-based substrates (strontium titanate or $SrTiO_3$) that was codeveloped with the U.S. Air Force Research Laboratory (AFRL), fiber-to-chip optical coupling loss, and complex N×M networks optical switches (these are large chips with a 300 BTO wafer holding 48 of them, operating at room temperature), directional couplers and crossings, low-loss chip-to-fiber coupling and high-efficiency photon-number-resolving photon-number resolution detectors (PNRDs) using spatial multiplexing of many SNSPD-like detectors. There are probably some other challenges ahead like with the classical computing capacity for decoding and feedforward handling. Their roadmap said that all of this could be implemented, tested and industrialized in six years, which seems overoptimistic.

The Nature paper contained some updates and supplemental materials [53] with the photonic chip nicknamed Omega [2779]. One interesting advance came from the PNRD (multiple photon detectors) which operate at 2.1K and showcases an efficiency of 96%. But it seems they need to further improve it to implement FBQC. One Omega chip seems to contain 750 million transis-

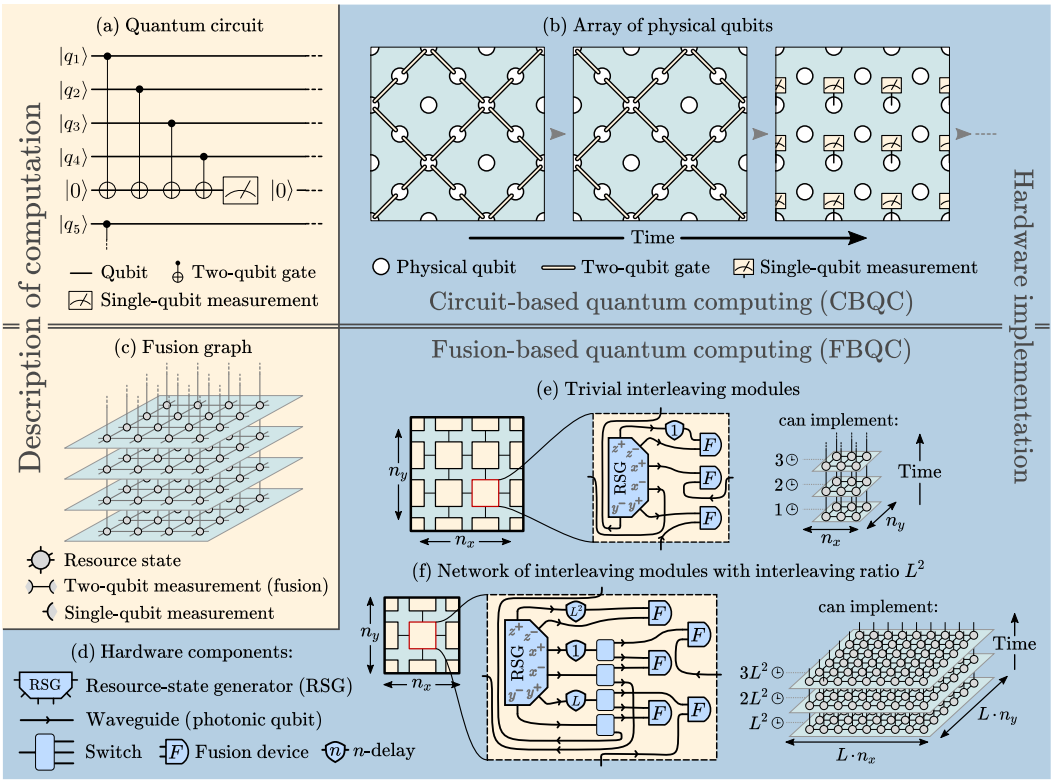


Figure 308: FBQC method description. Source: [2771].

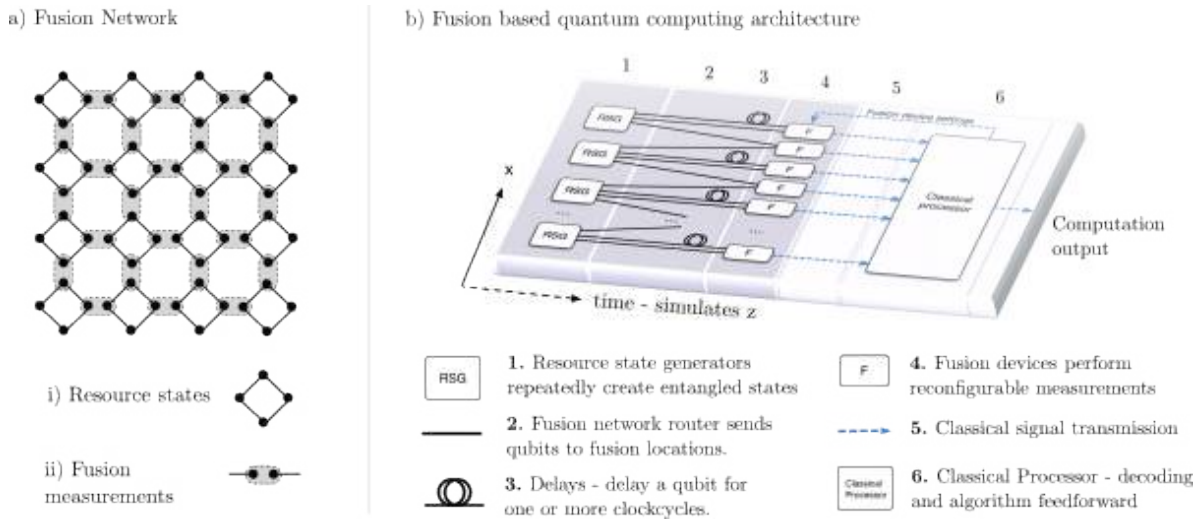


Figure 309: Physical description of the PsiQuantum FBQC architecture. Small cluster states of 4 entangled photons are generated (RSG) with the photons being dynamically routed into "fusion devices" which implement non-deterministic two-qubit gates between photons from separate cluster states. In between, delay lines can enable the routing of resource states generated at different moments. Classical processing is exploiting the results from the measurements in fusion devices. Their Si / Si_3N_4 and SiO_2 based spontaneous four-wave mixing (SFWM) single-photon sources are driven by a pulsed laser pump. The generation of a single photon is probabilistic and heralded by the detection of its pair. Their current photon detectors are superconducting nanowire single-photon detectors (SNSPDs), using a niobium nitride (NbN) layer. PsiQuantum will later replace it with photon-number-resolving detectors. Source: [53, 55].

tors, including 0.5GB of integrated SRAM, and with a thermal dissipation of 0.5 W.

In June 2025, the Nature paper was complemented by an arXiv describing the photon losses tolerable in their FBQC architecture with the Loss Per Photon Threshold (LPPT) [51]. With improved error correction codes, they can increase the LPPT from 1% to 18.8%, but this has an overhead cost in the resource states preparation with non-deterministic 3-photon GHZ sources.

In June 2025, Daniel Litinski (their "Craig Gidney") proposed the blocklet concatenation architecture, an FTQC protocol optimized for FBQC that abandons strict 2D

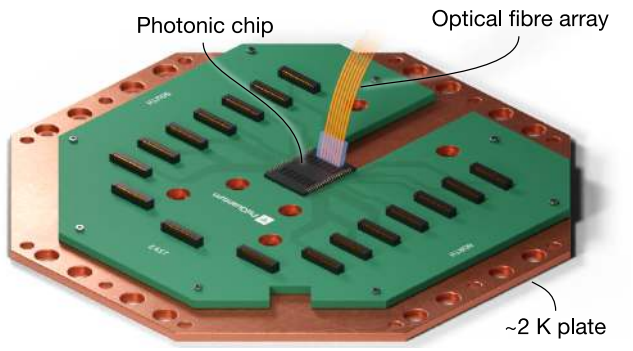


Figure 310: The main PsiQuantum chip as of 2025. Source: [53].

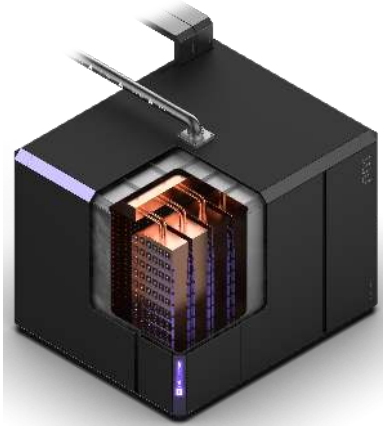


Figure 311: PsiQuantum cabinet conceptual view. Source: PsiQuantum web site as of July 2025.

locality constraints and uses code concatenation and transversal gates. It however requires larger resource states of 8 to 12 entangled photons. It benefits from high erasure thresholds of up to 19.1% while lowering the number of photons per logical qubit [2780]. They also explained how they plan to generate magic states in 2024 [2781].

Cryogenics. The PsiQuantum one million physical qubits computer will be made of thousands of computing chips. PsiQuantum's marketing message is to tout that their chips don't need the 15 mK cryogenics of superconducting qubits. They indeed need "only" 2 K cryogenics to cool their silicon chips [53] (Figure 310).

The temperature is higher but PsiQuantum's cryogenic cost is of unprecedented size, with about 50 MW needed for the support of an unspecified number of logical qubits and circuit size. PsiQuantum estimates that its systems will have a total power drain of 100 MW, with one in Brisbane and three in Chicago [2782–2784]. This corresponds to more than three times the roughly 30 MW peak draw of El Capitan, the largest supercomputer in the world.

Multiple chips are to be integrated into "cabinets" that are cooled with liquid helium. They did build several prototype cabinets with the PsiCube hosting 10 chips (10 W cooling power at 2.3K, Figure 312), the MK1 hosting 50 chips (30 W cooling power at 2.3K), and the MK2 hosting 40 blades and over 100 chips (50 W of cooling power at 2.3K, developed in Minnesota, Figure 313). Ultimately, production cabinets will need a cooling power of 360 W for hosting about 250 chips and their cryo-CMOS friends [2785, 2786]. At least 100 of these cabinets will be needed although PsiQuantum visual indicate that multiple hundreds of them may be needed for production scale FTQC systems [2787].

Cryogenics is based on a giant liquid helium farm built by Linde (Germany) which will generate a continuous stream of 4.5 K liquid helium. This stream must then cooled at about 2K by additional sub-atmospheric cold boxes not far from the cabinets. The electricity bill is then completed by the laser, control electronics and quantum error correction classical computing costs, which are unspecified.

UK. The company opened a UK R&D facility in March 2023 that is dedicated to the development of large scale cryogenic solutions. It is located at STFC's Daresbury Laboratory in the north-west of England where they access a large liquid-helium cryogenic plant providing about 100W of cooling power at about 3K. As part of this, they benefited from UK's government funding in the tune of £9M.

Australia. In April 2024, the Australian government and the region of Queensland signed a deal with PsiQuantum, involving a dilutive and non-dilutive (loans, grants) investment of AU$940M, about US$617M at the time to fund the establishment of their regional APAC office and a manufacturing plant in Brisbane [2788]. PsiQuantum promised that this investment would drive the creation of 400 direct and 4,000 indirect jobs plus $5B of economic value in the country. The deal is about creating new premises and not relocating their existing US and UK employees. The Australian government is mentioning that the BCG estimates that investing in the "*world's first commercial-scale fault-tolerant quantum computer could lead to up to an additional $48B in GDP and 240,000 new jobs in Australia by 2040*", a clear political overpromise. PsiQuantum will create a research center dedicated to finding quantum computing case studies related to climate change. It also partners with local universities [2789]. The Australian decision has been controversial among local quantum groups. The shadow cabinet of the opposition to the Labor party spurred the launch of an inquiry due to the lack of a fair and open tender process [2790–2792].

Other players like Diraq were of course quite frustrated by this move of their own government which didn't even consult their quantum scientific council before making such an important decision. This government intervention is unprecedented in size and is not even matched by

Figure 312: PsiCube, the first PsiQuantum prototype cabinet cooled with liquid helium with a cooling power of 10W at 2.3K.

Figure 313: PsiQuantum prototype Mk2 cabinet hosting 100 Omega chips and cooled with liquid helium with a cooling power of about 50W at 2.3K.

any private investment, either from venture capital or even from PsiQuantum itself. This investment followed sustained advocacy by PsiQuantum. It commissioned a study to Mandala Partners, an Australian analyst firm to justify the non-competitive choice of PsiQuantum [2793, 2794].

Figure 314: PsiQuantum map of their upcoming Brisbane facility with a cryoplant, a compute building to host their 100 logical qubit QPU, a research and office building. Right, two cryogenic casing for PsiQuantum's QPU. Construction began in June 2026 after over a year of delay. The Linde cryoplant will be installed in mid-2027 and the first cabinets afterwards. Source: [2795].

PsiQuantum had started this lobbying effort back in 2020, reaching out to many countries including EU member states like France and Germany. Jeremy O'Brien was asking for €500M in loans and grants to establish its headquarters in the EU. No country, of course, could afford to make such a large bet, at the expense of its local quantum ecosystem. The Australian government investment in PsiQuantum's establishment in the country is the equivalent of the total country investment in quantum science and technology over the last 20 years. No serious quantum scientist would make such a bet at the expense of all other qubit modalities. PsiQuantum participated to the creation of the Queensland's Quantum Decarbonisation Alliance (QDA) with QUBIC (the Australian Research Council Centre of Excellence in Quantum Biotechnology) [2796].

Figure 315: PsiQuantum map of their Chicago site which will host a prototype FTQC system (on the right) and then, three full-size FTQC systems. Construction began in 2026. Source: [2783].

Chicago. Days after the Australia's deal announcement, there was some talks about a project to create a "$20B"

quantum campus in Chicago that would be anchored by…PsiQuantum, which would create 500 direct jobs. The site is to host a cryogenic facility costing between $300M and $500M [2797, 2798]. This project was officialized in July 2024 with the announcement of the creation of a PsiQuantum site at the newly created Illinois Quantum and Microelectronics Park (IQMP) that includes the University of Illinois Urbana-Champaign, the University of Chicago, the Chicago Quantum Exchange, the DoE Argonne and Fermi National Laboratories and DARPA [2799]. They plan to build a full-blown datacenter, after the first one in Brisbane which will host a prototype system and three full-sized systems. Illinois is investing $500M for the campus development including an undisclosed share for the cryoplant buildup, plus a tax incentive package of $500M over the course of 30 years. DARPA is setting up its Quantum Benchmarking Initiative (QBI) at the new park with a $140M investment and a matching $140M funding from Illinois.

Software. PsiQuantum developed its own quantum resource estimator, Bartiq, in connection with their QREF (quantum resource estimator format) [2800] and a proposal to reduce the number of required logical qubits to run some chemical simulations [2801]. They also estimated the resources to implement chemical catalyzis dynamic simulations [2802]. In September 2025, PsiQuantum launched Construct through an early-access program, its software platform for designing, developing, and optimizing FTQC algorithms targeting its future QPUs. It contains Circuit Designer, a visual editor for prototyping and documenting large quantum circuits, Workbench, a Python library for creating algorithms with billions of operations on hundreds of logical qubits, and their Resource Analyzer, probably derived from Bartiq. All this is integrated in a Quantum Development Environment. It added the support of Nvidia CUDA in 2026 with 450× speedup compared to using only CPUs. They also proposed ways to reduce the cost of running a QPE at the Toffoli count level [2803].

Case studies. All case studies published by PsiQuantum are resource estimates for large FTQC QPUs with thousands of logical qubits and very large circuits, mostly in chemical simulations, like for the work they do with **Mitsubishi** [2804]. They also work with **Boehringer Ingelheim Pharma** on quantum chemistry [2805], with **National Cancer Center Japan**, and with **Airbus** with a focus on computational fluid dynamics [2806].

Customers. At this point in time, no visible customer has declared some interest in acquiring a PsiQuantum QPU given its planned price sits in the $1B zone. DARPA selected PsiQuantum in January 2025 in the second phase of its Utility-Scale Quantum Computing (US2QC) program. As part of this program, PsiQuantum got a DARPA funding of $31.8M in September 2025 plus $125M in July 2026. In October 2022, it also got a $22.5M contract from the US Air Force Research Laboratory, followed in April 2025 by an extension of $10.8M to help AFRL develop custom chips reusing the Omega chip and its barium titanate electro-optic technology.

Xanadu Quantum Technologies

Canada, 2016, $619M

Xanadu is a startup created by Christian Weedbrook, a prolific researcher having started at MIT and the University of Toronto, among others.

Company. They were 245 as of March 2026, a stable headcount since 2024. The company was introduced at the Nasdaq in March 2026 after a SPAC, which brought them $302M of additional funding. They were also planning some funding by the Government of Canada for $274M. It followed a Canadian federal government investment of about €27M in January 2023 [2807] and in February 2023, with a grant of CAD $3.75M from the Ontario region to develop quantum research and education. It led to the opening in June 2025 of a $10M photonic packaging facility in Toronto. It was extended in August 2026 with the project OPTIMISM funded by the Canadian government for CAN $195M, which is about the Inception 14.7K m^2 photonic circuits research, manufacturing and assembly facility.

Technology. The startup is developing a photon qubit quantum computer targeting FTQC capabilities. In September 2020, they launched a cloud-based testing platform of 8 and 12 qubits. Their qubits are qumodes based on squeezed states using continuous variables encoding. Their work and research are rather well documented with over 100 published papers [2808–2812].

The 8-qubit silicon-nitride chip from their X-Series QPUs is 4mm × 10 mm wide, fed by infrared laser pulses and generating "squeezed states" superposing multiple photons, then flowing through an interferometer made of beam splitters and phase shifters performing quantum gates, and exiting to superconducting photon detectors [2813]. Their photon sources and photon detectors require some cooling. Their currently used superconducting transition edge sensor (TES) photon counting detectors are operating at about 100 mK, which does require a dilution refrigerator and is a real caveat to the "photonics runs warm" argument [2814]. They plan to later use room-temperature detectors using SPADs (single photon avalanche diodes) and QFC (quantum frequency conversion) [2815]. Later, they may use photon number resolving detectors (PNRD) for both Gaussian Boson Sampling (GBS) and for the preparation of non-Gaussian GKP states, cat states and NOON states which combine N quantum objects in the $|0\rangle$ state and as many in the $|1\rangle$ state [2816].

In 2021, a team of Xanadu and Canadian researchers published a blueprint with more details on the Xanadu FTQC architecture. It is based on MBQC and three-dimensional resource states comprising both GKP bosonic qubits and squeezed states of light. This hy-

bridization would enable the implementation of both Clifford and non-Clifford gates, all of this running on 2D photonic chips [2817, 2818].

In June 2022, Xanadu announced their own quantum advantage with their own gaussian boson sampling architecture (GBS). Their Borealis QPU reached a record of 216 photon modes by using frequency multiplexing and delay lines implementing time-bin multiplexing.

Their system was programmable with parametrizable photon phases, and it was put online on the cloud on Amazon Bracket. However, Xanadu was cautious in saying that it didn't yet find use case with some useful quantum advantage [2819], but later, proved that it could bring some quantum advantage [2820].

In January 2025, Xanadu presented Aurora, its first distributed quantum computing platform. The prototype uses interconnected racks with a total of 35 photonic chips, fibre-optic interconnects, 84 squeezers and 36 PNRDs supporting a total of 12 physical qubit modes [169] (Figure 316). It supports creation of a photonic cluster state of 86.4 billion modes. They are also working, alongside with Hyperlight (2018, USA), on improving thin-film lithium niobate (TFLN) photonic chips that waveguide reduce losses.

Roadmap. When they announced their SPAC in September 2025, Xanadu said it planned to support 1,000 logical qubits with about 100,000 physical qubits by 2029 [2821]. In August 2026, the deadline was postponed to 2031, but with the ambitious goal to support logical error rates of 10^{-16} [21].

Manufacturing. In August 2021, Xanadu announced that their FTQC silicon-nitride chips would be manufactured by IMEC in Belgium but in March 2022, they switched gear and announced a partnership with GlobalFoundries for the manufacturing of their chip on 300 mm silicon wafers, like PsiQuantum. Xanadu is relying on other cleanrooms to built their chips with the Albany Nanotech from NY Creates, as well as Tower Semi-conductors for III/V chips, UMC, and IME. They expect to scale up to 1,000 logical qubits, which would require tens of thousands of racks, with increasing their chip density by two orders of magnitude compared to their Aurora prototype. It is so large that they plan to accommodate all these racks in a 40-floors building. This FTQC system may need several tens of megawatts of electricity power. But they also plan to significantly reduce photon losses from 24% to 1%, which could reduce their hardware footprint.

Software. Xanadu develops the open-source software platform **Strawberry Fields** and **PennyLane** in Python [2822]. It is quite popular, just after Qiskit. It includes the Blackbird language and targets chemistry use cases, graph theory problems and quantum machine learning. Their main application is the analysis of similarities between graphs to identify those that are similar and/or separate them into several classes of similarity. Classical methods for solving this kind of problem are similar to finding a matrix determinant [2823]. Xanadu is also developing its own QEC codes [2824]. It also believes strongly that quantum computing can bring value in the field of quantum machine learning [2825].

Error correction. Xanadu is studying qLDPC QEC on their GKP photonic qubits which are using homological measurements [2826–2829]. Homological measurements detect and correct errors by looking at the global topological properties of quantum states, rather than local qubit states. It is used with topological QEC codes like the surface code where logical qubits are encoded across many physical qubits. Homological measurements detect changes in the topology caused by errors, such as loops formed by qubit flips or defects on the lattice. These measurements help identify non-trivial topological features, allowing error correction by assessing the global state of the system rather than qubits X and Z parity errors. In March and June 2025, they provided more scientific details on their error correction schemes, always based on GKP codes [2830, 2831]. In 2026, they proposed a way to save about 50% of the Toffoli gates needed in an FTQC circuits using a QROM, a coherent table lookup technique used in many circuits like a QPE [2832].

Case studies. On the customer side, Xanadu is like most vendors in a hurry to display some practical use cases for their systems. They are partnering with **BMW** on machine learning use cases, with prototypes using only four qubits and therefore far below a scale associated with computational advantage [2833, 2834] and with **Volkswagen** and 1Qbit to simulate lithium-ion batteries Li_2FeSiO_4 oxides, which would require 2,375 to 6,652 logical qubits that are about 10 years away in Xanadu's roadmap [2835]. In 2026, they published a paper with resource estimates to simulate photoreactivity in cancer-targeted photosensitizers, landing with a requirement of 180 to 350 logical qubits and up to 10^9 Toffoli gates [2836].

Partnerships. In January 2023, Xanadu announced a partnership with **KAIST** (Korea Advanced Institute of Science and Technology) in South Korea with the aim to create quantum algorithms for designing next-generation lithium-ion batteries, a rather long-term goal given it indeed sits in the FTQC realm [2837]. In September 2023, this partnership was extended "*to train and educate South Korea's future quantum workforce*". They are partnering with **Entropica Labs** from Singapore for the development of their QEC/FTQC platform, using Entropica's EKA, a library preserving the context of low-level QEC instructions. Finally, **Applied Materials** helps them since 2025 to develop a 300 mm wafer process for the production of superconducting transition edge sensors (TESs) which are used in Xanadu's photon-number resolving detectors (PNRDs).

Quandela

France, 2017, €67.5M

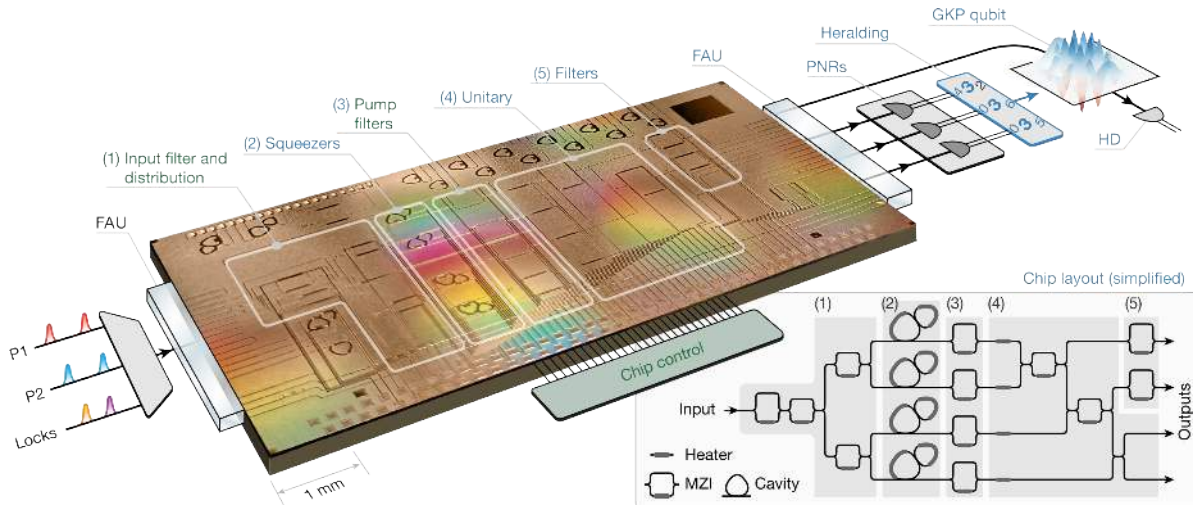


Figure 316: Xanadu's PIC architecture. Source: [169].

Quandela decided in 2020 to expand its historical single photon source activity to create photon qubits computers as part of their project ROQC (Reconfigurable Optical Quantum Computer). Quandela is always teaming up with Pascale Senellart's C2N research team in Palaiseau, France. They have a research office in Munich, and a new site established in Montréal since 2024, related to their partnership with Exaion, a data center and cloud infrastructure operator. As of March 2026, the company had a staff of 140 people.

Technology. Quandela is using discrete variable photons encoding with three different models in its existing NISQ offering:

- A **KLM probabilistic model** using dual rail Fock states as shown in Figure 322 [2838–2840].
- A **native photons model** using a larger Hilbert space enabled by photon Fock states where data can be encoded with zero, one or more photons, in sorts of qudits (they call this qubit logic on qudits or QLOQ). This enables efficient circuit compression that can save orders of magnitude in computing time for NISQ algorithms like a VQE [2841], but not necessarily in a quantum advantage regime.
- A **boson sampler model** which they plan to use for quantum reservoir computing. In 2025, they published a preprint on the optimization of a linear optical circuit for NISQ operations with reducing the number of MZI (interferometers) to run a boson sampling on n<50 photons and n«m, m being the number of photon modes (dimensionality) [2842]. In 2026, they demonstrated that their boson sampling could theoretically show an energetic advantage before a computational advantage, although with no input data [2843].

In February 2022, Rawad Mezher and Shane Mansfield from Quandela proposed a single-number benchmark metric, the Photonic Quality Factor (PQF), defined as the largest number of input photons for which the output statistics pass all tests. It covers photons quantum computing using single photon sources, multi-mode linear optics and photon detectors, including boson sampling experiments [2844].

With Fabio Sciarrino's team from Sapienza University in Rome, Italy, they developed an interferometer to assess the indistinguishability of 4 entangled photons generated by their quantum dots source, as shown in Figure 319 [2845].

Quandela is also participating in various collaborative projects, the EPIQUE EU project [2846] and the OQuLus project in France [2847].

Figure 317: Quandela Belenos with 12 qubits, released in 2025 and delivered under the nickname "Lucy" to CEA TGCC in 2026. Photo: Quandela.

NISQ hardware. Their first QPU was MosaiQ, with 2 to 12 photon modes and consuming 1 kW. It was first deployed online in November 2022. Ascella, their 6-photon and 12-mode QPU, was their first publicly available QPU online. They launched Belenos in 2025, a 12-qubit photonic QPU. Such a system was deployed at TGCC as part of the EuroHPC program in 2026, under the name "Lucy". It consumes only 5 kW. Quandela's

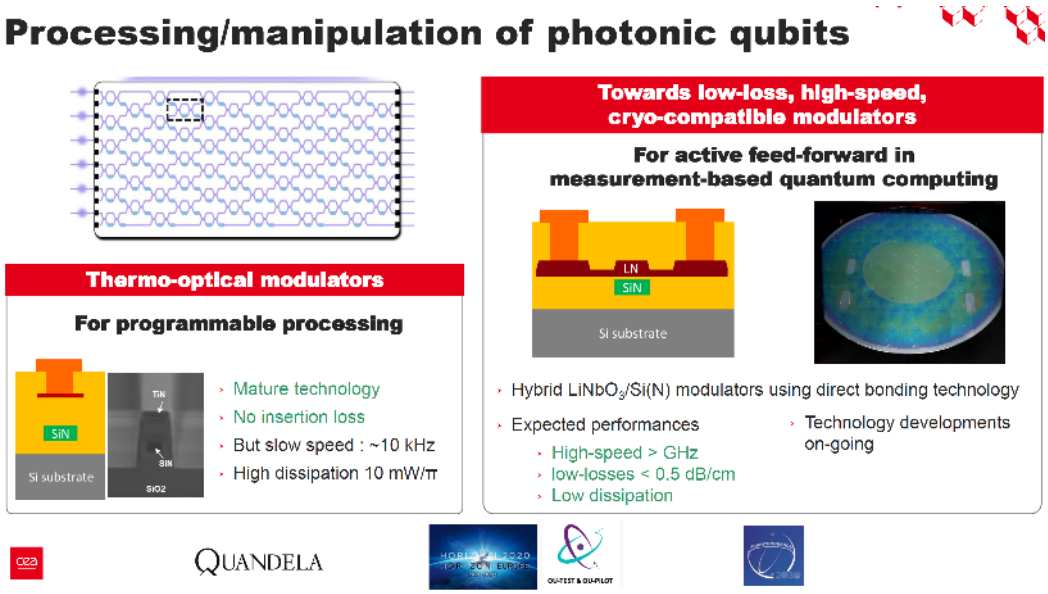


Figure 318: Two generations of programmable photonic modulators to implement MZI (Mach-Zehnder Interferometers) in path encoding photonic computing. The first is using thermo-optical modulators (left) and the second will be based on hybrid $LiNbO_3$/Si(N) modulators using direct bonding. Source: [1218].

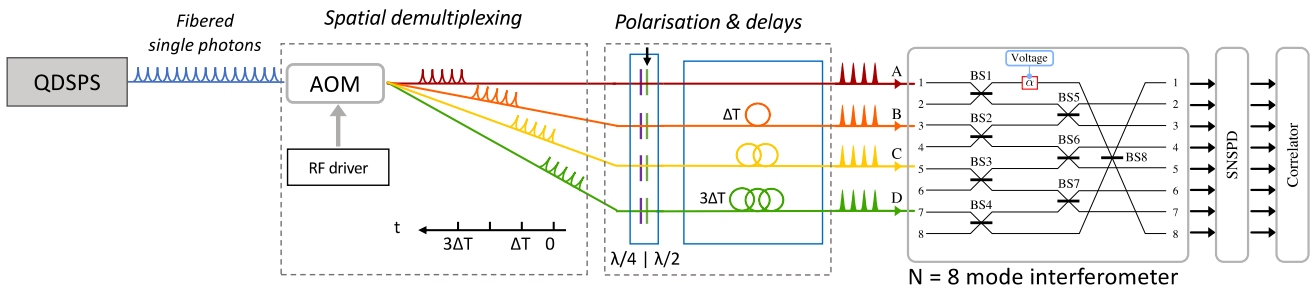


Figure 319: An interferometer used to validate the indistinguishability of a set of generated photons paving the way for the creation of cluster states of entangled photons. Source: [2845].

2024 NISQ plans were to build Canopus (24 qubits, with cluster states) in 2024 and Deneb (48 qubits) in 2026. That schedule slipped: as of 2025, Canopus and its 24 qubits were pushed to 2026 (Figure 317), which are not there yet as of September 2026.

FTQC roadmap. Quandela plans to build FTQC systems. They started with investigating the MBQC path and the generation of entangled photon cluster states [2732, 2848], with combining polarization and frequency deterministic entangled cluster states [2849]. It was extended in 2024 to cluster states of arbitrary topology [2850]. Their FTQC systems will be built using spin-optical quantum computing (SPOQC) architecture introduced in November 2023. It uses quantum dots as computing qubits and photons as ancilla qubits, with probabilistic two-qubit "repeat until success" (RUS) CZ gates and photon routing to connect all these quantum-dots based qubits [2522].

Single qubit gates will be implemented at the quantum dot level using a static magnetic field that creates a Zeeman energy splitting of the dot electron spin and picosecond laser pulses to simulate the effect of a dynamic magnetic field. It uses two-photon Raman transitions based on the use of two laser beams with a specific frequency difference which drives flips between spin states. Dynamic voltages shift the quantum dot's energy levels into or out of resonance with the optical cavity using the Stark effect. It also stabilizes the environment and neutralizes the noise generated by the surrounding nuclear spins (*aka* the Overhauser field) [2851].

In a December 2024 preprint, Quandela et al. presented an efficient way to generate cluster states of entangled photons. They tested three different architectures for constructing a 24-photon Shor-encoded (2,2) 6-ring resource state that can achieve a loss tolerance of 7.5%. These require much less resources than probabilistic single photon sources coupled to heralding, *ala* PsiQuantum. It was a way to compare the efficiency of their single photon sources vs the heralded source from PsiQuantum. But these cluster states don't seem to be part of their SPOQC architecture [2852]. A bit later, in 2025, they demonstrated 2, 3, 4 and 6-photon entanglement generation at respective rates of 6 kHz, 120 Hz, 2.2 Hz, and 2 mHz (which means a cluster state every 8 minutes) [2853]. It seems to be an enabler for the

method presented in December 2024. Meanwhile, they significantly improved the coherence time of their quantum dot spin by two orders of magnitude in June 2026, to about 2 ms, not far from their SPOQC threshold of 4 ms [2854].

Closer to the needs of the SPOQC architecture, they published a preprint in April 2026 showing how distant quantum dots could generate near indistinguishable photons [2855]. In June 2026, they then published a preprint demonstrating how they could assemble about a hundred quantum dots sources on the same chip, each with a 80% efficiency (before the attached fiber), showing an improvement of 20% in about a year [2854]. They also ran successful indistinguishability tests on the photons generated by these quantum dots and in September 2026, did demonstrate how their quantum dots two electron spin up and down states interact bijectively with the photons they emit, creating the equivalent of a deterministic C-NOT gate between the quantum dots and their emitted photons, enabling efficient resource state generation for an FBQC model [2856]. This however, shouldn't be confused with a C-NOT gate to be implemented probabilistically with the RUS method on two quantum dots emitting their photons which is the basis of their SPOQC architecture.

Their 2024 roadmap contained the release of Diadem with 100 logical qubits in 2027 and Electra with hundreds of logical qubits in 2028. As SPOQC became their platform of choice, in 2025, they updated their plans with 10 logical qubits by 2027 with Andromeda and 50 by 2028 with Draco. One of their challenges is to extend their quantum dot source coherence time to enable this platform. One encouraging sign comes from the work at the University for Cambridge, with spin coherence times of 0.11 ms [2857, 2858]. As part of their long term roadmap, Quandela also established a partnership with **Welinq** for the development of a cold atom based QPU interconnect solution between several Quandela QPUs.

In May 2026, they published a resource estimate paper exhibiting the need for 1.35 million quantum dots for supporting a Fermi-Hubbard simulation on a 8×8 lattice under 2 hours with the SPOQC architecture [2859]. It uses a biplanar honeycomb correction code, a T state factory, lattice surgery for T states teleportation and a transversal CNOT. They had previously compared the honeycomb code favorably vs surface codes [2860].

Quandela also teams up with Alexia Auffèves's quantum energy team in Singapore for the optimization of quantum dots energetic operations [2861, 2862].

Manufacturing. Quandela's quantum dot photon sources are manufactured in Palaiseau in their own cleanroom hosted at the IPVF facility. Their nanophotonic chips are produced by Ligentec in Switzerland. They use single photon detectors from various sources including **QuantumOpus**. They also announced in October 2022 that some future photonic chips will be designed and manufactured by CEA-Leti in Grenoble using SiN, and embedding photon detectors in the circuit in a future version as shown in Figure 318. They also plan to grow their quantum dots in Munich. Their cryogenic systems come from Attocube (Germany) and cools their photon sources and SNSPD photon detectors at 2.5 K with a very small form factor fitting into less than half of a rack. In June 2023, Quandela inaugurated its assembly, integration, and testing production line in Palaiseau, France.

Quandela also participates to the European pilot Photonics for Quantum (P4Q) launched in 2026, that is coordinated by the University of Twente in the Netherlands.

Software. In April 2022, Quandela released **Perceval**, their photon qubits physical classical simulation software. It enables the simulation at low level of photonic linear circuits (PBS, …), help understand how photon qubits work and create adapted algorithms like Grover, Shor, GBS, VQE and QML [2863]. These efforts benefit from a research collaboration with Inria teams [2864, 2865]. In June 2025, Quandela launched Merlin, a QML emulation SDK running with Nvidia GPUs. They believe a lot on the potential of quantum machine learning on their platform, even in NISQ mode [2866]. Quandela organized a 6-month hackathon in 2025 on finding ways to classify MNIST dataset images with various QML methods [2867, 2868]. They provided a systematic benchmarking method of 13 different approaches. None revealed any quantum advantage at this point with quantum photonic-based machine learning due to limitations of emulation hardware and of their QPU capacity, but the floor is opened to more research [2869, 2870]. In November 2025, Quandela and Nvidia used GPUs to accelerate by a factor of ×20,000 the speed of their circuit classical simulation vs a reference QuTip simulation [2871, 2872], thanks to the use of the ZPG technique created by Stephen Wein from Quandela in 2023 which simulates the probability of measuring exactly zero photons which then makes it easier to detect one of multiple photon arrivals in other detectors. It brings an exponential speedup to the simulations [2873].

Cloud. They announced that Perceval was proposed in the cloud in partnership with **OVHcloud** and connector with popular programming frameworks like Qiskit. In May 2024, Quandela announced its Cloud 2.0 platform which improves their all software suite, including Perceval, introducing an SDK for the development of hybrid classical-quantum applications [126], a Quantum Toolbox with software patterns like VQE and graph analysis, Exqalibur, a GPU-based emulator. It also contains an error mitigation tool and AI-driven quantum fidelity enhancement enabling single-qubit gate fidelities of 99.94%, and two-qubit gate fidelities of 98.2% and a Q-score of 6.

QRNG. Quandela developed a certified device independent QRNG solution with their two-photons MosaiQ QPU, based on Bell state pair generations and their Entropy patented protocol [2874, 2875]. It led to OVH-

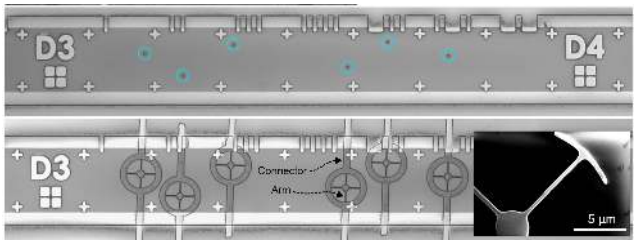


Figure 320: Quandela demonstrated in June 2026 the capability to assemble multiple quantum dots on the same chip. They are still randomly placed as show in the top of this figure. The quantum dots position is detected at cryogenic temperature and the surrounding pillars are then etched with the result showing at the bottom. Source: [2854].

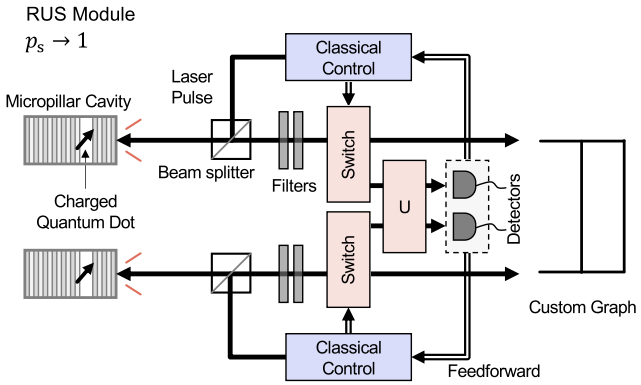


Figure 321: The generation of a cluster state of entangled photons can use two series entangled photons in polarization generated by quantum dots acting as memory qubits and where the dots spin is controlled by magnetism. The photons from the two sources are then entangled using the probabilistic RUS (repeat until success) method. Source: [2852].

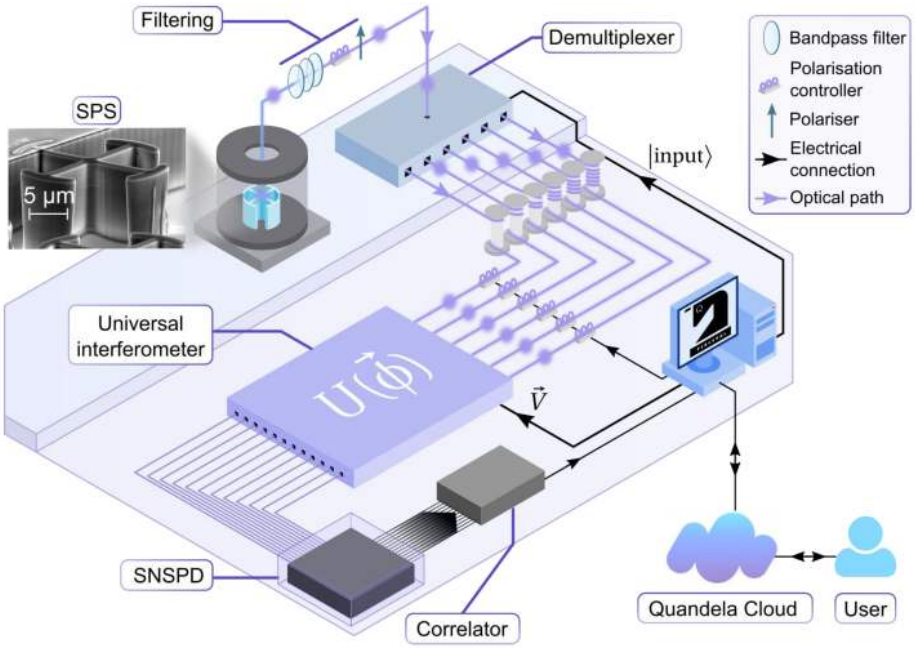


Figure 322: A typical first generation Quandela QPU first generation setup using photon path encoding with the quantum dot source, a time-bin demultiplexer with output delay lines, a universal programmable interferometer with 6 photons input, and 12 SNSPD photon detectors at the exit. The Quandela photonic architecture enables several computing modes: one using quantum gates, another one labelled "photon native" used for some quantum machine learning tasks and a boson sampling mode using a randomized 12×12 matrix. Source: [50].

cloud ordering a two-photon Quandela QPU, to generate random numbers in their R&D and cloud offering for security data encryption [2876]. The QPU was installed in OVHcloud data centers in October 2023 and inaugurated in March 2024. Quandela Ascella's QRNG capabilities were later benchmarked independently, with finding "*certain disparities attributed to factors such as imperfections in beam splitters and single-photon sources, as well as quantum noise*" [2877]. Also, Quandela announced a partnership with PQC vendor CryptoNext Security for the same reason [2878].

Use cases. Quandela started to work with **CACIB** for the development of default risk prediction models, with **EDF** on solving partial differential equations, with **MBDA** to calculate the behavior of polymer materials, with **SNCF** along with Sopra-Steria for the creation of train optimization solutions, with **Orientom** in South Korea for the development of power grid optimization, and with the service company **Mekdam** to deploy solutions in Qatar.

Quandela is also working with various partners on the creation of hybrid quantum machine learning algorithms

and prototype chemical simulations. They published a paper on solving graph problems computing a permanent using their Ascella system [2879, 2880], another one on reinforcement learning [2881, 2882], and on a generative adversarial network [2883, 2884].

Quandela is partnering with Alysophil in life sciences. In 2022, it ran a hybrid binary classification of polymer structures using a mix of 3 tested quantum and a single classical machine learning techniques. They obtain good results with the method but it is far from any quantum advantage. It was tested on the classical Perceval emulator [2885].

In May 2025, Quandela signed a MOU with BTQ Technologies to develop proof of work protocols for an energy efficient variant of the Bitcoin and proof of stake for Ethereum blockchains. This would use Quandela's boson sampling capabilities in a NISQ regime. They would commercialize it if the proof of concept works, for example in the Belenos QPU.

In June 2025, Quandela and AdvanThink partnered to develop quantum-enhanced AI systems for real-time payment fraud detection. Here as well, it will start with a proof-of-concept using some QML method along with AdvanThink's existing fraud detection solution. The related quantum advantage of such a solution remains to be found.

Customers. On top of the Belenos/Lucy machine installed in 2025 at CEA's TGCC supercomputing center as part of the EuroHPC/GENCI initiative, Quandela also sold two QPUs to Exaion, which are deployed in Quebec. They had deployed 5 systems as of mid-2026. In June 2026, Quandela entered DARPA's QBI program in phase A.

ORCA Computing

UK, 2019, $18.7M

ORCA Computing was cofounded by Richard Murray (CEO, former head of the UK quantum program), Josh Nunn (CTO, from Oxford University, and also working with VeriQloud) and Cristina Escoda (COO, an entrepreneur with a background in finance and deep tech) [2886]. Quantonation is among their investors. Ian Walmsley from Oxford University is Chairman of their Board. In January 2024, the startup acquired Integrated Photonics Division of **GXC** (USA) to complement their hybrid photonic materials assets [2887].

Technology. The startup is developing a quantum computing platform based on qumodes photons and a proprietary photonic memory using delay lines plus programmable beam splitters [2888, 2889] (Figure 323). They use photon frequency multiplexing (PT- series) and plan to later add time and space multiplexing (PA-Series) using a boson sampling mode. Their first chip was manufactured by **Ligentec** in Switzerland. They also develop their own SNSPD (single photon detectors). Their photon source is using atom ensemble in cavities.

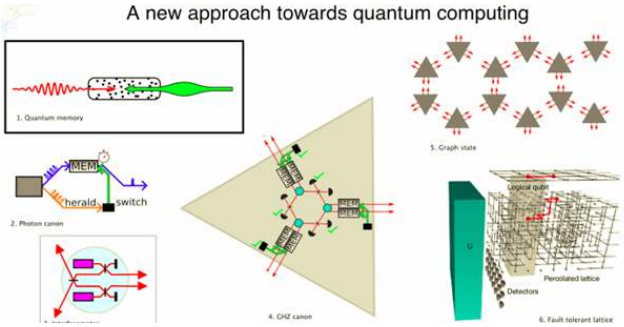


Figure 323: Orca's view of quantum computing. Source: Orca Computing.

The startup leverages research done by Ian Walmsley's Ultra-fast and Nonlinear Quantum Optics Group from the University of Oxford. They work on the efficient preparation of cluster states using dual-rail photonic qubits, and GHZ-based fusion of multiple cluster states [2890, 2891]. In 2025, they proposed an FTQC architecture that used strong single-photon nonlinearities into their GHZ-measurement-based architecture [2892]. Launched in October 2024, the PT-2 system seems to be a PT-1 connected to Nvidia GPUs. It can be used to run boson sampling [2893].

Roadmap. The company is working on the support of FTQC. They plan to support thousands of logical qubits.

Software. They developed hybrid machine learning and QUBO algorithms with their Python software library [2894, 2895] and in the financial sector [2896]. The PT-1 was independently benchmarked by researchers from the University of York, who found that even with scaling, it may not perform better than classical solution to solve some optimization problem [2897]. Orca also proposed in 2025 a binary optimization algorithm for its QPU [2898]. And in July 2026, they published a paper on how to optimize parameterized (NISQ) photonic quantum circuits [2899].

Partners. Orca announced several partnerships in 2025. With ParTec AG to integrate their QPU and HPCs, and to be deployed at various European supercomputers centers, including ELBJUWEL in Dresden and VESUVIO in Naples. With AIST in Japan to work on system engineering challenges, including reliability, availability, and maintainability, hardware integration with classical computing, and system software optimization. And with Toyota Tsusho for selling and deploying their QPUs in Japan and APAC, particularly for use cases in automotive, chemicals, and so-called Industry 4.0 applications. Also in Japan, they partner with Jij Inc. for the development of software solutions targeting logistics, energy planning, and manufacturing optimization. They also initiated a partnership in 2026 with SiC Systems for creating solutions for chemical and biomanufacturing process design, control and maintenance.

Customers. In June 2022, the UK MoD announced the procurement of Orca's PT-1 quantum computer, which fits into a single rack and manages 8 qumodes. They

planned to support 128 qumodes by 2024, and are to deliver it by the end of 2026. Sideways, Orca delivered a PT-series QPU to the UK NQCC in June 2025. The startup is also collaborating with BT Group with other partners (KETS, PQShield, Riverlane, Universities of Bath and Bristol, UCL) and the funding of Innovate UK to fuel the vision of a 'quantum data center of the future' (QDCF) [2900]. Orca also sold a PT-1 QPU to Israel's Quantum Computing Centre managed by Quantum Machines in July 2022 and two PT-1 to Poznań Supercomputing and Networking Center in Poland [2901], with a GPU hybrid PPQC-quantum environment [2902].

TundraSystems

UK, 2014

TundraSystems is developing a silicon-based linear optics quantum processor operating at room temperature with up to 60 qubits, and the related software development libraries.

Their Advisory Board includes Xinliang Zhang and Pochi Yeh, both specialized in optronics, the latter being a Taiwanese-American professor at UC Santa Barbara (site).

QuiX

The Netherlands, 2019, €38M
+ €17.5M EIC grant

QuiX is developing a photonic quantum processor using silicon nitrides (Si_3N_4) TriPlex waveguides generating low losses. It came out of a project from the University of Twente and the AMOLF laboratory in Amsterdam. The company is a subsidiary of the fab Lionix.

Technology. QuiX presented in 2021 a record 12×12 programmable photonic processor. It uses thermo-optic phase shifters and tunable beam splitters. The circuit is labeled a 12×12 because it is a universal 12-mode interferometer, with 12 input and 12 output spatial modes, not because of a photon count or a gate depth [2903] (Figure 324). It was tested to run some thermodynamic simulation but with only 3 photon lines being used [2904]. In March 2022, QuiX announced the "*world's largest photonic quantum processor*" expanding the previous 2021 performance from 12 to 20 "qumodes" [2905]. It contains 380 thermo-optic tunable elements and a photon source made of a Ti:Sapphire laser pumping a crystal. QuiX is teaming up with **PHIX** (The Netherlands), an assembly subcontractor, to create an even larger quantum photonic processor with 50 qumodes, using over a hundred optical fiber connections and about 5,000 electrical connections. In 2023, QuiX along with teams from Leibniz University Hannover and the University of Twente (the Netherlands) created a chip based entangled light source using a spontaneous four-wave mixing, an electrically pumped InP gain section and a Si_3N_4 low-loss microring filter system [2906] (Figure 325).

In July 2026, QuiX built Carina, a fully integrated quantum computer built for DLR (Germany) which includes every subsystem required for quantum computation: photon generation, multiplexing, cluster state generation, and feed-forward control (based on their Feed-Forward Control Unit or FFCU), packaged together to run gate-based quantum algorithms. In August 2026, QuiX introduced Alquor 2.0, its rack-mountable quantum photonic processor which is a successor to the previous generation, Alquor 1.0 which supported 8, 12, 20, and 32 photon modes. QuiX had sold 20 of these systems.

Customers. In September 2022, the company signed a €14M contract with **DLR**, the German Aerospace Center, to build a 64-qubit quantum computer and as a result opened an office in Germany. The company plans to build a 10K qumodes system after 2030.

Software. In May 2023, **QMware** (a Terra Quantum company) and QuiX announced the creation of a hybrid quantum-classical platform with combining photonic and classical computing in a collocated datacenter at Enschede in the Netherlands. It was to become operational in August 2023 for commercial applications deployments, promising tenfold speed improvement for unspecified use cases. They also published papers on the realization of quantum walks with 8 photons [2907], on a boson sampling to accelerate some classical Monte Carlo simulation [2908] and on the implementation of some quantum error detection technique [2909].

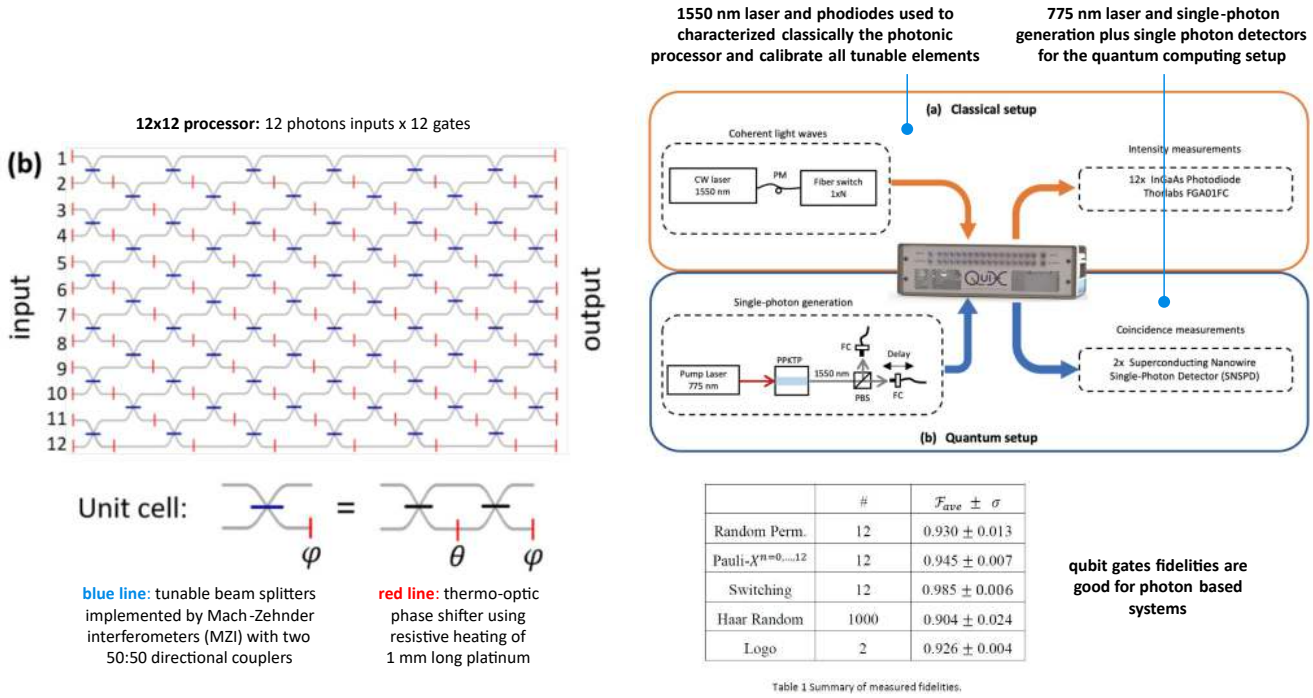
Use cases. In March 2025, QuiX, Fermioniq, and Deltares partnered to develop quantum modeling solutions for water management and infrastructure using hydrodynamic simulations. Here, Fermioniq provides quantum-inspired software solutions and Deltares brings its expertise in water research. The project is funded by the Dutch Ministries of Defence and Water Management.

QBoson

China, 2020, $160M

QBoson *aka* "Bose Quantum" was founded by Wen Kai and Ma Yin, and is headquartered in the Chaoyang district of Beijing. Kai studied at Tsinghua University and later got a PhD from Stanford in quantum computing. He also worked at Google AI in the USA.

Their model is a variant of coherent Ising machines (CIM) [2910]. It uses a network of degenerate optical parametric oscillators (DOPOs) that settle collectively into the ground state of an Ising Hamiltonian, with the capability to solve QUBO-formulated combinatorial optimization problems. They opened a dedicated manufacturing plant in Shenzhen for their photonic quantum hardware in November 2025. It is not quantum per se. As of 2025, their CIM system handled only 100 variables [2911]. As of 2026, their CPQC (Coherent Photonic Quantum Computer) is available with 100, 550, and 1,000 photons.



	#	$\mathcal{F}_{ave} \pm \sigma$
Random Perm.	12	0.930 ± 0.013
Pauli-$X^{n=0,\ldots,12}$	12	0.945 ± 0.007
Switching	12	0.985 ± 0.006
Haar Random	1000	0.904 ± 0.024
Logo	2	0.926 ± 0.004

Figure 324: QuiX circuit handling 12×12 photons (12 photons and 12 quantum gate depth using MZIs). Source: [2903].

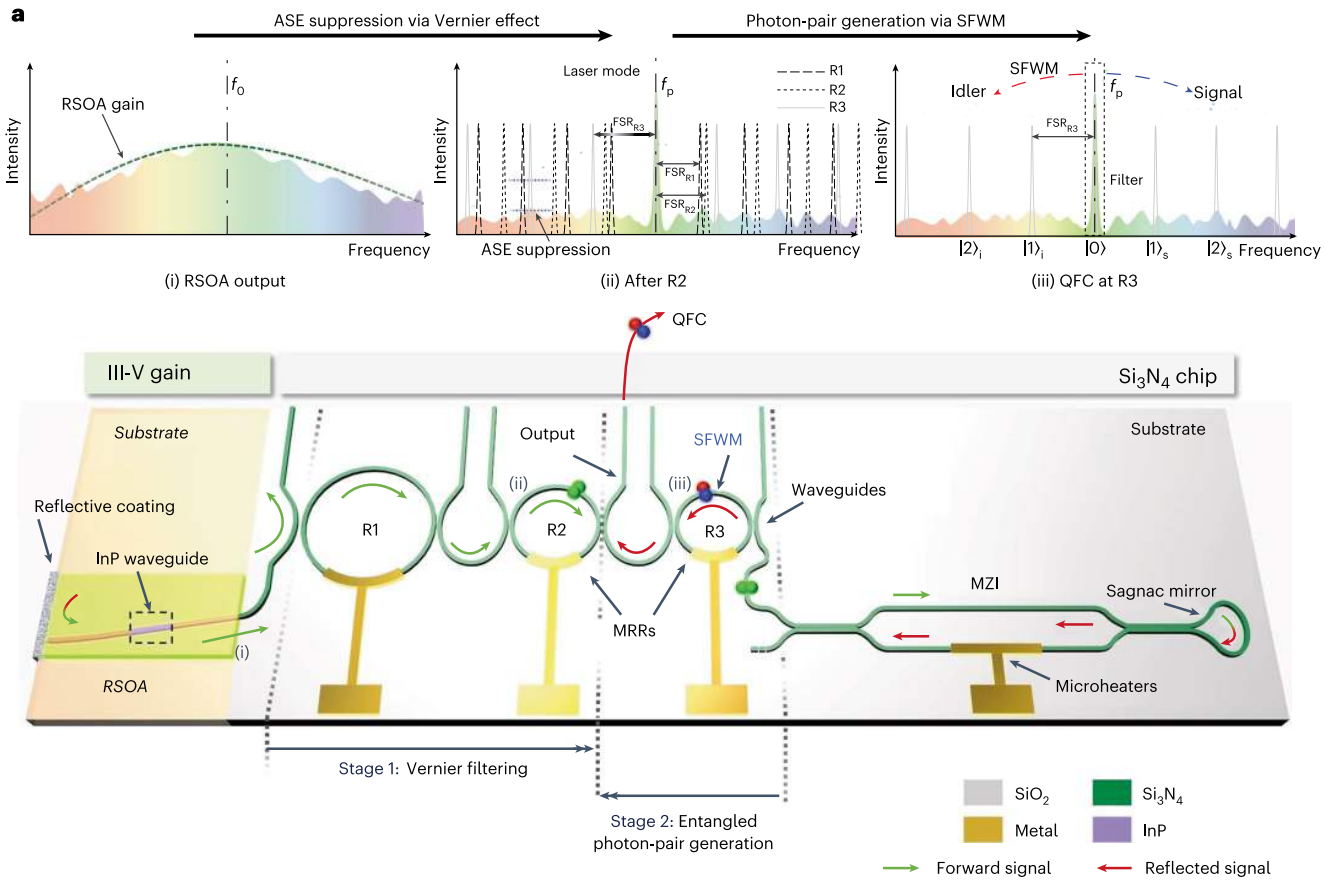


Figure 325: The chip-based QuiX entangled photonic source showing how entangled photons are created with different frequencies (i), (ii) and (iii). Source: [2906].

They operate the Wuyue quantum cloud platform and the PyTorch-integrated Kaiwu SDK. Case study wise, they published a paper in Entropy in 2024 on a fraud detection method to detect fraud communities, using a QUBO problem reformulation [2912]. In 2025, they published a paper on the optimization of bus routes in Beijing, the problem being formulated in QUBO [2913]. It was not clear it brought some computing advantage

in a generic way, particularly against the Gurobi classical solver. Their known customers are the National Supercomputing Center in Chengdu, China Mobile Communications Group, Beijing Electronic Zone High-tech Group, and North China University of Technology.

Duality Quantum Photonics

UK, 2020

Duality Quantum Photonics is a Bristol-based startup created in February 2020. Its founder is Anthony Laing, from the Department of Physics at the University of Bristol where he developed a quantum simulator based on lithium niobate generated photons.

He targets drugs design for the pharmaceutical industry. They were supposed to create a prototype in 2021.

TuringQ

China, 2021, $79M

TuringQ creates lithium niobate on insulator (LNOI) optical quantum computer chips and femtosecond lasers. Not to be confused with Turing Quantum (USA) who is specialized in NV centers computing and Turing (USA) which develops quantum software. The company was created in Shanghai by Xianmin Jin, a student from Jian-Wei Pan. The company also seems to work on photonic computing systems to solve combinatorial problems [2914]. In 2026, it released with academic partners DeepQuantum, a Pytorch-based software platform for quantum machine learning and quantum photonic computing [2915]. In August 2026, it started its IPO process in Shanghai.

In September 2026, TuringQ with academic partners created a GBS system using their thin-film lithium niobate chip supporting the detection of up to 11,059 photons. They first demonstrated some quantum advantage showing that its classical simulation could require 9.7×10^6 years on a single Nvidia A100 GPU. They then used it to modelize some physical dynamics [2686].

Quantum Computing Inc

USA, 2018, $350M

Quantum Computing Inc (aka QCi), also covered in the software vendors section, acquired QPhoton, Inc in February 2022. QPhoton (USA) was a stealth quantum photonics computing and sensing company based in New Jersey. They held a portfolio of patents on quantum hardware, authentication protocols, simulators, photonic Lidar, imaging, and covert communications. They were mostly a contract research company working for DARPA, DoD, NASA and other US federal agencies who spent $30M on these projects. The company was created and headed by Yuping Huang, a professor at the Stevens Institute of Technology (Hoboken, New Jersey), who had earlier been a postdoctoral researcher at Northwestern University (Evanston, Illinois).

QCi has since expanded through several acquisitions: **millionways** (2017, USA, $10M) in May 2023, an emotional AI platform combining analysis and matchmaking algorithms on user-generated text or audio-to-text data (at least 500 words) based on the Personality Systems Interactive (PSI) theory [2916], **Luminar Semiconductor** (a Lidar company) in December 2025, **NuCrypt** (photonics for quantum communications and sensing) in April 2026, and **NHanced Semiconductors** in 2026 for $73.1M, which launches a second fab (Fab 2) expanding QCi's nanophotonics and advanced-packaging manufacturing and accelerating commercialization of its thin-film lithium niobate (TFLN) photonic IC platform. In February 2023, QCi also spun out a subsidiary named **QI Solutions Inc** (QIE) to work with the U.S. Government and DoD on entropy quantum computing, quantum communications, and sensing.

Optimization. As part of the Dirac and Entropy Quantum Computing line, QCi's Quantum Photonic System (QPS) is a nonlinear optical system using a so-called "Entropy Quantum Computing" (EQC) process [2917], handling up to 949 variables (Figure 326) [2918]. QCi announced in July 2022 having solved a combinatorial problem with 3,854 variables 70x faster than its 2021 hybrid D-Wave implementation [2919]. In September 2022, its Dirac-1 EQC was launched as a cloud-based subscription. The current version, Dirac-3, is sold for $300K and supports higher-order (k-body) interaction terms among qudits encoded as photon-number states across time-frequency modes, rather than the quadratic Ising terms of earlier machines. In December 2022, the company announced a collaboration with **Rabobank** using Dirac-1 to improve fraudulent card transaction detection. In September 2024, it extended a partnership with Los Alamos National Laboratory on Dirac-3 QUBO use cases, and in 2024 it was awarded a fifth NASA project to use Dirac-3 to denoise sunlight in satellite LiDAR images by casting the denoising task as an optimization problem, though the computational advantage over a simple PC appears questionable [2920]. In March 2026, QCi placed its first data-center Dirac-3 unit, at the Digital Crossroad Data Center (Hammond, Indiana), connected via a Toshiba QKD-secured 10G link to the Quantum Corridor quantum-safe network. In a 2025 benchmark, the company showcased a computing-time advantage in a fraud-detection classification task versus classical solutions (CVQBoost vs. XGBoost on 4 Nvidia GPUs) [2921], and a similar advantage for matrix factorization [2922].

In August 2026, a team in Singapore did test Dirac-3 in a set of portfolio optimizations applications and found that the classical optimizer Gurobi was superior for the most demanding tasks [2923]. Dirac-3 was better than Gurobi only for a narrow scenario ("*peak risk-adjusted alpha capture and drawdown mitigation, confined to a narrow hyperparameter calibration window*"). Gurobi

was better than Dirac-3 with supporting tail-risk protection, diversification, cross-seed stability, and wide parameter robustness.

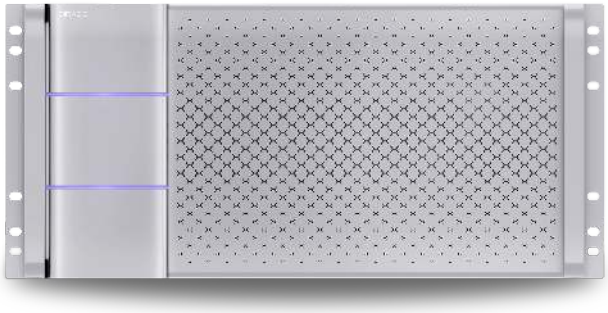


Figure 326: QCI photonic quantum computer package. Source: QCi. 2024.

AI inference. QCi also implements reservoir computing based machine learning solutions [2924], a non-von-Neumann approach well suited to time-series and signal-processing workloads. Its first product, EmuCore, was a FPGA-based edge device optimized for recurrent neural network applications. In November 2025, QCi unveiled its successor, **NeuraWave**, a standard PCIe plug-in card for hybrid photonic-digital AI inference at the edge (telecom, autonomous vehicles, robotics, healthcare, defense, industrial monitoring), built on a full electro-optic TFLN (thin-film lithium niobate) platform rather than FPGA emulation, targeting microsecond latency and real-time streaming performance not achievable on FPGA or GPU platforms. NeuraWave became available in April 2026, and in June 2026 QCi signed a framework agreement with Planck Dynamics (a Netherlands-based defense-tech portfolio company) for deployment of up to 100 NeuraWave systems, worth over $10M.

Photonic components and sensing. The company also sells an entanglement source creating entangled photon pairs based on a fiber-coupled periodically poled lithium niobate crystal to produce broadband entangled photons across the entire telecom C-band via SPDC, a quantum frequency conversion module converting C-band and O-band photons into sum-frequency visible-wavelength photons via a periodically poled lithium niobate waveguide, and uQRNG, a QRNG based on the arrival time of single photons in a photonic circuit.

Aegiq

UK, 2019, $4.3M

Aegiq is a spin-out from the University of Sheffield created by Maksym Sich, Andrii Iamshanov and Scott Dufferwiel. Pieter Kok from the University of Sheffield is their chief scientist.

It proposes its Artemis photonic-qubit QPU that is using its iSPS III-V deterministic single-photon source at 925 nm and a nanophotonic circuit from QuiX (Figure 327). Their quantum dots are manufactured at the UK National Centre for III–V Technologies in Sheffield. The QPU has an undisclosed number of photons or modes. Given QuiX's offering, it may be a 12-photon QPU. They only say that their system has a low power under 2 kW. In 2024, it won a competition to deliver a testbed QPU to NQCC by the beginning of 2025, with an undisclosed capacity [2925]. They also used QC Design's Plaquette simulation software.

Figure 327: Aegiq Artemis QPU. Source: Aegiq.

Aegiq also seems to work on the implementation of parameterized boson sampling [2926]. In December 2025, they published a blueprint describing an FBQC computing architecture using efficient GHZ-states based "repeat until success" (RUS) fusions [2927] and the QGATE (Quantum Gate Architecture via Teleportation and Entanglement) architecture mixing FBQC and entanglement quantum gates and ancilla qubits [2928]. It supports a universal gate set with a CZ two-qubit logical gate and a Toffoli logical gate. Its error correction is based on 3D foliated lattices [2928].

QC Design

Germany, 2021, €4.5M

QCDESIGN was initially named "It's Q" and a photonic qubits startup cofounded by Christine Silberhorn from the Institute for Photonic Quantum Systems (PhoQS) of the University of Paderborn.

The company was based on her research on frequency multiplexed qubits ("field-orthogonal temporal modes"), including the related pulsed photon pairs sources, and MBQC as well as quantum walks [2929], using $LiNbO_3$ on silicon oxide insulator circuits (lithium niobate). Christine Silberhorn is also investigating GBS (gaussian boson sampling) avenues as part of the German project PhoQuant led by Q.ANT. Quantonation was one of It's Q seed investors. In 2023, the company abandoned the photonic qubit route and Christine Silberhorn left the venture which was renamed QC Design. In July

2024, the startup was selected by the EIC accelerator program and got funding of €4M (€2.5M in grant and €1.5M in equity).

The company provides FTQC architectural designs and blueprints to third parties. Their IP assets seem to revolve around the way to implement surface codes. They developed Plaquette, their own FTQC simulator [2930], which is used by Aegiq, C12, QuiX, Yaqumo, ZuriQ, Quantum Source, PsiQuantum, and Qudora. The company CEO is Ish Dhand, a quantum computing researcher and former architecture team leader at Xanadu.

Quantum Source

Israel, 2021, $77M

Quantum Source is a photonic computer startup created by Oded Melamed (CEO), Gil Semo (R&D VP), Dan Charash (Chairman) and Barak Dayan (Chief Scientist, Associate Professor at the Weizmann Institute of Science, head of the Weizmann Quantum Optics group). In May 2023, they added former prime minister Naftali Bennet to their board. They had a staff of 45 as of September 2024.

Their architecture is based on using stationary ^{87}Rb rubidium atoms trapped in a high-quality photonic integrated circuit using silicon-nitride photonic resonators. Photons are used as intermediary to generate single and two-qubit gates [2931]. They look to fit a one million photonic qubit source in a simple server rack [2932]. They also work on an architecture that could remove the need for indistinguishable photons for the implementation of FBQC models [2933].

In June 2026, they published an FTQC blueprint based on an MBQC architecture [150]. Entangling gates, single-photon generation, and state preparation and measurement (SPAM) are fast, lasting only 10 ns. The photon-atom controlled-phase (CZ) gate has an estimated efficiency of 98.4%, while atomic state preparation reaches 96.9% and measurement 97.6%. The atom-cavity unit cell functions as a near-deterministic single-photon generator, also quoted at 98.4%. The two 98.4% figures apply to different operations, please confirm the second one against the blueprint.

Fault tolerance is implemented using the Raussendorf-Harrington-Goyal (RHG) lattice, where a 3D cluster state acts as an MBQC equivalent to the surface code. It supports correlated errors and the use of efficient minimum-weight perfect matching (MWPM) decoders. The full Clifford gate set (Hadamard, Phase, and CNOT) is implemented transversally using the system's nonlocal photonic connectivity. They support T-gates generation and teleportation. They plan to support a few thousand logical qubits with about one million physical qubits.

They also proposed in September 2026 a theoretical model for implementing QPU interconnect capabilities, using a memory-assisted asynchronous quantum interconnect designed to generate high-rate, high-fidelity remote entanglement between multiple quantum processors. They would use single trapped atoms inside their cavity as an intermediate quantum memory and gate mediator [2934]. With the addition of microwave-to/from-optical photons transduction, it would potentially enable superconducting qubit processors interconnect.

QC Design (Germany) provided them in 2024 the Plaquette software tool for designing FTQC and QEC architectures [2930].

PhotonicsQ

Israel, 2021

PhotonicsQ is a startup developing a photonics QPU chipset implementing some routing architecture to enable direct interactions between any qubits, independently of their physical proximity or quantity.

It is reusing concepts coming from classical CMOS and optical chip technology like pipeline processing using photonic registers for intermediate result storage and tristate photonic buses to facilitate data-path structures. The company was cofounded by Moti Kintzlinger (CEO), Itay Harel (COO) and Ron Folman (CSO and President), a professor of Quantum Physics at Ben Gurion University.

Quanfluence

India, 2021

Quanfluence is a stealth company building some photonics-based quantum computer. The company was cofounded by Aditi Vaidya and Sujoy Chakravarty.

Rotonium

Italy, 2022, €1M

Rotonium was launched by Roberto Siagri (CEO) and Fabrizio Tamburini (CTO) for the creation of a room-temperature photonic QPU using photon orbital angular momentum to encode quantum information. Their future QPU will target edge quantum computing use cases, which could make sense for the implementation of blind quantum computing protocols when a small edge QPU interacts with a large scale QPU through some quantum communication link in a highly secured manner. See some of their work published in 2025 in [2935–2937].

Fixstars Amplify

Japan, 2023

Fixstars Amplify launched in November 2024 a cloud accessible general-purpose continuous-variables and time-division multiplexing based optical QPU, that they call an analog optical quantum computer. It was created with RIKEN (Akira Furusawa) and NTT (Hidehiro Yonezawa). The architecture is described in detail in a June 2025 arXiv [2938]. It is using a hundred CV

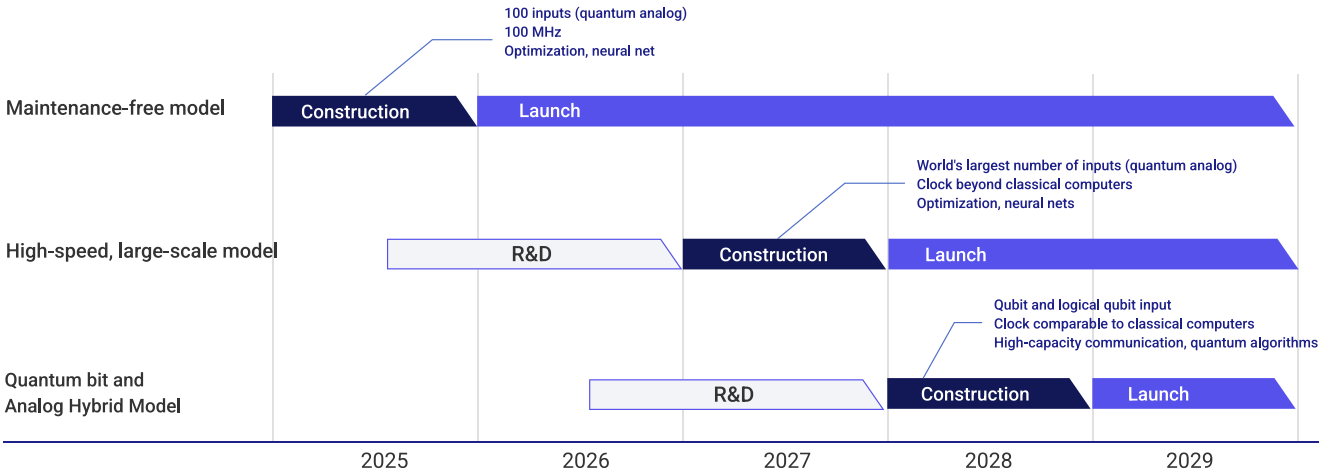


Figure 328: OptQC roadmap as of July 2025. Source: OptQC website.

photon inputs at 100 MHz. The paper doesn't describe any application or quantum advantage.

OptQC

Japan, 2025, $59M

OptQC is creating a time-domain-multiplexed cluster-based optical quantum computers. It spun-out from the Akira Furusawa Laboratory at the University of Tokyo. Their process is based on continuous variables [2939], quantum teleportation and entanglement [2940, 2941], Bell measurement and feed forward operations. See their roadmap in Figure 328. In August 2026, NTT announced it would become an investor in the company, with an undisclosed amount. Mitsubishi Electric also invested in the company.

QC82

USA, 2023

QC82 wants to deliver a QPU with millions of qubits using room temperature photon detection and low-loss photonic chip designs. It uses continuous variable photons and GKP qubits. They published a blueprint in December 2024 [2942].

Q.ANT

Germany, 2018, €80M

Q.ANT was founded by Michael Förtsch. It builds thin-film lithium niobate (TFLN) photonic chips on its own pilot line, runs a US HQ in Austin under new CTO Bruno Spruth. Their offering contains photonic enabling technologies and quantum sensing described later in 2.3.1 and classical analog photonic computing with the LENA architecture and the Native Processing Unit (NPU), sold as a PCIe-based Native Processing Server (NPS), working with the Q.PAL software library. It is doing matrix-vector multiplication and nonlinear neural-network operations directly in optical amplitude. They claim a reduction of energy consumption by a constant factor of 30 per AI operation vs GPUs with 16-bit floating-point precision.

They are also developing some CV-based photonic quantum computer, which is documented in a June 2026 preprint [2946]. It is an FPGA-based feedforward system for measurement-based Gaussian Boson Sampling exhibiting 95% quantum efficiency homodyne detection, 15 dB clearance at 1 GHz, and 196 ns total latency. It is still at the component-level with no disclosed qubit-count target or product roadmap.

Qluster

France, 2026, €450K

Qluster is a continuous-variable photonic quantum computing venture being spun out of the ENS LKB in Paris, France and created by David Fainsin (CEO), Valentina Parigi (CSO), Ambroise Boyer (CTO) and Clarisse Thibault (COO). Fainsin did his PhD in Parigi's group on the generation of large-scale CV entangled states using optical frequency combs.

Their goal is to encode quantum information on the quadratures of light and perform computation via sequential homodyne measurements on a pre-generated multimode entangled cluster state [2947], a measurement-based scheme operating at room temperature which therefore has a very low energy footprint. Scalability comes from time and frequency modes multiplexing. This is based on Parigi's research track record with squeezing across more than 21 frequency modes generated by single-pass parametric down-conversion (SPDC) in a nonlinear waveguide at telecom wavelength, with up to approximately 2.5 dB of squeezing, and demonstrates reconfigurable few-node cluster states from the same source [2948]. Related work on quantum reservoir computing using CV cluster states from the same group extends the platform toward NISQ applications [2949]. Their frequency-comb approach is deterministic rather than postselected, unlike most DV photonic schemes.

Outside the commercial world, let's mention **Prakash-1**, an experimental photonic quantum computing platform, designed for research in QML and optimal similarity measurements [2950]. It is located at Imperial College London (UK). Who developed there with the support from the University of Oxford and Nanjing University. It uses a photonic integrated circuit (PIC) with a 10×10 square mesh of symmetric MZIs which was manufactured by LioniX.

Key photonic quantum computing reviews

Here is a selection of photonic quantum computing scientific reviews to dig into the concepts presented in this section:

Linear optical quantum computing with photonic qubits by Kok *et al.*, January 2007 (40 pages): the founding survey of linear optical quantum computing: KLM, probabilistic two-qubit gates, realistic components and the errors they induce [2943].

Optical Quantum Computing by Hasnaoui *et al.*, September 2026 (54 pages): the broadest recent survey, sorted by encoding and by gate-based versus cluster-state computation, with tabulated experimental results per protocol and a dedicated section on non-universal photonic computing covering boson sampling, VQE and QML [2944].

Toward large-scale fault-tolerant universal photonic quantum computing by Takeda and Furusawa, June 2019 (11 pages): continuous-variable, hybrid qubit-CV deterministic gate sets, time-domain multiplexing and GKP-based fault tolerance [2945].

Integrated photonic quantum technologies by Wang *et al.*, April 2020 (12 pages): material platforms, on-chip sources and detectors, and what blocks scaling [2519].

2022 Roadmap on integrated quantum photonics by Moody *et al.*, January 2022 (80 pages): component-level roadmap covering PIC platforms, classical and quantum light sources, frequency conversion, detectors and applications [2646].

Heralded generation of entanglement with photons by Forbes *et al.*, August 2025 (26 pages): Heralding versus postselection, multiplexing, imperfection budgets and resource states for LOQC and FBQC [2715].

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[2782] Roll call purchase recommendations for Illinois Quantum and Microelectronics Park, by IQMP Board of Trustees, November 2024 The document mentions that "*IQMP, LLC will then execute a $15,000,000 purchase order with ComEd for a new onsite substation with multiple large transformers and capacity to supply 350MW of power at the IQMP*". These include 300MW to cover the need for three PsiQuantum systems with 100MW power draw each, and 50 MW for the rest of the IQMP park which hosts the National Quantum Facility (NQF). NCF will provide cryogenic services with up to 20 traditional cryostats for the park participants like IBM, Pasqal, Infleqtion and Diraq.

[2783] Illinois Quantum & Microelectronics Park, by IQMP.org, December 2025 (12 pages) describes the overall plan for the IQMP site in Chicago, the layout of the three PsiQuantum quantum computers on the site (phases two, three and four) and provides details on the National Quantum Facility (NQF).

[2784] Powering the Future: How ComEd's Partnership Sparked the Illinois Quantum Campus, by Excelon, Excelon website, August 2025 This press release from the electricity provider of the ICMP site in Chicago that will host three PsiQuantum computers mentions that: "*The demands of powering a utility-scale quantum campus are immense, estimated at approximately 350 megawatts, enough to support not only PsiQuantum but also shared facilities like a state-of-the-art cryogenic plant and, eventually, other cutting-edge companies drawn to the site [...]. Meeting these needs required out-of-the-box thinking. When PsiQuantum decided to accelerate the development of a prototype quantum computer at the IQMP, ComEd responded by repurposing retired transmission infrastructure, enabling rapid delivery of up to 100 megawatts*". We infer from this that a single PsiQuantum system needs 100 MW and that three of them will be installed in Chicago in their quantum data center.

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This **Photon qubits** subsection contains 468 bibliographical references and notes containing at least 8,005 pages.

1.11 Exotic qubits

Many research labs are working on exotic qubits of various kinds. Most of the time, these qubits are still at the fundamental research stage and far from being commercially viable solutions. In many cases, even a complete functional single-qubit demonstration has not yet been achieved.

Figuring out the TRL of these proposals is usually easy: it is very low, particularly when no experimental single- and two-qubit gate fidelities have been published. Depending on the platform, other useful figures of merit can still be available, such as coherence times (T_1, T_2), SPAM fidelities characterizing state preparation and measurement, or Bell-state fidelities characterizing the ability to generate entanglement. Bell-state fidelity is not, however, a substitute for randomized benchmarking or process characterization of a two-qubit gate. Compared with mature qubit platforms, these emerging approaches generally have much less complete demonstrations of initialization, control, entangling gates, readout, and scaling. Some nevertheless exhibit attractive individual properties, such as long coherence times. Most are therefore primarily interesting physics experiments at this stage. Some may also find useful applications in quantum sensing before quantum computing. This does not, of course, prevent research laboratory communication departments from fueling hype with overpromises about scalable quantum computing, as shown in Figure 331.

1.11.1 Atoms and molecules

In the atom and molecular realm, we can count on:

- **Molecular qubits** using calcium monofluoride or sodium cesium, in which quantum information is encoded in molecular rotational states and long-range electric dipole-dipole interactions provide entangling operations [2951–2953] (Figure 329). In CaF, dipolar spin exchange was used to implement an iSWAP operation and generate a Bell state. There is also a proposal to use BiPhi carbene molecular qubits with single-molecule spin-photon interface capabilities in the PIQC (Photonic Integrated Quantum Circuits) architecture [2954].

- **Diatomic molecules** with the qubit manifold encoded in molecular orientation states [2956].

- **Molecular ions**, which are easier to trap than neutral molecules using radio-frequency ion traps and could be used for gate-based computing and quantum simulation. Information can be encoded in rovibrational or rovibronic states, for example in rotational angular momentum or in combinations of rotational angular momentum and nuclear spin projections along a magnetic-field direction. The molecular internal state can be mapped onto a shared motional mode of a co-trapped atomic-molecular ion string. That motion can then be read through the co-trapped atomic ion, enabling indirect and potentially nondestructive readout of the molecular ion [2957]. A motional qubit encodes quantum information in two selected quantized motional states of the trapped-ion system.

- **Molecular magnets**, or molecular spin qubits [2958–2962]. One well-known example uses terbium bis-phthalocyanine, $TbPc_2$, also called "bis(phthalocyaninato)terbium(III)" (Figure 330). Its ^{159}Tb nucleus has spin $I = 3/2$, producing four nuclear-spin states that can form a qudit with $d = 4$. The acronym SMM stands for Single-Molecule Magnet. In single-molecule devices, the nuclear-spin state can be read electrically through transport in a transistor geometry, while coherent manipulation exploits the hyperfine and quadrupolar level structure [2955, 2963]. These molecules offer chemical tunability and multiple addressable levels, but control, integration, and scaling remain difficult. A molecular magnet was also coupled to a superconducting resonator in 2026 [2964].

- **Molecular spin qudits** (MSQs), on which a QFT was experimentally implemented in 2026 using ^{173}Yb(trensal) molecules. The molecule provides 12 electro-nuclear spin energy levels from an effective electronic spin $S = 1/2$ coupled to the ^{173}Yb nuclear spin $I = 5/2$. In the experiment, three levels were used as a qutrit for the QFT demonstration, with refocusing used to mitigate inhomogeneous broadening [2965]. Trensal is the organic ligand 2,2',2"-tris(salicylideneimino)triethylamine. This platform is a variant of molecular spin qudits and molecular magnets.

- **Polar molecules** in optical tweezers or optical lattices, with qubits often encoded in hyperfine or rotational states [2966–2969]. Proposals also exploit larger rotational manifolds to define qudits with dimensions up to $d = 5$, for example with SrF and ^{87}Rb^{133}Cs molecules [2970].

- **Asymmetric-top molecules**, which can enable the realization of qutrits [2971].

- **2D organic-molecule networks** using optical excitation for two-qubit gates [2972, 2973] (Figure 332).

- **Fluorescent proteins** with optically addressable molecular spins, which may be more relevant for quantum sensing than computing [2974, 2975].

- **Nematic bits in liquid crystals** [2976]. These "nbits" are topological defect configurations in nematic liquid crystals whose state space can be mapped mathematically onto a Poincaré-Bloch sphere. Despite the analogy with Pauli and Hadamard operations, they are not quantum qubits and the proposed logic is classical or nonclassical

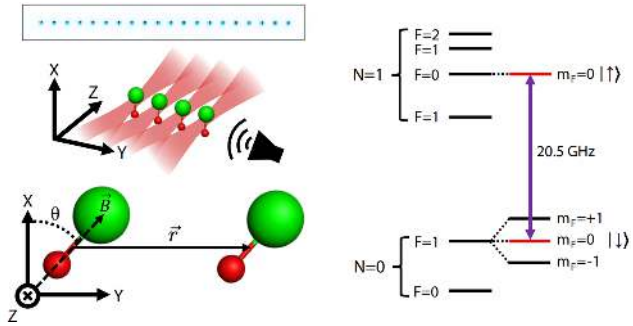

Figure 329: An example of a molecular qubit. Source: [2951].

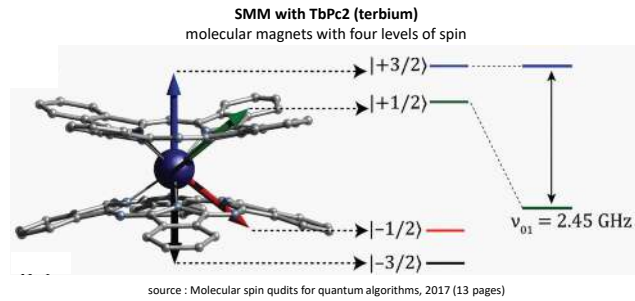

Figure 330: $TbPc_2$ is a molecular magnet used as a prototype molecular spin qudit. Source: [2955].

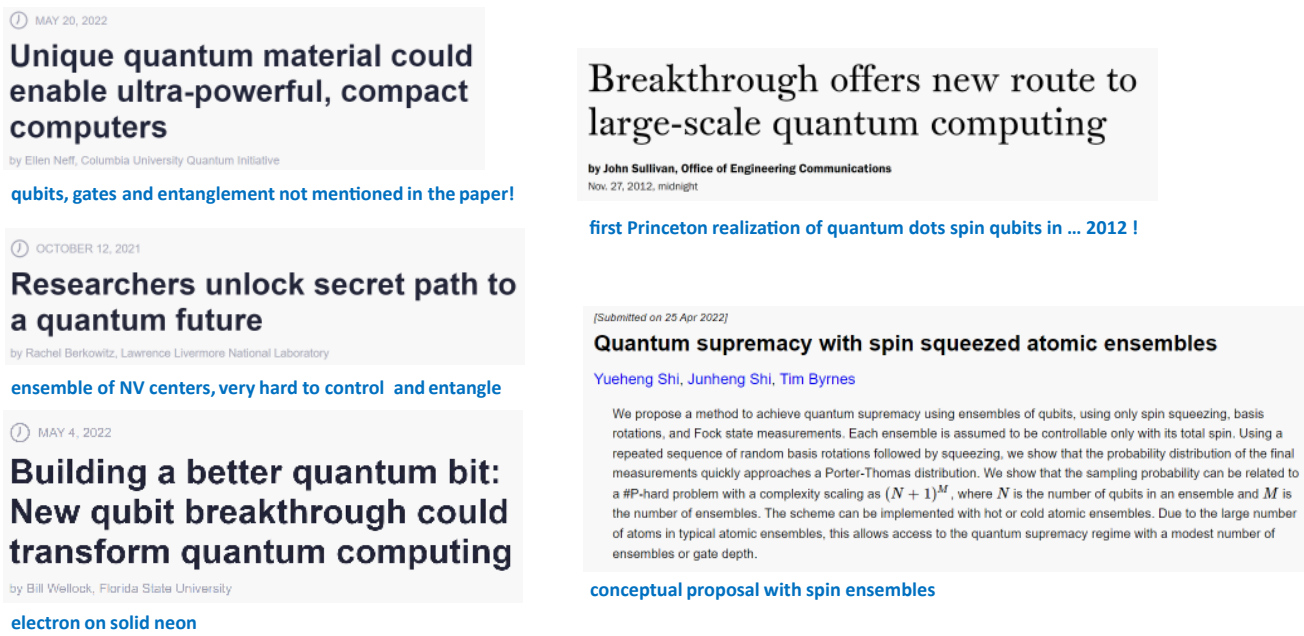

Figure 331: Examples of research laboratory communication on new exotic qubits with very low TRL, 2022.

continuous computation rather than quantum computation. Other proposals use chemical compounds with photon-controlled state transitions [2977].

- **DNA qubits**, a highly theoretical approach for which any practical implementation remains a major challenge [2978].

- **Rare-earth ions** in an insulating solid-state matrix, with quantum information encoded in nuclear-spin states [2979].

- **Nuclear-level qubits in trapped ions**, such as a 2025 theoretical proposal using $^{229}Th^{3+}$ ions and the approximately 148.4 nm nuclear transition. The proposed scheme uses continuous-wave vacuum-ultraviolet driving for coherent nuclear-state control and phonon-mediated entangling gates between trapped ions. High-fidelity two-qubit operation is predicted from realistic parameters, but has not yet been experimentally demonstrated [2980].

- **Multiexcitons** in metal-organic frameworks, initialized by photoexcitation. Singlet fission first creates a coupled triplet-pair state with singlet character, ^{1}TT, which can evolve into an exchange-coupled quintet state, ^{5}TT, with total spin $S = 2$ and five magnetic sublevels. Room-temperature coherence of the ^{5}TT state exceeding 100 ns has been observed. This is an interesting route toward molecular quantum information processing, but it is not yet a demonstrated gate-based qubit processor [2981].

- **Arsenic donors in silicon** [2982]. This is a donor-spin scenario, similar to phosphorus in silicon, where the donor electron spin provides a two-level qubit and the ^{75}As nuclear spin, with $I = 3/2$, provides additional long-lived quantum degrees of freedom coupled to the donor electron.

- **Titanium atoms on a magnesium oxide surface** [2983], with quantum information encoded in the spin of an unpaired valence electron of a single titanium atom.

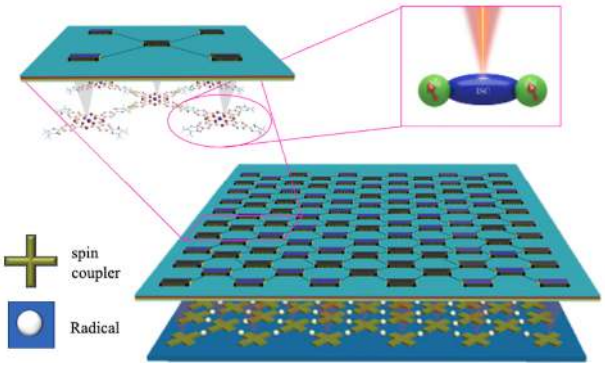

Figure 332: Organic-molecule qubits. Source: [2972].

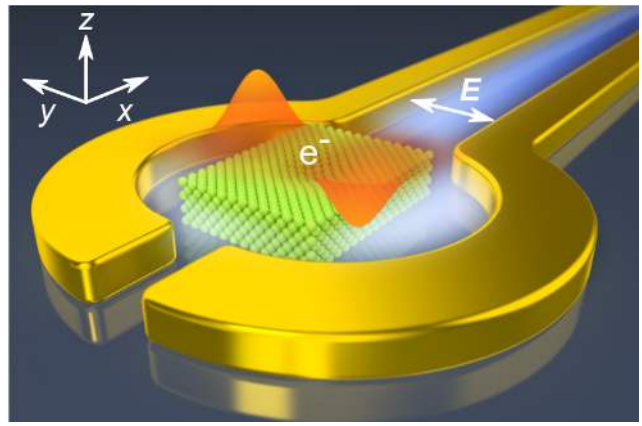

Figure 333: Electrons on solid neon. Source: [1304].

- **Nuclear spins** of carbon-based molecules, with a stated goal of assembling systems with up to 50 qubits [2984].
- **Microtubules** [2985], in a highly speculative theoretical proposal related to earlier quantum-coherence models of biological microtubules, including ideas associated with Penrose and Hameroff's Orch-OR framework. In this model, the information unit is a qudit constructed from four entangled two-state tubulin-dimer degrees of freedom associated with a parallelogram in the microtubule lattice. The paper proposes experimental tests, but no experimentally demonstrated microtubule qubit, entangling gate, or scalable quantum processor currently exists.

1.11.2 Electrons

In the electron realm, many approaches use electron spin, while others encode information in charge, orbital or motional states, collective magnetic excitations, or flying electronic wave packets:

- **Topological materials** [2986–2988].
- **Graphene-based qubits** [2989].
- **Carbon-nanotube-based mechanical oscillators** [2990].
- **Electron spins in magnetic materials**, including van der Waals crystals containing chromium [2991].
- **Spin defects in zinc oxide** (ZnO) [2992].
- **Electrons on solid neon**, where the qubit is encoded in quantized motional states of a single trapped electron coupled to a microwave resonator. The 2022 experiment measured T_1=15 μs and T_2>200 ns [1304] (Figure 333).
- **Skyrmion qubits**, in which quantum information is encoded in collective states of nanoscale magnetic textures. Proposals describe single- and two-qubit gates and readout, but decoherence and device-level control remain major challenges [2993–2995].
- **Magnonic qubits**, where quantum information can be encoded in the zero- and one-magnon states of a collective spin excitation in a ferromagnetic material. Hybrid circuit-QED experiments couple these magnetostatic modes to microwave cavities and superconducting qubits, which provide the nonlinearity needed for quantum control [2996].
- **Electronic-wave-packet qubits**, a proposed breed of flying qubit using time-bin encoding in semiconductor electron interferometers. The 2024 work demonstrated single-mode electronic interference as a building block, rather than a complete gate-based processor [2997].

1.11.3 Other breeds

You also have:

- **Neutrons**, as part of the QCN (Quantum Computing with a Neutron) endeavor related to the qBounce project [2998], led by Hartmut Abele, Hansjörg Dittus, and Markus Huber from TU Wien, Tobias Jenke from ILL in Grenoble, Skyler Degenkolb from Heidelberg University, and Beatrix Hiesmayr from the University of Vienna. These experiments use different neutron degrees of freedom as quantum-information subsystems and are primarily tests of quantum control and foundations rather than a route to a scalable multi-neutron quantum processor.
- **Superconducting quantum neural-network and reservoir-computing circuits**, which use modified or specially coupled superconducting-qubit networks for neuromorphic quantum information processing [2999–3001]. These are specialized circuit architectures rather than a distinct physical qubit species.

- **Quantum memristors** [3002], which are quantum circuit or device elements with memory-dependent response and are not, by themselves, a distinct qubit modality.

- **Toponomic quantum computing**, a theoretical computational framework related to topological concepts rather than a demonstrated qubit hardware platform [3003].

- **Topological insulators**, including a two-year FAU research project launched in 2025 with funding of about €900K to investigate topological-insulator-based qubits and the long-term possibility of compact quantum hardware. The work led by Vojislav Krstić explores nanoscale topological materials and symmetry breaking. A 2026 study reported room-temperature magnetic-force imaging of robust edge-state-related signals in Bi_2Te_3 crystallites [3004]. This is still far from demonstrating a qubit, coherent quantum gates, or a room-temperature quantum computer.

- **Qubit hybridization techniques**, which combine fast qubits with long-coherence quantum memories, for example superconducting qubits coupled to NV centers or to yttrium-iron-garnet magnon modes [3005]. This is an architectural strategy rather than a new qubit species.

- **Unruh-DeWitt quantum computers**, a theoretical proposal in which localized qubits couple to quantum-field-like excitations in condensed-matter systems. Suggested implementations include graphene ribbons, edge states in the quantum spin Hall phase of HgTe quantum wells, and quantum anomalous Hall phases in transition-metal dichalcogenides. The model can provide effective all-to-all connectivity through a Luttinger liquid, but no such quantum computer has been experimentally demonstrated [3006].

- **Qubit thermal machines**, a theoretical thermodynamic model proposed to solve a Deutsch-Jozsa problem, without a corresponding hardware implementation [3007].

- **Nanomechanical and mechanical-resonator qubits** of different breeds [3008]. In the 2024 ETH Zurich experiment, a high-overtone bulk acoustic wave resonator (HBAR) was coupled to a transmon superconducting circuit. The induced single-phonon anharmonicity exceeded the decoherence rate by a factor of 6.8, enabling initialization, readout, and direct single-qubit gates on the lowest two mechanical levels. The intrinsic mechanical-mode coherence times were T_1=104.0±1.1 μs and T_2=205.3±11.5 μs [3009]. In 2026, the same general hybrid architecture was extended to multiple mechanical modes and demonstrated a universal gate set including controlled arbitrary-phase gates, together with QFT and quantum period-finding experiments [3008]. A different 2024 proposal uses atomic surface forces to create a silicon nanomechanical qubit with a predicted 60 MHz frequency and about 5 MHz single-phonon anharmonicity [3010] (Figure 334). These results make mechanical modes increasingly interesting for quantum memories and hybrid processors, although scaling, control hardware, and fault-tolerant operation remain open challenges.

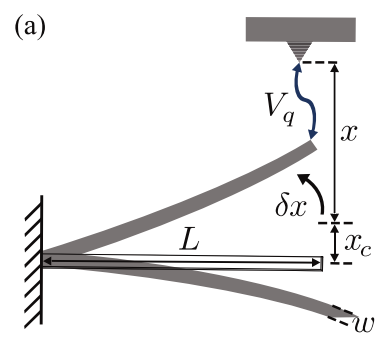

Figure 334: A proposed silicon nanomechanical atomic-force qubit. Source: [3010].

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This **Exotic qubits** subsection contains 61 bibliographical references and notes containing at least 796 pages.

1.12 Quantum computing hardware key takeaways

- Superconducting qubits are among the most common approaches today, implemented by IBM, Google, Rigetti, IQM and Origin Quantum among others. They remain noisy and face scaling challenges, particularly in control electronics, cabling and readout. One approach is to use bosonic encodings such as GKP and cat qubits, which combine microwave modes stored in cavities with superconducting circuits for manipulation and readout (Alice & Bob, AWS, Nord Quantique). Fluxonium qubits seem promising, but only a few vendors pursue them, including Google, which acquired Atlantic Quantum in October 2025. Alibaba was active in that segment but ended its quantum computing R&D in late 2023.

- Quantum-dots spin qubits could scale well due to their small size, the reuse of classical CMOS semiconductor manufacturing known-how, their higher working temperature enabling the usage of control cryo-electronics. They have however been demonstrated only at a very low scale at this stage.

- NV-center qubits have the benefit to be stable and to work potentially at ambient temperature. An increasing number of startups are playing in this field, like Quantum Brilliance (Australia and Germany). None of these commercial products support more than 10 qubits and it's been the case for several years. Don't count on it for scalable quantum computing and scalable room temperature operations. There are variations with other cavities and defects like with silicon-carbide (SiC) and SnV (tin vacancy color centers) but their technology readiness level remains very low as well.

- Topological qubits aim to obtain intrinsic protection against some classes of errors and could improve scalability if a suitable topological platform is demonstrated. Experimental solid-state platforms investigate Majorana zero modes, which are emergent quasiparticle excitations and should not be conflated with hypothetical elementary Majorana fermions. Microsoft's Majorana-1 and -2 announcements in 2025 and 2026 do not yet validate the architecture which is still lacking operational metrics. Microsoft's 2029 FTQC objective is a roadmap target whose feasibility remains uncertain if not totally unrealistic.

- Trapped-ion qubits have achieved very high fidelities and provide a credible approach for running NISQ algorithms. They have historically faced scaling challenges, with the current record as of September 2026 being Quantinuum's Helios 98-qubit processor. Recent progress with QCCD architectures shows additional scaling potential. One key limitation is slower gate speed, partly offset by high qubit-to-qubit connectivity that can reduce routing overhead and circuit depth, as well as potentially lower hardware and energy requirements in some architectures.

- Cold-atom qubits are widely used in quantum simulation, where systems can scale to hundreds or thousands of atoms, and they can also be used for gate-based quantum computing. Key demonstrations at the end of 2023, particularly with QuEra, increased interest in scaling these systems in gate-based mode and with quantum error correction. Pasqal (France), QuEra (USA), Infleqtion (USA), Atom Computing (USA) and planqc (Germany) are among the industry vendors in this field. New players entered the field in 2025-2026, including Q-Factor (Israel), Logiqal, Oratomic and Google (USA).

- Photonic qubits are flying qubits, propagating from sources to detectors through optical components that implement state preparation, transformations and measurements. The main encodings include discrete-variable and continuous-variable photonic schemes. Scalability remains challenging, particularly because of photon generation, loss and detection efficiency. Limited deterministic gate availability motivates measurement-based approaches such as MBQC and fusion-based quantum computing (FBQC), the latter being pursued by PsiQuantum. Quandela (France), Xanadu (Canada) and QuiX (The Netherlands) are other key players in this space. A key capability for measurement-based schemes is the generation of large, high-fidelity entangled photonic resource states, which remains an active research and engineering challenge.

- There are many other qubit types proposed by academic research teams, including molecular, nanomechanical and other emerging approaches. These generally have a very low technology readiness level, and many have not yet demonstrated a complete gate set or reported gate fidelities. Some may nevertheless represent promising approaches worth monitoring.

2 Quantum enabling technologies

Building a quantum computer, and other second quantum revolution related products, combines a broad set of complex technologies, some of which are quantum-specific and others that have more generalist uses. These enabling technologies, which are covered in this section of the book, are critical components, especially in quantum computing, as their characteristics and performances frequently have a direct impact on the performance and scalability. We look here at the following enabling technologies and their respective vendors in cryogenics and vacuum, control electronics including cabling and classical electronics, photonics including lasers (Figure 335) and semiconductor manufacturing. The chapter will also address their supply chain, most specifically the provenance, scarcity and transformation of the raw materials.

2.1 Cryogenics

Most types of qubits require some cryogenic technology, the most demanding being the very low operating temperatures of superconducting qubits, at about 10 mK to 15 mK. Spin qubits like silicon or silicon-germanium qubits require cooling between 500 mK and 1.5 K. Other technologies like photonic qubits usually require cryogenics operating at about 2 K to 4 K for their photon sources and detectors, and now, frequently for everything in-between (circuits, fiber) to avoid adding distance that generates photon losses [3011] (Figure 336). Cold atom and trapped ion QPUs may also rely on 4 K cryogenics for cooling their ionic ultra-vacuum pumps and atom chamber, usually to avoid thermal photons or to help reach UHV conditions.

By definition, cryogenics operates below 123 K, or −150°C. Bearing in mind that −153.15°C is the temperature below which permanent gases, i.e. gases in the ambient air, all condense into liquid at ambient pressure. Detectors must indeed be cooled to avoid the photon dark count effect, when thermal noise originated photons are detected instead of useful photons.

The Kelvin scale starts at absolute zero (0 K). This temperature, where thermal motion vanishes while zero-point motion remains, is unreachable. If it were, Heisenberg indeterminacy would be broken. It can be approached asymptotically. The lowest temperature record is 38 pK (pico-kelvin), reached in 2021 in Germany [3012]. Absolute temperature cannot fall below 0 K. One proposal nevertheless describes an effective cooling below the equilibrium ground state, by suppressing quantum fluctuations for strontium titanate ($SrTiO_3$) by inducing a strong out-of-equilibrium regime with resonant mid-infrared pulses. This suppression of fluctuations leads to a dynamical cooling of the atom nuclei effectively reducing the nuclear kinetic energy below its equilibrium zero-point value. This is a nonequilibrium effective temperature, not a negative absolute temperature [3013].

Let us recall that the science of low temperatures used in quantum computing has benefited from numerous advances from other fields: space and especially space telescopes where a large part of the instruments needs to be cooled such as infrared sensors or bolometers, particle accelerators with their superconducting magnets and finally, medical imaging, especially MRI, which also needs low temperatures to cool its superconducting magnets.

In the following text, we describe first how 4 K temperatures are obtained, and then focus on 15 mK wet and dry dilution refrigerators. These cryogenic technologies are central to the operation of many quantum computers and will need to integrate many innovations to accommodate the growth of quantum computers with large numbers of physical qubits.

2.1.1 4K stage cryogenics

In the quantum technology field, 4 K cryogenics can be handled in two key ways: compressors with pulse tubes, or helium liquefiers. The first liquefaction of helium was achieved in 1908 in Leyden, the Netherlands, by Kamerlingh Onnes. It is currently used to cool superconducting magnets from the CERN LHC as well as from the nuclear fusion ITER prototype reactor and many other large-scale physics experiments [3014].

Compressors and pulse tubes. A pulse tube has no moving parts at its cold end. The pressure wave feeding it is generated either by a valveless Stirling-type linear compressor or by a Gifford-McMahon type compressor with rotary valves, the latter being the most frequently used, particularly at CryoMech. It uses a piston. Stirling engines are used to cool infrared devices but not in dilution systems. It can be seen in the curve on the right of Figure 338 that the available cooling power decreases rapidly with temperature. It provides a cooling power that currently sits around 1 W at 4 K and 50 W at 50 K (Table 12).

There are no moving mechanical parts inside a cryostat, either in the pulse tube or in the dilution circuit. This avoids the generation of unwanted vibrations that could disturb the wiring and the qubits, which are extremely sensitive. The flow of gases and liquids produces very little disturbance in the dilution circuit.

Figure 335: A market map of enabling technologies vendors. © Olivier Ezratty, 2020-2026.

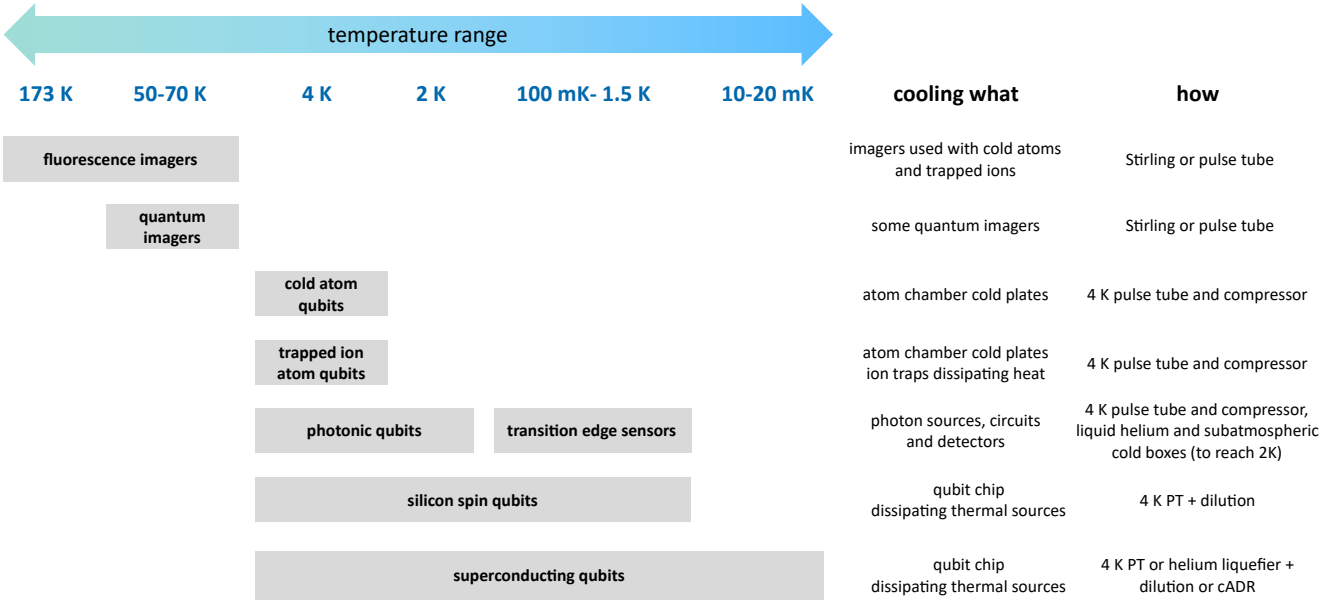

Figure 336: High-level overview of the cryogenic needs per qubit type and technology, why, and how it's done. The range is broad with solid-state qubits due to the stage thermalization occurring in cryostats across many levels (cold plates) from 50 K down to the qubit operating temperature. ⓒ Olivier Ezratty, September 2026.

A refrigeration system is evaluated with its coefficient of performance (COP), the ratio of the heat lifted at the cold stage to the electrical power drawn at the wall, and with the ratio of that COP to the Carnot COP for the same temperatures. This cycle describes a perfect thermodynamic cycle using four perfectly reversible thermodynamic processes involving work-heat exchange. No real machine reaches the Carnot COP.

Between a 300 K sink and a 4.2 K cold stage, the Carnot COP is $T_c/(T_h - T_c) \simeq 1.4\%$, meaning an ideal machine would draw 70 W of input power per watt of heat lifted at 4.2 K [3015]. A commercial 4 K pulse tube needs about 10 kW per watt of heat lift, some 140 times the Carnot input, which corresponds to a COP of about 10^{-4}, or roughly 0.7% of Carnot. These figures are wall-plug electrical power for the compressor at its rated load and do not include the chiller.

The pulse tube compressor must be cooled, usually with water. Regular water-air based cooling systems add about 2 kW per pulse tube to the energetic bill.

Helium liquefiers. In the quantum computing realm, helium liquefiers are now a thing. They will be used at least in two situations.

One is with the large PsiQuantum datacenters being built in Brisbane (Australia) and Chicago (USA). They will cool large cabinets hosting their photonic silicon chips as well as some cryo-CMOS control electronics at temperatures ranging from 2K to 4K. This will be based on a two-stage cooling system. The first one will generate 4.5 liquid helium with a liquefier. The second stage cools this liquid helium down to an operating temperature of about 2K. It is using a mix of Joule-Thompson valves to vaporize LHe and so-called subatmospheric cold compressors that pumps the subatmospheric helium vapor [3014, 3017]. It also uses subatmospheric heat exchangers.

The second use case is for large-scale superconducting computers like the future IBM Starling and Bluejay planned for 2029 and 2033. They will also both rely on centralized liquid helium production, feeding their cryostats, which will be completed by conventional dilution refrigerators.

These large-scale systems rely on a modular architecture, allocating more space for all control electronics, enabling multi-chip installations on cold plates and cryogenic interconnect between these modules. Bluefors and Maybell Quantum were the first cryogenic vendors to adopt this approach in 2026.

The industry vendors in that space are Air Liquide (France), Linde (Germany), Chart Industries / Cryo Technologies (USA), Fullcryo (Beijing Sinoscience Full-Cryo Technology, China) and Demaco (the Netherlands). Liquid helium cryogenic installations like Helial SF from Air Liquide offer a cooling power of 100 W to 1 kW at 4 K.

2.1.2 Dilution refrigeration

Superconducting qubit quantum computers from IBM, Google and others are frequently pictured as gold chandeliers containing wires, various devices and circular plates segmenting the central column into different sections. The systems combine passive and active control electronics that reach the qubits processor and control the low temperature cooling system. The bottom section of the chandelier houses the quantum processor. The chamber must isolate the chip from unwanted distur-

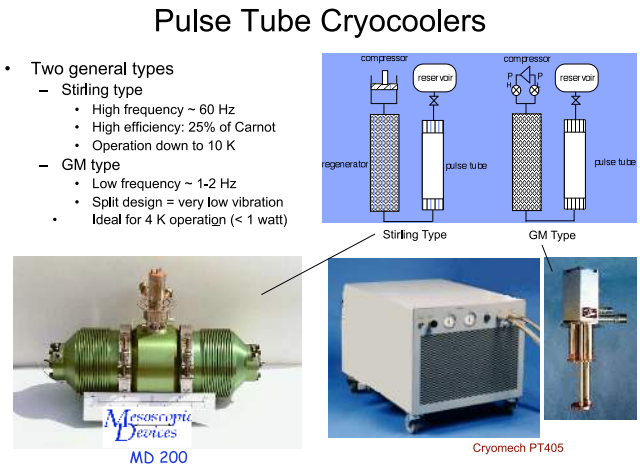

Figure 337: Pulse tubes models with Stirling and Gifford-McMahon types. Source: [3016].

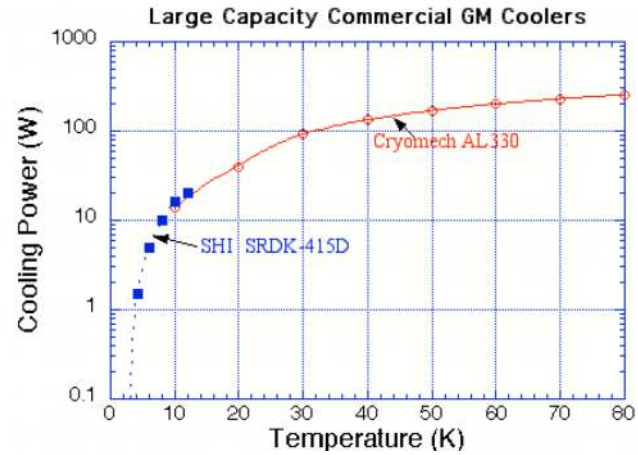

Figure 338: Commercial cryocooler capacities available in 2010. Source: [3016].

Vendor	Model	Type	$\dot{Q}$ @ 4.2 K	$\dot{Q}$ 1st stage	Input power (compressor)
Bluefors/Cryomech *(USA)*					
Cryomech	PT410	PT	1.0 W	40 W @ 45 K	∼ 8 kW [3018]
Cryomech	PT415	PT	1.5 W	40 W @ 45 K	9.2/10.7 kW, CP1110 [3019]
Cryomech	PT420	PT	2.0 W	55 W @ 45 K	∼ 11.5 kW, CP1114 [3019, 3020]
Cryomech	PT450	PT	5.0 W	65 W @ 45 K	n.d. [3019]
Sumitomo *(Japan)*					
SHI	RP-062B	PT	0.5 W	30 W @ 65 K	6.5–7.2 kW, F-50 [3021]
SHI	RP-082B2	PT	1.0 W	40 W @ 45 K	6.4/7.7 kW, F-70 [3021, 3022]
SHI	RP-182C2S	PT	1.5 W	42 W @ 45 K	∼ 7 kW (water-cooled) [3021]
SHI	RDK-415D	GM	1.5 W	35 W @ 50 K	6.5–7.2 kW, CSA-71A [3021]
SHI	RDE-412	GM	1.25 W	60 W @ 48.5 K	6.0 kW, F-50L [3023]
China vendors					
CAS (domestic)	home-made	PT	1.5 W	45 W @ 45 K	domestic compr., n.d. [3024]
SUSTech	home-made	PT	LHe reached	large cap.	n.d. [3025]
CASQI	(integrated)	PT	n.d.[a]	n.d.	n.d.
CETC	XS1000	PT	n.d.[b]	n.d.	n.d.
CryoPride	(CSSC Pengli)	GM/PT	n.d.[c]	n.d.	n.d.
Physike	(integrated)	PT	n.d.	n.d.	n.d.
Origin Quantum	SL400/SL1000	PT	n.d.[d]	n.d.	n.d.

Table 12: Cooling power at the 4.2 K stage and at the 50 K stage (with reference temperatures varying between 43 and 65 K depending on the vendor for common commercial 4 K pulse tube (PT) and Gifford-McMahon (GM) cryocoolers, with their related compressor input power in W. Two-value power figures are 50 Hz/60 Hz. All figures are as of September 2026, taken from manufacturer datasheets, and depend on configuration and measurement conditions. n.d. = not publicly disclosed by the vendor. *Notes:* [a]CASQI (2024 CAS Institute of Physics spinout) reports system-level DR performance of 6.6 mK and 2000 μW @ 102 mK using PT precooling, without cold-head load maps. [b]CETC 16th Institute produces ∼1000 GM cryocoolers/year, XS1000 is a dry DR (2025). [c]CSSC Pengli is the second mass producer of 4 K GM cryocoolers worldwide after SHI. [d]Origin (Benyuan) SL1000 DR delivers ≥ 400 μW @ 100 mK. 🅭 Olivier Ezratty, 2026.

bances, requiring control over temperature, magnetism, vacuum, and even mechanical vibrations.

The central column is the refrigerated part of a quantum computer with superconducting or silicon qubits. It is divided into stages, with the warmest sections at the top as shown in Figure 339:

- On the upper level, a plate, not represented in most illustrations, is thermalized at 50K. This is where both the electronic cables for controlling and reading the qubits as well as the fluids used for refrigeration arrive in the cryostat.
- One level below, running at 4K, i.e., 4°C above absolute zero (273.15°C), sits the lower part of the pulse tube, which achieves cooling through oscillatory compression and expansion of an ideal gas within a closed volume.
- The below plate is at around 800 mK. Between these two floors is the lowest temperature in space, which is

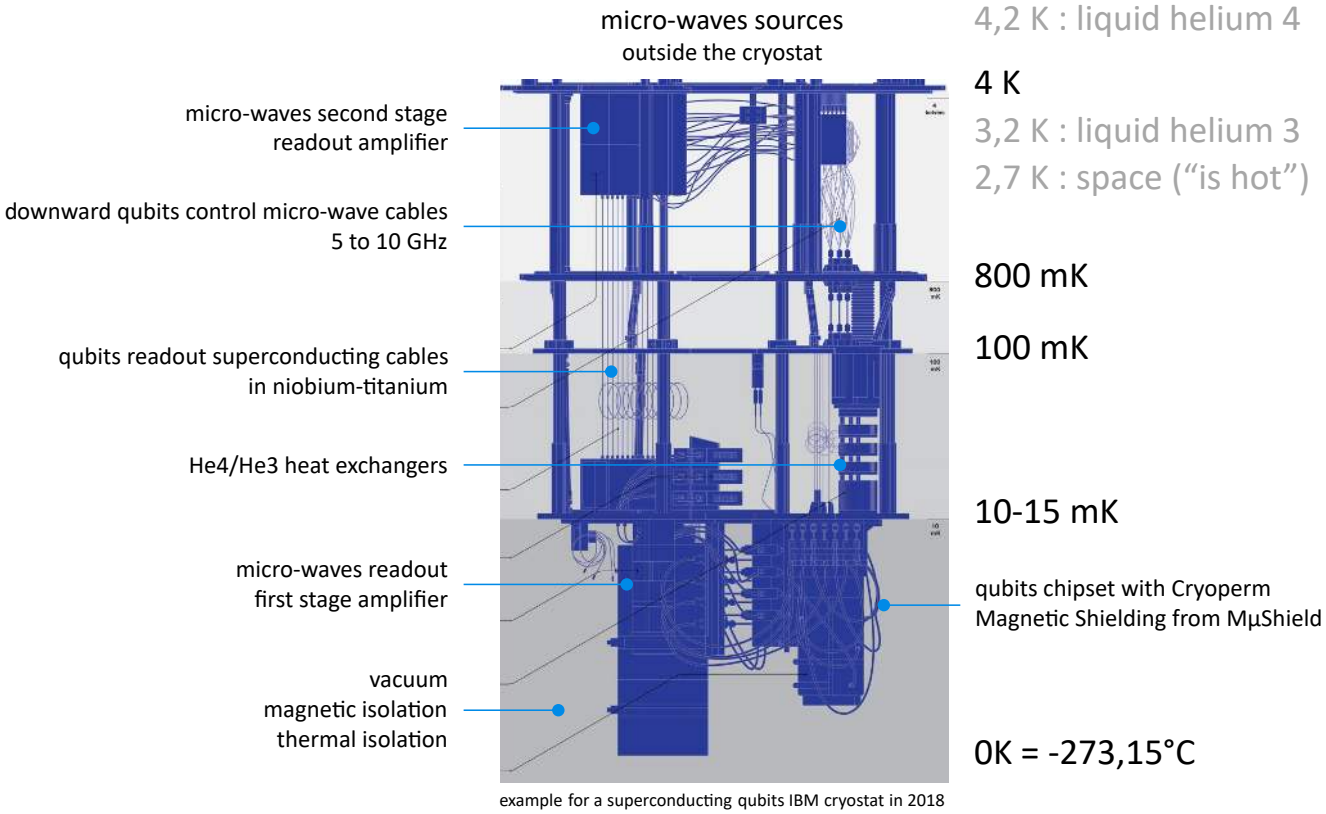

Figure 339: Interior of an IBM superconducting qubit cryostat. Image source: [3026] with legends added by Olivier Ezratty in 2018 and afterward. The overall scheme is still valid nowadays for small size superconducting qubits QPUs.

2.7 K and also corresponds to the cosmic background radiation.

- Another plate is generally located at a temperature of 100 mK.
- The lowest stage plate is where the quantum processor sits, and is cooled between 10 and 25mK, usually around 15mK. It is also called the "mixing chamber cold plate". A cold plate is a one-stage copper plate and the mixing chamber is the last level at the bottom of the dilution refrigeration system that we will explore later.

We will now study the detailed characteristics of the very low temperature cryogenics used in these superconducting quantum computers [3027–3029], show the difference between wet and dry dilutions, and then detail dry dilution installations and engineering.

Dilution refrigeration relies on a mixture of two helium isotopes, ^{4}He and ^{3}He, whose different quantum statistics give them complementary properties: ^{4}He is a boson and becomes superfluid, while ^{3}He is a fermion and behaves as a degenerate Fermi liquid. Helium was discovered indirectly in 1868 through the discovery of an unexplained spectral line in the light spectrum of the sun by astronomers Pierre Jules Janssen (1827-1907, France) and Joseph Norman Lockyer (1836-1920, United Kingdom). It was then isolated for the first time in 1895 by the Scottish chemist William Ramsay (1852-1916). The two isotopes have boiling temperatures of 4.2 K and 3.2 K respectively. ^{4}He becomes superfluid at 2.17 K while ^{3}He becomes superfluid at a much lower temperature, 2.49 mK on its melting curve at 34.3 bar and only 0.93 mK at saturated vapor pressure [3030, 3031].

The dilution cryostat concept was proposed by Heinz London in 1951 and was tested in 1965 at the University of Leiden, when it reached 220 mK. The record temperature went down to 60 mK in 1972 and then to 1.75 mK in 1999. Such a refrigerator exploits the finite solubility of ^{3}He in ^{4}He. Below about 870 mK the liquid mixture separates into a concentrated phase, almost pure ^{3}He, floating on a dilute phase where a few percent of ^{3}He is dissolved in superfluid ^{4}He. Cooling arises from the enthalpy of mixing as ^{3}He crosses the phase boundary from the concentrated into the dilute phase inside the mixing chamber, an endothermic process that continues down to the millikelvin range because the solubility of ^{3}He in ^{4}He stays finite, near 6.6%, as the temperature goes to zero. A third, gaseous ^{3}He phase is pumped away from the still, which sits higher in the circuit. Let's explain first why helium is so important for low temperature cryogenics. Hydrogen becomes liquid at 20.3 K, nitrogen at 77.4 K and oxygen at 90.2 K. These gases are useless for low temperature cryogenics. Liquid hydrogen cryogenics uses spin variations of hydrogen, instead of isotopic ones. H_2 molecules exist in two forms, with both hydrogen atoms having the same spin (orthohydrogen) or an opposite spin (parahydrogen). At 300

K, the ratio is 75% orthohydrogen and 25% parahydrogen. At low temperature, the ratio is different and the conversion between orthohydrogen and parahydrogen is exothermic, used in the refrigeration process.

On the other hand, ^{4}He liquefies at 4.2 K at ambient pressure and a ^{4}He cryostat can reach 1 K, while ^{3}He cryostats can go as low as 300 mK (Figure 342). A ^{3}He–^{4}He mixture powers dilution refrigerators reaching 15 mK. Note the low density of ^{4}He which is 125 g/L at 4.2 K.

There are two types of dilution refrigerators: "dry" and "wet".

Wet dilution refrigerators are built with a first system that cools the enclosure to 4K with liquid ^{4}He. A second so-called dilution system uses a mixture of liquid ^{4}He and ^{3}He with a flow circulating in ducts connecting the metal plates down to less than 15 mK in the bottom stage. Wet dilution systems were used until the early 2000s (Figure 343). They were then largely replaced by dry dilution systems that are simpler to operate, especially to create quantum computers that are easy to install at customer sites, thanks to avoiding liquid helium. However, wet dilution systems are still used for various physics experiments where the dry system is not appropriate, but usually not for quantum computing.

One interesting breed of wet dilution cryostats is the inverted dilution refrigerator (IDR). These inverted cryostats enable fast and easy experiment samples loading and fast cooling as well. Figure 340 shows an example IDR from Nicolas Roch's laboratory at Institut Néel.

The team then created in 2026 an ultracompact IDR reaching 70 mK and weighing only 3 kg, with a diameter of 10 cm, and a fast cooldown and warm-up cycle time of about two hours with a loaded configuration [3032]. It provides 20 μW of cooling power at 100 mK with only one liter of ^{3}He gas. It was used to test fluxonium superconducting chips (Figure 341). While it is not documented in the paper, I suspect that the 4 K cooling is done with liquid ^{4}He since Institut Néel has a centralized liquid helium cooling plant. They would then not need a compressor and pulse tube, only the external gas-handling pumps that circulate ^{3}He.

While most cryostats for quantum computers use dry dilution refrigerators, Fermilab is currently putting the final touch on an impressive wet dilution system developed to house a 3D supercomputing system, probably co-developed with Rigetti. Its numbers are impressive: it provides 625 W of cooling power at 4.5 K, 50 W at 2 K and, above all, 300 μW at 20 mK for a load fitting in a 2 m wide cylinder. And it is using 2000 liters of liquid helium [3033]. What is interesting here is that 625 W cooling power at 4.5 K could have another application: superconducting (non-quantum) computing [3034].

Dry dilution refrigerators or so-called cryogen-free refrigerators do not use a liquid helium bath. The two isotopes are stored and handled as gas at room temperature, and condensed inside the cryostat. Like wet systems, they have two stages: the lower dilution stage is essentially identical, with ^{3}He crossing the phase boundary into the dilute ^{3}He–^{4}He phase inside the mixing chamber. This covers cooling below 1 K.

The upper stage relies on the pulse tube technique that manages cryogenics down to about 2.8 K with ^{4}He gas and a large external water-cooled compressor. This technique has been mastered for about twenty years and has been progressing incrementally since then. Its arrival coincides with the first experiments with superconducting qubits. Dry dilution refrigerators are generally used for qubit cryogenics that require operating temperatures below 1 K. Figure 344 explains how it works.

The circuit shown in red in Figure 345 is used to pre-cool the cryostat in the thermalization preparation. This is done in three steps: first, by starting the pulse tube which cools the 50 K and 4 K stages with ^{4}He gas and the external compressor of about 12 kW, in yellow.

Then by using the pre-cooling circuit which will circulate a ^{3}He–^{4}He mixture to the lower stages, and which will have been cooled by the pulse tube, in the circuit in red in the diagram. At CryoMech, the compressors adapted to these dilution systems consume from 7.9 to 12 kW, from the PT410 to the PT420. About 4 kW must be added for the gas handling system (GHS), which manages the dilution circuit with their pumps and controls as well as for the computer and the assembly dashboard.

Finally the dilution circuit takes over from the pre-cooling stage and brings the lowest cold plate down to 15 mK (in light blue).

Adopting a space rocket analogy, the pulse tube and its 7 to 12 kW compressor are the equivalent of the first stage of a Saturn V Apollo launcher. The pre-cooling system is the analogue of the rocket second stage, and the dilution system is the equivalent of the third stage that sends the lunar module and the LEM to the moon, here, the chip. Extracting the Earth's gravity over a large mass is equivalent to cooling a large metal mass inside the cryostat to 50 K and 4 K. While the dilution system is responsible for cooling a smaller mass from 4 K to 15 mK, the lower cold plate and the payload attached to it.

These systems must be optimized by considering a large number of parameters. The modeling of a cryostat could one day benefit from quantum computation, especially since the fluids used are in a superfluid quantum state. There are even digital twins developed for such systems [3037].

A good part of the power is used to lower the temperature to 1 K, because that is where the mass to be cooled is largest. The cylinder that protects the part cooled at 4 K receives thermal radiation coming from the 50 K stage. This makes a big thermal difference to absorb.

A single-dilution 15 mK cryostat of the LD or XLD class draws about 16 kW of wall-plug electrical power

Figure 340: Custom made inverted dilution refrigerator (IDR) cryostats made at CNRS Institut Néel in Grenoble. Pictures source: Olivier Ezratty, added in 2022.

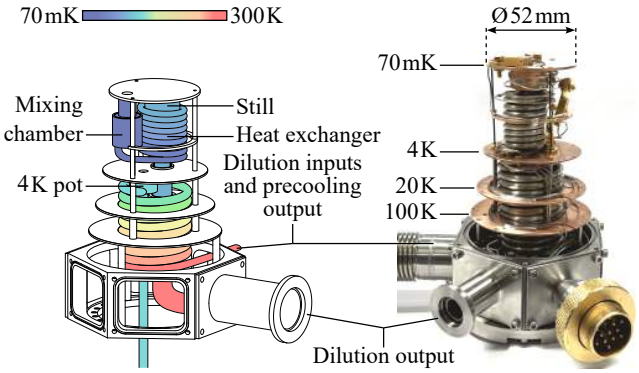

Figure 341: A smaller IDR created at CNRS Institut Néel in Grenoble in 2026. Source: [3032].

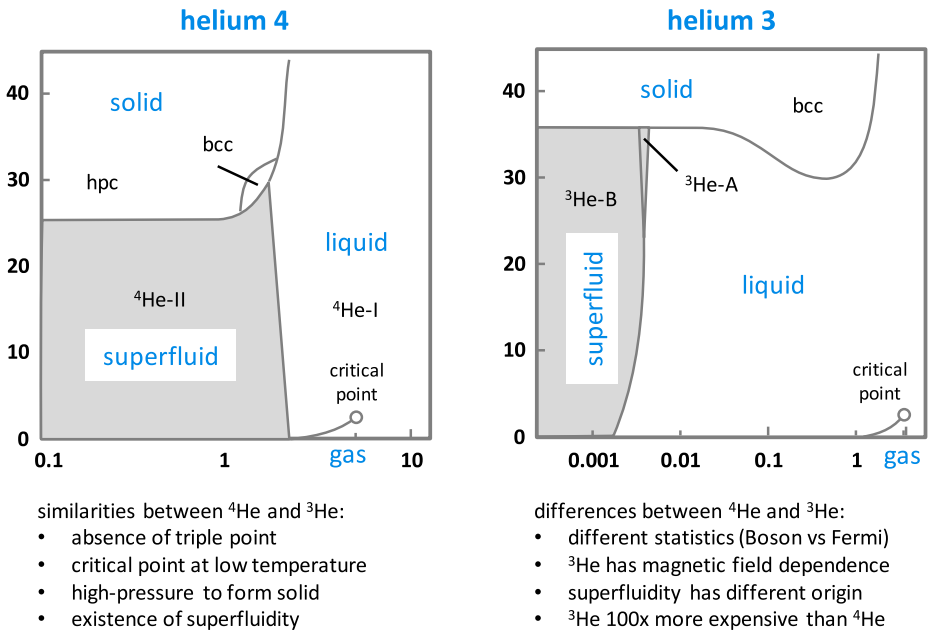

Figure 342: Phase diagrams of ^{3}He and ^{4}He. Bcc means body-centered cubic and hcp, hexagonal close-packed. These are two states of solid helium which are of no interest in dilution refrigerators. A phase diagram shows the phase of the element as a function of temperature (in X in logarithmic scale) and pressure conditions (in Y, 1 bar = atmospheric pressure). It shows that in the regime used below 1 K, ^{3}He is a normal liquid and ^{4}He is superfluid. This difference makes it possible to operate refrigeration at these low temperatures. Source: [3035].

once thermalized, with a NISQ-scale payload: about 12 kW for the 4 K pulse tube compressor, about 1 to 2 kW for the dilution unit, which contains the gas handling system (GHS) pumps and their control electronics, and about 1 to 2 kW for the water/air chiller that cools the compressor water loop. These are indicative figures for one class of commercial systems, not a specification: they scale with the cryostat model, the number of pulse tubes and dilution units, the payload and the ambient conditions. The dilution circuit uses gas-handling pumps to circulate ^{3}He, and these are distinct from the compressor that drives the pulse tube cryocooler. The circuit needs no compressor of its own because the returning ^{3}He is condensed after being pre-cooled by the pulse tube. In practice, nearly all the heat extracted from the cryostat is rejected through the water-cooled pulse tube compressor.

Figure 345 details the operation of the dilution system as well as the phase (liquid or gaseous) and the concentration of ^{3}He and ^{4}He in each stage and component. It shows the descending circuit of ^{3}He, which condenses in the condenser fed by the still, before being cooled further in the heat exchangers.

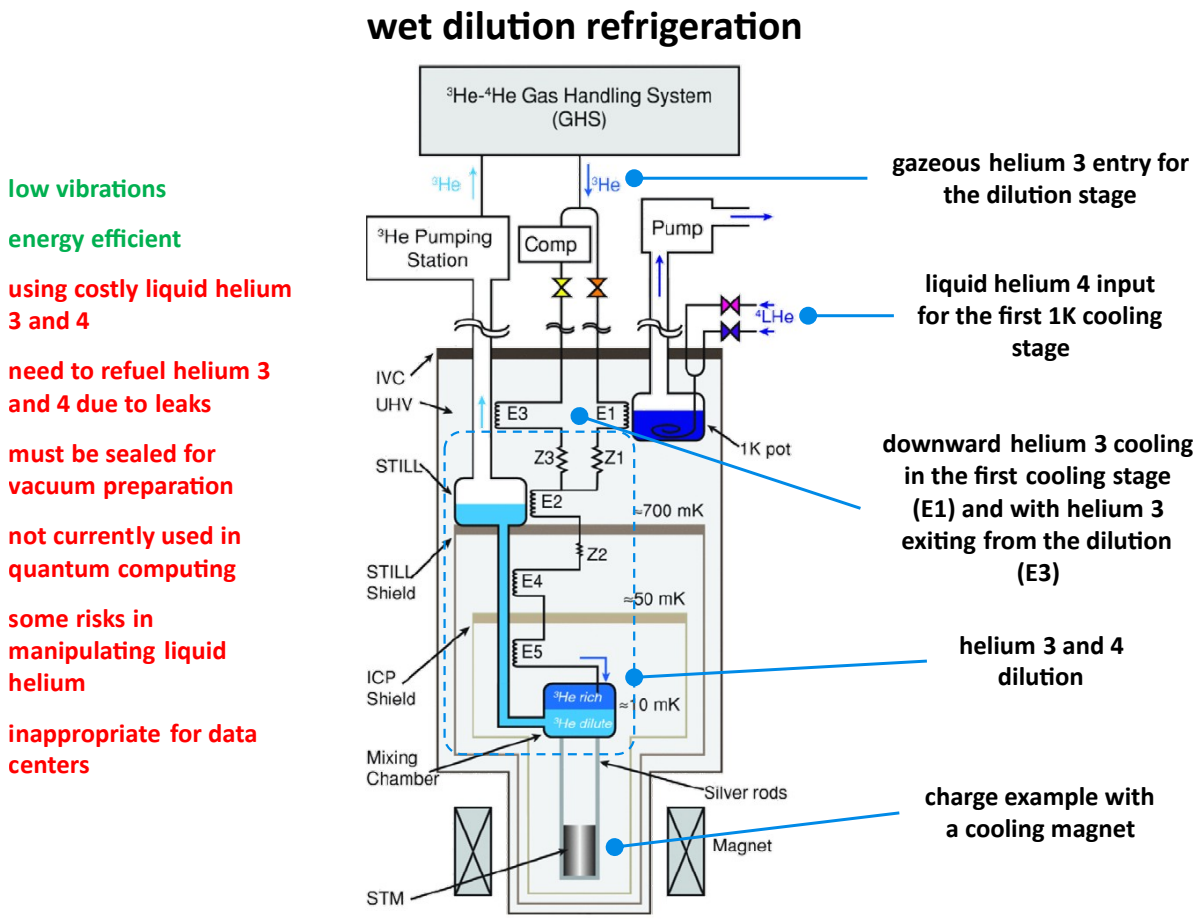

Figure 343: Wet dilution refrigerator operations. Schema from [3035] and legends from Olivier Ezratty, 2020.

In the circuit going up from the mixing chamber, the dilute phase rises, mostly superfluid ^{4}He carrying a few percent of ^{3}He, and the ^{3}He concentration falls as the stages go up. The still, held around 600 mK to 800 mK, is where ^{3}He becomes gaseous: the vapor pressure of ^{3}He is roughly two orders of magnitude above that of ^{4}He at this temperature, so the still preferentially evaporates ^{3}He from the dilute phase rather than mechanically separating it from the ^{4}He. Phase separation and the cooling itself happen in the mixing chamber, not in the still. The superfluid ^{4}He stays liquid and tends to creep upward as a film, which is blocked by a film burner or a constriction that sends it back down.

The ^{3}He arriving in the mixing chamber must reach it within about 1 mK of the mixing chamber temperature. It is pre-cooled by the cold dilute stream moving upward. The only way to achieve this is to increase the contact surfaces, which is done in the discrete heat exchangers just below the cold plate at the 100 mK level.

Cryogenics at 10-20 mK is specific to quantum computers whose qubits must be cooled at very low temperatures, mainly those based on electrons (superconducting, electron-spin and Majorana-based qubits). Theoretically, silicon qubits should only need cooling to 1 K, but for the moment they are still cooled to about 15 mK. An Australian team created a proof of concept of silicon qubits running even at 1.5 K and another one from Intel and QuTech at 1.1 K [1316, 3038].

To reach **lower temperatures**, below 3 mK, a complementary technique is used, adiabatic nuclear demagnetization (see its description in the Kiutra vendor part later). Laser and evaporative cooling can produce ultracold atomic ensembles with subnanokelvin motional temperatures, using magneto-optical traps and the like. These are not bulk refrigeration platforms and these numbers are not cryostat base temperatures: they characterize the motional state of a dilute trapped gas, with no usable cooling power for a payload. There is a connection between Landauer's bound, the creation of quantum pure states and Nernst's unattainability principle, according to which infinite resources (time, energy) are required to cool a system to absolute zero temperature. Thus, a new Carnot-Landauer limit that generalizes Landauer's principle was formalized [3039].

Dry dilution setup. It is divided into two large parts with the compressor, pumps, liquid nitrogen and helium gas reservoirs positioned in one room, and the refrigerated enclosure in another room. This is quite logical since the compressor will generate heat that will have to be dissipated, via an incoming and outgoing water pipe [3040, 3041].

Here are some key engineering aspects of these setups:

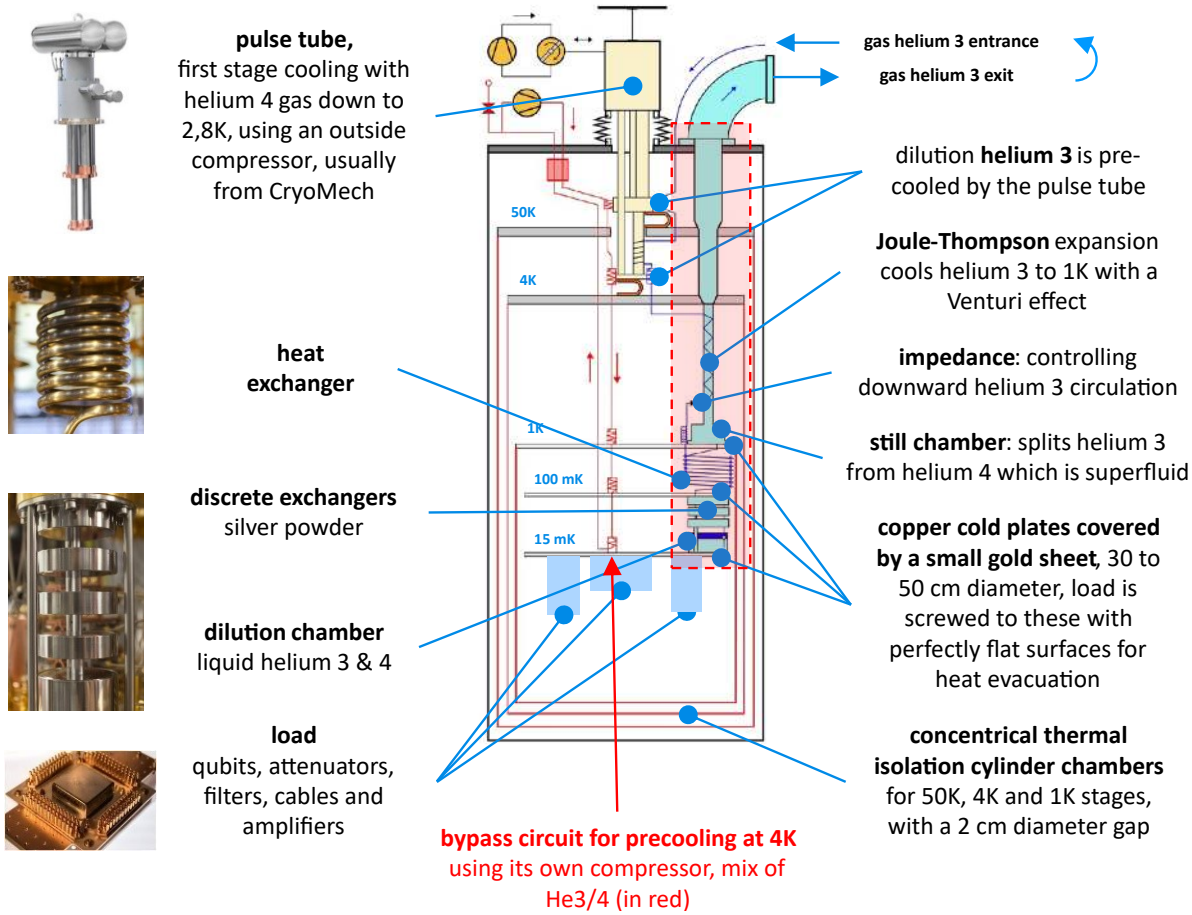

Figure 344: Dry dilution schematic inspired from [3035], illustrations from CryoMech documentation, Janis, [3036] and IBM.

- **Safety**. With dry dilution refrigerators, the safety constraints are quite light compared to wet versions (see a typical setting in Figure 346). Wet dilution uses up to 80 liters of liquid helium which could drive a cryostat explosion if heated too abruptly because the expansion of the gas is important compared to its liquid state, with a ratio of 1 to 700. It was necessary to handle liquid helium canisters and fill tanks with protective equipment against splashes. The oxygen level in the room could also dangerously decrease due to the accidental evaporation of nitrogen or liquid helium. Contact with cryogenic materials, particularly carbon steel, should also be avoided. Rooms must be large enough, and care must be taken in the upper areas where helium may accumulate, since it is lighter than air.

  Thermal contraction, and differential contraction between dissimilar materials, can be significant at cryogenic temperatures. This has an impact on the design of the whole device and the choice of materials. The materials that can be used are special steels with nickel, chromium, aluminum, bronze, copper, composite materials, niobium-titanium for wiring, nickel-copper alloys, indium for joints, kapton and mylar for insulation.

- **Vacuum**. The cryostat is usually placed in vacuum. The management of high vacuum and ultra-high vacuum (UHV) are industrial specialties. Cryostats of superconducting and silicon quantum computers only require high vacuum, of the order of 10^{-5} to 10^{-6} mbar in the vacuum can before cooldown. They use commercially available pumps from e.g. **Pfeiffer** (Germany). Pumping only takes place when the system starts up and is deactivated once the system is thermalized at low temperature. Cooling down to 15 mK does not require active ultra-high vacuum pumping: cold surfaces cryopump most of the residual gases, which improves the vacuum inside the can. The effect depends on the gas species and on the surface temperature, since helium and, to a lesser extent, hydrogen are poorly cryopumped and end up setting the residual pressure. Using too much pumping to generate ultra-high vacuum could propagate dust from these solidified gases, damaging the qubits or the rest of the equipment in the cryostat. Ultra-high vacuum is used for cold atom-based computers.

- **Thermal leaks** are coming from cables entering and leaving the enclosure or radiation as well as from various passive and active dissipative electronic components (filters, attenuators, circulators, and amplifiers sitting at the dilution stage or the 4K stage). Numerous layers of thermally insulating materials are integrated into the cryostat. They are cylinders stacked upside down like Russian dolls. It is made of

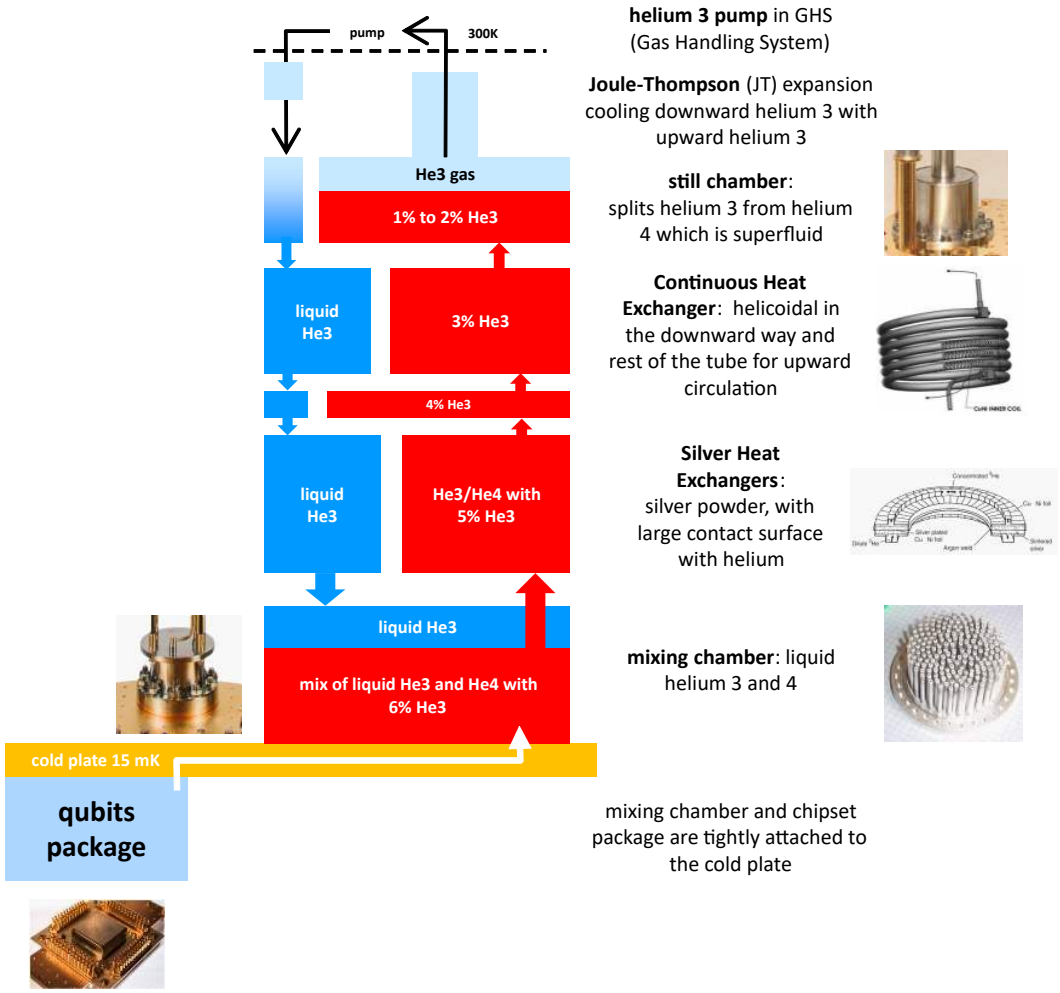

Figure 345: Details of the dilution inner working and the ^{3}He and ^{4}He phases that are used. Olivier Ezratty, 2021.

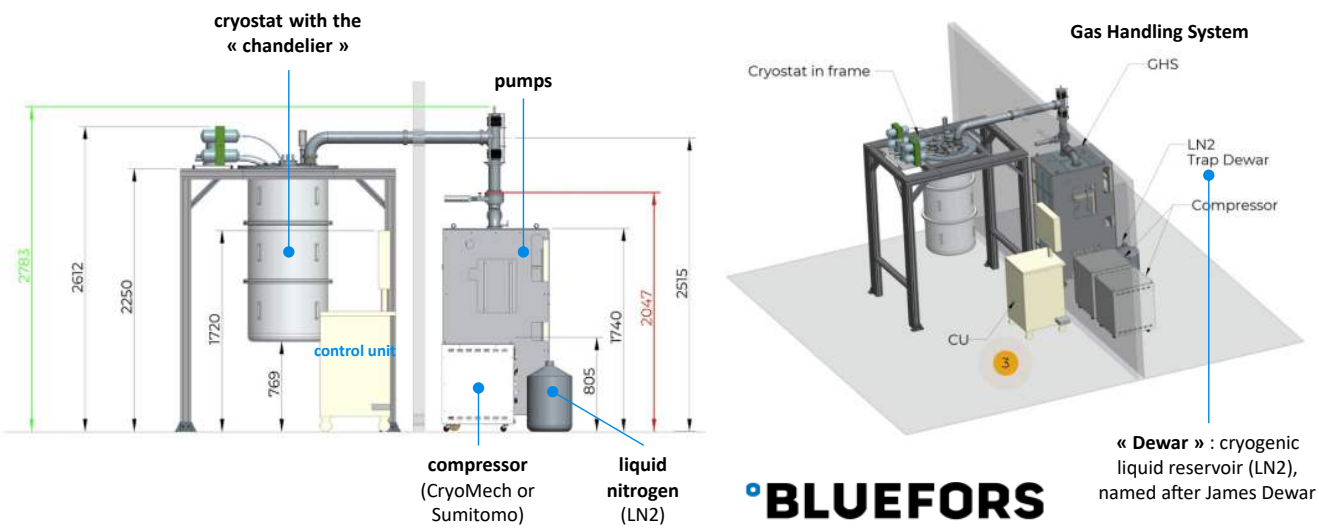

Figure 346: Bluefors recommendations for setting up one of their dilution refrigerators. Source: Bluefors documentation.

aluminum, copper and steel. Each cylinder and plate acts as a thermal insulator vs the lower cylinder.

- **Magnetic isolation**. The quantum chip is magnetically isolated from the outside. Magnetic isolation uses several Russian doll enclosures made of various alloys, including **Mu-metal,** an alloy of nickel, iron and molybdenum, aluminum alloys and other superconducting alloys. The quantum processor can also be magnetically shielded. IBM uses a Cryoperm Magnetic Shielding from **MμShield**.

- **Superconducting magnets**. Apart from this magnetic isolation, cryostats in research laboratories may be supplemented by superconducting magnet systems that occupy the lower part of the cryostat cylinder. They have a cylindrical shape that surrounds a measuring instrument. These magnets are also supplied with liquid helium to guarantee the superconducting effect that is used to generate intense magnetic fields of several teslas. These magnetic fields are used to set up various experiments, particularly in astronomy or fundamental physics. They are sometimes used in quantum computing, especially with silicon qubits for electron-spin control. Magnets producing fields of several teslas can be installed in a cryostat. At D-Wave, the magnetic field is reduced to about 1 nT in the computer enclosure, compared to the Earth's magnetic field, which can reach 65 μT, giving us a ratio of 1 to 65,000. D-Wave communicates on a ratio of 1 for 50,000.

- **Liquid nitrogen**. These dry cryostats still use a cryogen, liquid nitrogen at 77 K, to filter helium gas and remove impurities (LN_2 for liquid nitrogen, gaseous nitrogen being a molecule of two nitrogen atoms). This filtration is based on zeolite powder, made of microporous aluminosilicate crystals. The liquid nitrogen tank used for this pre-cooling is called a "cold trap". It contains about 20 liters of liquid nitrogen that must be replaced every three weeks in NISQ superconducting qubits systems. This filtering is completed in the cryostat 4 K stage by another filtering system based on activated carbon powder which works better at low temperatures and increases the contact surfaces with the gas to better filter it. There is the possibility to use the 50 K stage of the cryocooler to filter the incoming ^{3}He into the dilution unit to replace the liquid nitrogen tank. The mounting is two filters in parallel where you can use one when you clean the other. This is not standard yet but can entirely remove cryogenic liquid waste from the system. Liquid nitrogen is also sometimes used to pre-cool the metallic structure of the cryostat during the warm-up. This is unrelated to the helium circuit. This can save up to five hours for the cryostat thermalization. But this process is not commonly used for quantum computer cryostats. It is used for precooling heavier payloads for physics experiments using equipment weighing up to several hundred kilograms, including superconducting magnets. This technique is not used for quantum computing.

- **Thermalization**. The complete thermalization of a quantum computing cryostat takes about 24 hours. The so-called "1K" stage was actually cooled at about 1.2K in wet cryogenics and is around 800 mK for dry cryogenics. Power consumption is identical between the thermalization phase and the temperature maintenance of the instruments once the thermalization is completed.

- **Cold plates** are located at each cooling stage of the cryostat. That's where various experimental devices are attached. They are generally made of 99.99% pure copper with very low oxygen content to maximize their thermal conductivity. They are "OFHC" for oxygen-free high thermal conductivity. Cold plates are also covered with a few microns thick layer of gold which serves as a protection against oxidation and radiation. It also has good thermal conductivity and is soft, which is very useful for solidly anchoring and cooling all the attached components. Figure 347 shows an example of a BlueFors cryostat cold plate. These plates are custom perforated to allow all the cables to pass through, not including the cryostat components. All the holes must be used to avoid thermal leaks between the bottom and top of these cold plates. Infrared rays must be prevented from passing from one level to another and generating downward heat leakage. These plates act as nested light-tight radiation shields, reducing the radiative heat load and the stray photons reaching the coldest stage. The trend is to increase the size of the cold plates, with a diameter reaching 50 cm. Knowing that their size is slightly decreasing from the top to bottom cold plates because of the concentric cylinder shields surrounding them.

  In cryostats for quantum computers, the current standard for the bottom plate is 30 cm to 40 cm for research and 50 cm in production, to accommodate more electronic components. It could soon reach 100 cm. Infrared photons are filtered with an **Eccosorb** resin that surrounds the superconducting cables in the lowest stage of the system. This resin is a mixture of epoxy and metal powder. It is a laminated structure of polyurethane foam generating a controlled conductivity gradient. It is injected into copper filters (OFHC) that surround the cables in the coldest stage of the cryostat as shown in Figure 348 [3042, 3043]. The resin is usually supplied by **Laird Performance Materials** (UK), a subsidiary of Dupont. An alternative using sapphire sphere in epoxy resin is being developed to provide better infrared shielding [3044].

- **Lower temperatures**. To reach ultra-low temperatures of 1 mK and below, continuous nuclear demagnetization refrigeration (cNDR) can be used, in complement with dry refrigeration [3031, 3045]. It is different from continuous adiabatic demagnetization refrigeration (cADR), which relies on the electronic spins of a paramagnetic salt and stops around 10 to 50 mK. This temperature is required for some physics experiments but not with solid-state based quantum computers (superconducting or electron spin qubits). At such a low temperature, the cooling budget is equally super low, at just 20 nW, and the residual heat leak of the demagnetization stage itself sits in the nW range. As we will see with Kiutra, cADR

Figure 347: Cold plate with a gold finish which is used to facilitate the assembly with experimental devices and optimize thermal conductivity. Photo: Bluefors.

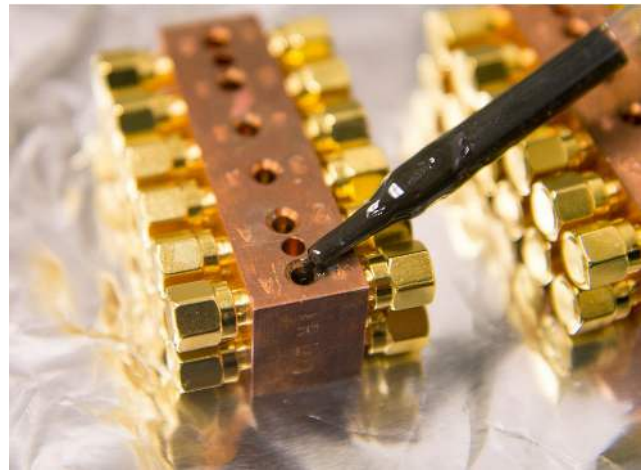

Figure 348: How the Eccosorb resin is injected in the filters.

can also be used in place of a dilution to generate 10-20 mK.

Cooling budgets. The level of cooling power at ultra-low temperature is quite low. This limits the energy that can be released by the qubits themselves and by the microwave attenuation and amplification circuits used to read the state of the qubits. Table 13 compares these cooling power budgets by supplier, with the base temperatures and mixing chamber cold plate diameters. The Bluefors dilution refrigerator thermal budget ranges from 12 μW (LD250) to 34 μW (XLD1000) at 20 mK, and from 250 μW (LD250) to 1,000 μW (XLD1000) at 100 mK. Quantum Design / Oxford Instruments' TritonXL also has a thermal budget of 1,000 μW at 100 mK but with two pulse tubes, while the Proteox reaches 500 μW with only one pulse tube. It is completed by a removable system for qubit control cables supporting up to 140 [3046]. The **FormFactor** JDry-500-QPro, inherited from **Janis ULT**, has a thermal budget of 14 μW at 20 mK and 500 μW at 100 mK (*above*, in-house compilation). At the 4 K stage, the available thermal budget is around 1 W to 2 W with a single pulse tube. Multiple pulse tubes can be combined in the same cryostat to augment the cooling power at 4K, and multiple dilutions as well for the 10-20 mK level. This is the case with the Bluefors KIDE system.

The thermal budget of the coldest stage is conditioned by the equation: $\dot{Q}_m = 84\,\dot{n}_3 T^2$ where $\dot{Q}_m$ is the cooling power in W, $\dot{n}_3$ is the molar flow rate of ^{3}He crossing the phase boundary in mol/s and T is the mixing chamber temperature in kelvins [3052]. This law that can be simply called "Q=84NT2" explains that the thermal budget at 15 mK is very low compared to the cooling budget available at the upper stages (up to 25 μW at 15 mK, 1 mW at 100 mK and 1.5 W at 4 K).

There is another constraint related to the Kapitza resistance. It limits heat exchange between the liquid ^{3}He and the heat exchanger walls. The heat flow across a solid-to-helium boundary scales as $A(T_1^4 - T_2^4)$, so it collapses as T^4 when the stage gets colder. Lowering the operating temperature by a factor of 10 therefore requires multiplying the exchange surfaces in the lower parts of the dilution system by 10,000 to transfer the same heat! This is done using silver powders integrated into the discrete heat exchangers above the mixing chamber. These powders are structured to maximize the heat exchange surface area with the liquid ^{3}He flowing through them. Their deposition process must maximize the flat contact surface with the small tanks where they are located. It is possible to increase cryostats cooling power by adding more cooling stages, improving their COP relative to Carnot, and multiplying the pulse tubes and dilution units.

2.1.3 Cryogenics vendors

We cover here the whole cryogenics vendor space covering the 4K range (compressors and pulse tubes) as well as the 10-20 mK range (dilutions).

The main suppliers of cryostats for quantum computers are **Bluefors** (Finland), which equips IBM, Rigetti and many others, **Quantum Design** (USA), which is used by D-Wave and Microsoft, **FormFactor** (USA), used by Google, **Maybell Quantum** (USA), **Leiden Cryogenics** (the Netherlands) [3053], which manufactures the most powerful cryostats on the market, used mainly for physics experiments, and **CryoConcept** (France), a branch of **Air Liquide** since 2020 but which discontinued its operations in 2025. The world market for cryogenic systems, all categories combined, was about $1.8B in 2020 [3054]. Market share wise, Bluefors leads the pack with over 70% and about €200M in revenue as of 2024. This inventory contains a lot of vendors from China, which has been investing a lot over the last decade to build up its self-sufficiency in the field.

Vendor	Model	PTs	Base T	$\dot{Q}$ @ 20 mK	$\dot{Q}$ @ 100 mK	MC cold plate
BLUEFORS	Ultra-Compact LD	1	n.d.	16 μW	500 μW	29.4 cm [3047]
	LD250	1	10 mK	12 μW	250 μW	30–50 cm
	XLD400	2	8 mK	14 μW	450 μW	30–50 cm
	XLD1000	2	8 mK	34 μW	1,000 μW	30–50 cm
	KIDE	9[a]	n.d.	n.d.[a]	n.d.[a]	hexag., $\sim$ 1.5 m [3048]
FormFactor	JDry-500-QPro	1	7 mK	14 μW	500 μW	50 cm
	JDry-600	n.d.	$<$ 10 mK	17 μW	630 μW	n.d.
Oxford Instruments	TritonXL	2	5 mK	25 μW	1,000 μW	43 cm
	TritonXL-Q	2 or 4	7 mK	25 μW	850 μW	50 cm
	Proteox	1	10 mK	$>$ 25 μW	500 μW	36 cm
	ProteoxLX	2	n.d.	25 μW	850 μW	n.d.
Leiden Cryogenics	CF2400 Maglev	2	4 mK	n.d.	2,000 μW	49 cm
	CF1400 Maglev	2	8 mK	n.d.	1,000 μW	49 cm
	CUORE custom	5	7 mK	3 μW @ 12 mK	n.d.	1-ton payload [3049]
Maybell	Big Fridge	n.d.	$<$ 10 mK	n.d.	n.d.	$>$ 4,000 cm^2 ($\varnothing$ 71 cm)
CASQI 中科量仪	L400	n.d.	n.d.	10 μW	400 μW	39.5 cm
	L1000	n.d.	n.d.	20 μW	1,000 μW	50 cm
	4-dilution proto.	2	6.6 mK	n.d.	2,000 μW[b]	n.d. [3050]
CETC 中国电科	XS1000	n.d.	$<$ 10 mK	n.d.	1,100 μW	n.d.
CryoPride	KDDR-1-400	n.d.	n.d.	12 μW	$\sim$ 400 μW	n.d.
本源量子 Origin Quantum	SL400	n.d.	n.d.	n.d.	$\geq$ 400 μW	336 coax lines
	SL1000	n.d.	n.d.	n.d.	1,000 μW	840 coax lines
PHYSIKE	Icecore-400/500	1	$<$ 10 mK	$>$ 12 μW	500 μW	40 cm
国盾量子 QuantumCTek	ez-Q	n.d.	10 mK	n.d.	450 μW	n.d. [3051]
ZL CRYOGENIC	ZL-DR400	n.d.	7.45 mK	18 μW	650 μW	30 cm
	ZL-DR1000	n.d.	n.d.	n.d.	n.d.	n.d.

Table 13: Comparison of commercial dry dilution refrigerators with their number of pulse tubes (PTs), base temperature, cooling power $\dot{Q}$ at the 20 mK and 100 mK stages, and mixing chamber (MC) cold plate diameter. The two cooling powers are interdependent: the mixing chamber obeys $\dot{Q}_m = 84\,\dot{n}_3 T^2$, so at constant ^{3}He flow the 100 mK figure should be about 25× above the 20 mK one. The observed ratios span 20× (LD250, Proteox) to 40× (TritonXL), which shows that vendors quote the two stages at different circulation rates rather than on a single operating point, and that these numbers should be compared with care. The best commercial figure at 100 mK is 2,000 μW, reached by the Leiden CF2400 and the CASQI 4-dilution prototype, and the lowest base temperature is 4 mK. Cold plate diameters have converged around 30 to 50 cm, the practical size being constrained by the concentric radiation shields. n.d. = not publicly disclosed. [a] the KIDE has nine pulse tubes and aggregates three dilutions, so its budget is roughly three times a single XLD unit, but Bluefors does not publish a consolidated figure. [b] measured at 102.5 mK on four parallel dilution units inside a single vacuum chamber. 🅭 Olivier Ezratty, 2020-September 2026.

Absolut System

France, 2010

Absolut System was created by Alain Ravex, former head of the low temperature department of the CEA in Grenoble in the 1980's and 1990's, then a consultant for Air Liquide. He sold the company to his partners and now consults for them and other players in the cryogenics field.

The company develops custom cryostats running at temperatures higher than 1.8K and targets a wide range of applications in research and in the industry, particularly for the production of liquid nitrogen. Their

customers include CEA-Leti, Thales, Air Liquide and Quobly. They are based near Grenoble.

They developed the ACE-Cube (Advanced Cryogenic Equipment), a cryogen free helium cryostat using a remote cooling technique. It is implemented for specific infrared detectors and semiconductors characterization and above 10K.

They also launched AFCryo (2017), a joint subsidiary in New Zealand, with Fabrum Solutions (2004) also based in New Zealand [3055].

Air Liquide

France

Air Liquide is a provider of liquid helium sources for high-power cooling of large QPUs. It has several undisclosed customers in the field.

Attocube

Germany, 2001

Attocube has different line of businesses including cryostats mainly targeting the research community. It sells the attoDry series, closed-cycle dry cryostats (with cooling temperatures ranging from 1.65K to 4K), and the attoLIQUID series (300 mK), liquid helium cryostats. They provide cryostats to Quandela for the cooling of their photon sources and SNSPD photon detectors.

Bluefors

Finland, 2007

Bluefors is the worldwide leader of low temperature cryogenic systems, using dry dilution with a market share exceeding 70% for dilution refrigerators. It is focused on the quantum computing market.

Company. The spin-off from Aalto University delivered overs 1,200 systems with its 600+ employees and a revenue of about €200M as of 2024. It has a broad range of dry dilution systems, with some cabling (coaxial, ribbon optical) and filters, QDevil X, codeveloped with **QDevil**. Bluefors acquired Cryomech (USA) in March 2023, the leader in 4K compressors. It has a manufacturing plant in Syracuse, north of New York State and also a startup lab in Delft, in the Netherlands.

Compressors. 4K compressors have two main components: a compressor (Figure 349) and a pulse tube (Figure 350). These are the first stage of dry dilution refrigeration systems. They use an expansion system of compressed gas outside the cryostat with no rotating parts in the cryostat. These pulsed tubes are used in particular in the semiconductor industry, in vacuum deposition machines (CVD, MOCVD) and plasma deposition machines. They are operating down to 10K, which is sufficient for semiconductor production. The compressor is water-cooled, with a flow rate of 5 to 12 liters per minute depending on the incoming temperature. But this water must also be cooled, and it can require up to an additional 10 kW of electric power unless the computer is located in a cool region.

Bluefors pulse tubes range includes the PT415 and PT420 (Figure 350). Its main competitor is the SHI Cryogenics Group subsidiary of **Sumitomo**. There are other pulse head and compressor manufacturers such as Fabrum Solutions (New Zealand) but the latter only targets temperatures of 77 K for liquid nitrogen production. These compressors are sold combined with their related pulsed tubes. At the APS March meeting in Las Vegas, in March 2023, Cryomech introduced a new high-range compressor (CP3000) and pulse tube (PT450) with a record cooling power of 5.0 W at 4.2 K. In March 2025, the range was extended at the bottom with the PT205, a compact two-stage pulse tube made for quantum sensing and quantum communication applications. It delivers 10 mW of cooling power at 2.5 K with a power drain of 1.3 kW. It can for example support superconducting nanowire single-photon detectors (SNSPDs).

GHS. The gas handling system (GHS) is the part of a cryostat that controls the dilution. It usually fits in a rack. In 2024, Bluefors introduced its new modular and upgradeable GHS 2, using new pumps and sensors, including a new multi-stage roots main circulation pump. Its new control software is accessible through a touch screen UI and allows intelligent automation with fully automated cooldown, or control of individual components [3056]. This GHS 2 was then integrated in the new compact LD system [3047]. It has the performance of the LD400 system with 16 μW of cooling power at 20 mK and 500 μW at 100 mK. The mixing chamber has a diameter of 294 mm. The entire system can be moved around.

Figure 351: The Bluefors Ultra-Compact LD with its cryostat. Source: Bluefors.

LD. Bluefors cryostats start with the entry-level LD that is used to test a couple physical qubits in academic and startup labs. Bluefors launched in 2025 the Ultra-Compact LD, a smaller version of the LD system with a 19" rack containing 10U for measurement electronics and the GHS2. It also embeds dampening solutions for

Figure 349: A Cryomech compressor, that is connected to a pulse tube. This is the devices that generates the repetitive "pchit-pchit" sound in the labs and companies which use it. Source: Cryomech.

Figure 350: A Bluefors/Cryomech PT420 pulse tube, that cools a cryostat down to 4 K. Its cooling power is of 2 W at 4.2 K and 55 W at the 45 K stage. Indeed, these pulse tubes have two stages that are visible in the pictures, being attached to two consecutive cold plates in the cryostat. The pulse tube is also used to cool down the helium 3 and 4 mixture circulating in a dilution that is attached to the pulse tube. Source: Bluefors.

low-vibration operations, with 8-14 dB lower noise than the LD system (Figure 351).

XLD. The XLD is a larger cryostat with a larger cylinder that can accommodate a larger number of qubits. It is the cryostat that IBM used for Osprey, the 433-qubit processor announced in 2022, and Condor, the 1,121-qubit processor announced in 2023, but never really used. In August 2024, Bluefors introduced the XLDHe High Power System, a new version of the XLD that is tailored for using 1K devices like silicon spin qubit chips or single photon detector applications (SNSPD). It provides 200 to 700 mW of cooling power at 1 to 1.2 K. It uses from two to three Cryomech PT425 pulse tubes. It also embeds six side-loading ports for fast exchange of experimental wiring (Figure 352).

KIDE. The KIDE announced in November 2021 is a high-power cryostat that has a hexagonal shape to make it easier to assemble them next to each other for distributed QPU setups and with 9 pulse tubes and three dilutions each (Figure 353). Kide means a crystal or a snowflake in Finnish. It has dedicated pulse tubes for operational cooling, customer payload cooling, and cooling the shields. Its production started in 2023 for IBM and Rigetti, IBM receiving its first unit in April 2023 at Yorktown Heights [3048]. The KIDE seems to have a width of about 1.5 m wide for the vacuum chamber with hexagonal cold plates. Its steel and aluminum doors are easy to open for loading equipment and samples, which is much easier than using huge cylindrical cans. Still, there are at least 5 doors to remove since the inside of the cryostat is a hexagonal Russian doll instead of being a cylindrical one. It can accommodate 1,000 qubits and 4,000 High-Density Wiring RF lines with the possibility of scaling up to 10,000 qubits, with a payload of up to 500 kg. The whole system weighs 5.7 tons.

Modular Cryogenic Platform. In March 2021, Bluefors announced a partnership with **Linde** (Germany) to create high-capacity cryogenic systems dedicated to scalable quantum computers. Linde is a gas producer competing with Air Liquide. It is related to the support of helium liquefiers. It explains their announcement in 2026 of their Modular Cryogenic Platform which can accommodate large configurations with series of dilutions, including a support of cooled interconnect microwave cabling between computing units, a bit like what IBM is planning with Starling and Bluejay [3057] (Figure 354). The system is a large vacuum chamber, with full access doors on all sides. Each module will support payloads up to 800 kg and up to 36 side-loading wiring ports.

Sample holder. Apart from the quantum computing market, Bluefors released in 2024 a new handler for MRI experiments [3058] and the Cryomech HeRL02-RM, a new helium reliquefier designed specifically for helium recovery from a single NMR instrument, which used liquid helium cooled superconducting magnets.

Wiring. Bluefors also offers compact wiring solutions. The latest is the High-Density Flex Wiring (FPC) launched in 2025 which works along the LD400sl system with its side-loading ports (Figure 355). The EPC supports up to 240 channels per side-loading port.

Cryoprober. Bluefors also developed with **Afore** (Finland, a subsidiary of AEM from Singapore since 2018) a Cryogenic Wafer Prober, a system used for the characterization of 300 mm wafers down to 1K (Figure 356). It was acquired by **CEA-Leti** in 2021 to test the quality

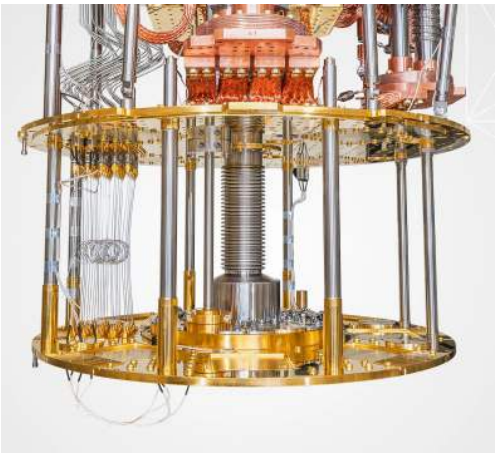

Figure 352: The XLDHe cryostat available space which can accommodate up to hundred physical superconducting qubits. Source: Bluefors, 2024.

Figure 353: BlueFors KIDE dilution refrigerator. Source: Bluefors, 2023.

Figure 354: 3D rendering of the Bluefors Modular Cryogenic Platform. Source: Bluefors, in 2026.

Figure 355: The interior of the LD400sl with its side loader and the associated EPC high-density flex wiring. Source: Bluefors, July 2025.

Figure 356: The Bluefors/Afore cryoprober used by Intel and CEA-Leti.

of their silicon qubits wafers. **Intel** acquired a similar tool as well, for their own silicon qubits development efforts in their D1D fab in Hillsboro, Oregon, USA.

Boreas Cryogenics

China, 2018

The company based in Shanghai was created by Haizheng Dang (CEO) [3059], who leads the cryogenics division of the State Key Laboratory of Infrared Physics at the Shanghai Institute of Technical Physics (SITP), Chinese Academy of Sciences.

Their product range includes a low-interference high-frequency pulse tube systems operating down to 2 K, regenerative and recuperative hybrid technologies covering 2 K to sub-Kelvin, and dry dilution refrigerators. They support high-power pulse tube cryocooler with one milestone of 1,220 W of cooling power at 77 K [3060]. One dilution reached 7 mK with 1200 μW of net cooling power at 100 mK, with a specific pulse tube providing over 2.8 W at 4.2 K. They published work on a three-stage Stirling-based pulse tube [3061].

CASQI

China, 2024

Zhong Qing Ji's research team in Beijing was working on the development of dilution refrigerators [3062]. It led to the creation of CASQI, *aka* Zhongke Measuring Instrument (Beijing) Technology Co, a spinout from the CAS Institute of Physics in Beijing. They offer the L400 with 10 μW of cooling power at 20 mK on a 395 mm cold plate and 400 μW at 100 mK. The L1000 has 20 μW of cooling power at 20 mK on a 500 mm cold plate and 1 mW of cooling power at 100 mK. They created a record 4-dilution system reaching 6.6 mK with a cooling power of 2,000 μW at 102.5 mK, fed by two pulse tubes and cryocoolers [3050]. They also develop 1K and 4K cryocoolers and pulse tubes.

CETC

China, 2019

CETC aka China Electronics Technology Group Corporation, 16th Research Institute, is among the military-industrial groups directly managed by the government. It is connected to the Hefei Low-Temperature Electronics Research Institute. The company has a long history in the creation of Stirling coolers, Gifford-MacMahon cryocoolers, superconducting electronics and cryogenic receivers. It started covering the quantum computing market in 2019. Their XS1000 unveiled at the November 2025 Hefei Quantum Conference has a dilution refrigerator which supports a base temperature below 10 mK and a cooling power of 1,100 μW at 100 mK.

CryoFab

USA, 1971

CryoFab provides liquid helium containers and related accessories.

Cryogenic Limited

UK, 1991

Cryogenic Limited provides a various set of cryogenic systems and superconducting magnets. It includes liquid helium systems and ultra-low temperature systems using their own magnet and an off-the-shelf cryostat from Leiden.

CryoPride

China, 2010

CryoPride *aka* CSSC Pride Cryogenic Technology, Pride Cryogenics and CSSC Pengli was created by Chen Jie, a graduate of Zhejiang University, who specialized in small-scale low-temperature cryocoolers. It is a subsidiary of CSSC (China State Shipbuilding Corporation), a state-owned defense industrial group. It develops cryocoolers and cryogenic engineering application devices, including 4K, 10K and 77K Gifford-McMahon cryocoolers, helium reliquefiers, and gas recovery, purification and liquefaction systems. Its cryocoolers target the MRI market, research laboratories and semiconductor manufacturing. It also manufactures cryogenic vacuum pumps. It launched a line of dilution refrigerators in 2023 which cover the China domestic market with the KDDR-1-400 which has a cooling power of 12 μW at 20 mK and about 400 μW at 100 mK.

FormFactor

USA, 1993

FormFactor is a provider of electronic test and measurement tools for the semiconductor industry with some products dedicated to quantum technologies who is consolidating the dry dilution refrigerators business in the USA.

They acquired in early 2022 the dry-refrigerator business line from Janis ULT. Their offering covers chipsets inspection and metrology, characterization, modeling, reliability, and design debug, to qualification and production test. In 2020, they acquired **High Precision Devices** (1993, USA), which develops cryogenic instruments adapted to superconducting quantum chipsets.

Thus, their HPD IQ3000, a cryogenic probe station for on-wafer and multi-chip measurements (*left* in Figure 358). It can embed IR-sensor test, radiometric test and configurable DC and RF cabling and custom probe cards. It supports 150 mm, 200 mm and 300 mm wafers at 4 K (while Bluefors' probe station also supports 300 mm wafers). The HPD IQ2000 is a chip-scale prober for individual die testing operating at 2K or at 4 K. The tested chipset can be cooled from 300 K to 4 K in less than an hour (Figure 358). It also supports automated wafer motion and a monitoring camera.

They sell dry dilution refrigerators supporting 10 mK and below temperatures that are used for test and measurement (JDry-250, JDry-500, its quantum-oriented JDry-500-QPro variant reaching 7 mK with 14 μW at 20 mK and 500 μW at 100 mK on a 50 cm mixing chamber plate, and JDry-600, this last one offering a 630 μW cooling power at 100 mK and 17 μW at 20 mK), all coming from Janis ULT.

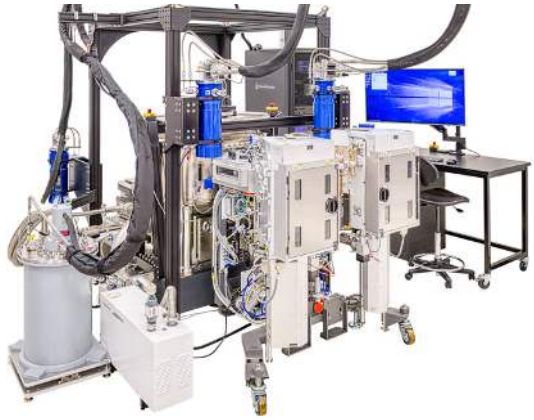

Figure 357: FormFactor HPD IQ3000 cryoprober. Source: FormFactor. 2023

Figure 358: FormFactor HPD IQ2000 chip-scale prober. Source: FormFactor. 2023

They also sell one or two-stage ADR (Adiabatic Demagnetization Refrigerators) using a salt crystal to strong magnetic fields, complementing dilution refrigerators. Among others, FormFactor partners with SEEQC and Keysight.

Hexin Instruments

China, 2022

In 2024, Hexin Instruments acquired Liangyi Technology, a company specializing in the creation of dilution refrigerators created in 2022.

ICE

UK, 2004

ICE, aka ICEoxford, was created in 2004 by Chris Busby and Paul Kelly to design and manufacture custom wet and dry Ultra Low Temperature (ULT) cryostats (but not below 300 mK) and High Magnetic Field equipment for research applications. In October 2025, they launched the ICE-Q platform, a modular system that uses a series of cube-shaped modules fitting into a standard 19-inch rack mount. It includes a cooling module, a payload for the quantum chip, and side-loading wiring modules.

Intelline

Canada, 2018

Intelline produces customized cryogenic refrigeration systems that are expected to be more affordable than those of its competitors. But they seem to target markets other than quantum computer cryogenics, at least at temperatures below 1K.

JanisULT

USA, 1961

JanisULT was initially Janis, a generalist cryostat manufacturer. In 2020, they sold their 'classical' laboratory cryostats business to Lake Shore.

They kept their ultra-low temperature cryostat business under the brand Janis ULT. They have an offering of wet and dry dilution refrigerators for various use cases, including quantum computing. Their high-end wet dilution refrigerator is the JDry-500-QPro with a 508 mm cold plate and >450 μW of cooling power at 100 mK achieved with a single pulse tube, coming from Sumitomo SHI.

Kiutra

Germany, 2017, $15.2M

Kiutra is the only vendor specialized in the development and production of ADR or Adiabatic Demagnetization Refrigeration systems.

Company. It is a startup from the TUM (Technical University of Munich) launched by Alexander Regnat. It was seed financed by APEX Ventures and German investors, but the amount is not known. Kiutra had a staff of 40 as of early 2023.

Technology. ADR was created by William Giauque (1895-1982, USA) in 1927. He was awarded the Nobel prize in physics in 1949. It was then of course not designed for quantum computing. This type of refrigeration can be added to a wet or dry dilution cryostat. The principle is using a paramagnetic salt which is magnetized with a strong enough field, of 6 Tesla or more. This will heat the salt. The heat is evacuated via a 4K liquid helium bath (Figure 359). The suppression of the magnetic field cools the salt by expansion. The process complexity lies in the heating-cooling cycle which can disturb the cooled equipment. It is treated by combining several devices that take turns to smooth the temperature curve of the system. The process has been tried and tested for a long time, but the cooling power available is very low (Figure 360).

Products. Kiutra used initially this technique to obtain more classical temperatures of a few hundred mK, one of its advantages being that it does not generate vibrations [3063]. These temperatures were interesting for cooling silicon qubits. Their cryostat range went down to 100 mK (in pulsed mode) or 300 mK (in continuous mode), which is insufficient to cool superconducting Josephson effect quantum computers but could possibly be suitable for electron spin silicon chips that can theoretically be satisfied with a temperature of 1K. Their system uses the magnetocaloric effect which was discovered in stages in 1881, 1917 and demonstrated in 1933 to reach a temperature of 250 mK.

In 2026, Kiutra, announced that its technology could reach the operating temperature of superconducting qubits, with the potential of getting rid of ^{3}He based dilutions [86, 3064]. ADR was used first in space applications where dilutions can't operate due to the absence of gravity [3065]. It supports 50 mK temperatures with pilots getting as low at 20 mK [3066]. Their plan is to use a multi-stage cADR [3067]. Such a setup was tested by Kiutra and Qutech to cool superconducting qubits in 2026, operating at 27 mK with a future version planned to support 20 mK with a cooling power of up to 20 μW [3068]. A practically shortcoming of cADR its space constraints in the cryostat. And the Kiutra cADR results are recent and have not been yet demonstrated at scale.

To smooth in time and space this heating/cooling cycle, they combine several cooling units with what they call cADR (continuous Adiabatic Demagnetization Refrigeration) [3064, 3069].

The apparatus proposed by Kiutra seems to be mainly designed to cool small samples and does not seem to be yet adapted to the usual architectures of quantum computers with their cooling stages stacked between 4K at the top and 15 mK at the bottom. On the other hand, some dry cryostats can reach temperatures situated between 5 and 10 mK.

They are dedicated to physics experiments unrelated to quantum computing such as the search for dark matter (for the detection of WIMP, Weakly Interacting Massive Particles) and the analysis of cosmic radiation using calorimeters operating between 5 mK and 7 mK. This is the case, for example, of the **CUORE** (Cryogenic Underground Observatory for Rare Events) bolometer installed in Italy. The cryostat comprises five pulse tubes and cools a 750 kg payload of tellurium dioxide to 10 mK. It searches for neutrinoless double-beta decay, whose observation would provide evidence that neutrinos are Majorana particles. This particle-physics question is distinct from the condensed-matter Majorana zero modes proposed for topological qubits. No signal has been reported so far.

Leiden Cryogenics

the Netherlands, 1992

Leiden Cryogenics was founded by Giorgio Frossati and Alex Kamper. The former had been working on dilution refrigeration since the 1970s. Among other things, he invented silver powder heat exchangers.

He started to work at the Centre de Recherche sur les Très Basses Températures in Grenoble, which became the research center on Condensed Matter and Low Temperatures (MCBT) of the Institut Néel of the CNRS. He then became a professor at the University of Leiden in the Netherlands. He designed there a dilution refrigerator reaching a record temperature of 1.75 mK with a cooling power of 25 μW at 10 mK [3052]. The heat exchanger technologies he developed were licensed to Oxford Instruments. At last, BlueFors was created by Georgio Frossati's post-docs! What a small world!

Leiden is behind what looks like the largest very low temperature cryostat ever built for a large load as shown in Figure 361. It was achieved between 2016 and 2018 for CUORE (Cryogenic Underground Observatory for Rare Events).

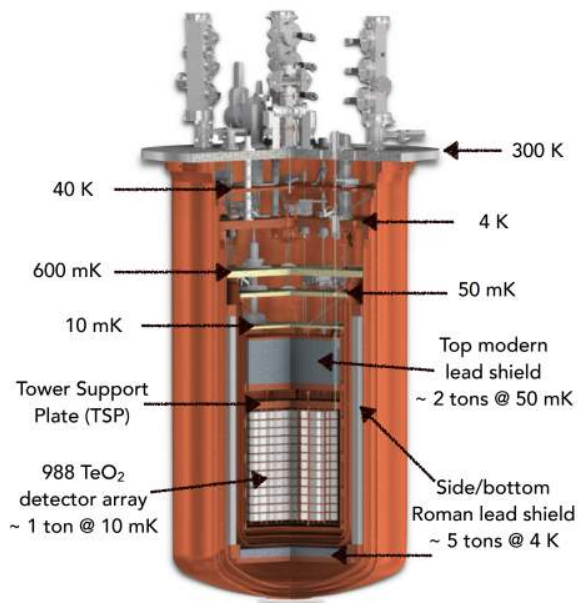

Figure 361: The CUORE mega-cryostat cooling a load of one ton.

It is a bolometric experiment for neutrinoless double-beta decay detection in TeO_2 (tellurium dioxide) that is installed at the underground facility of Laboratori Nazionali del Gran Sasso (LNGS) in the Alps. The CUORE cryostat is cooling a one ton mass of metal with a one cubic meter size to 7 mK. It is using a three stage cooling system with liquid Helium vapors for the first stage at 50K, five Cryomech PT415 pulse tubes and compressors for the 4K stage and only a single modified Leiden dilution unit for the stage below 10 mK. Interestingly, the cooling power of the lowest stage is only of 3 μW at 12 mK, lower than the maximum cooling power at 15 mK of most dilutions analyzed in this section. The difference is it took 26 days to cool

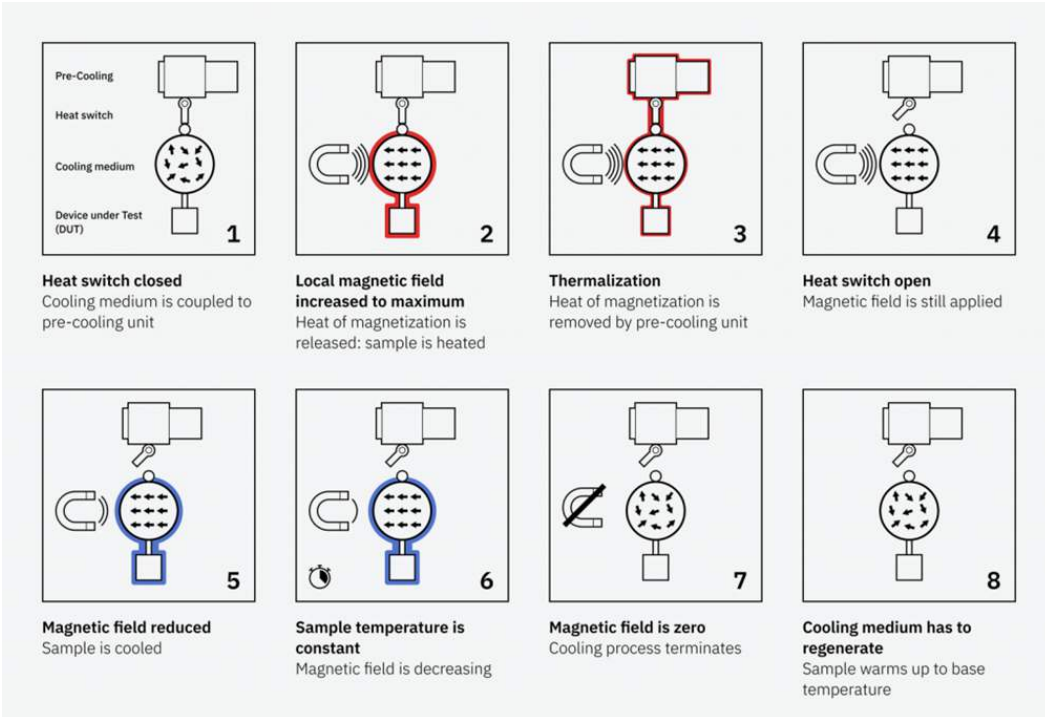

Figure 359: The Kiutra magnetic refrigeration process. Source: Kiutra.

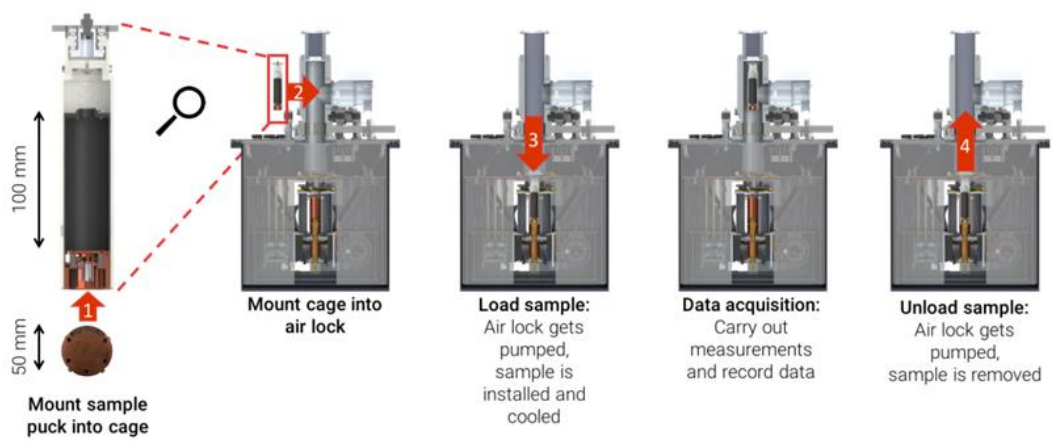

Figure 360: Kiutra cooling process. Source: Kiutra.

down the experiment, including only 4 days for the last stage of one ton after 22 days to reach 3.4 K [3049].

Linde

Germany, 1879

Linde is a global chemical company and the world's largest industrial gas supplier. Its engineering branch entered the quantum computing market in 2025 with announcing it would deliver a cryogenic cooling plant to PsiQuantum, to be built in Brisbane, Australia. It will operate at 4 K (−452°F, −269°C) to cool the cryogenic cabinets containing PsiQuantum's Omega chipsets Figure 362.

The plant is gigantic and has a scale similar to the cryogenic plant at CERN and ITER (these two being provided by Air Liquide). The total PsiQuantum QPU will need a power "plug" of 100 MW but the share of this that comes from cooling is not documented yet. It will need to provide 10 kW of cooling power at temperatures ranging from 2 K to 4 K.

Figure 362: Part of the Linde installation that will be built in Brisbane for PsiQuantum. Source: Linde.

Maybell Quantum

USA, 2022, $26M

Maybell Quantum is a company created in Colorado by Corban Tillemann-Dick (CEO, formerly at the BCG), Kyle Thompson (CTO, from the MIT Lincoln Labs and Janis ULT) and Brian Choo.

Company. Maybell Quantum's initial funding came from Colorado's Advanced Industry Accelerator (AIA) venture fund and the US DoD National Security Innovation Capital fund (NSIC) which belongs to the Defense Innovation Unit. The company already had some contracts from DARPA.

Technology. Maybell develops a dilution refrigerator, the Icebox, that is intended to support three times more qubits in 10% of the usual space, all at a temperature below 10 mK. Above all, they announce a capacity of 4,500 cables to drive qubits with microwaves up to 12 GHz (meaning: superconducting qubits and electron spin qubits) thanks to their Flexlines, ultra-high-density RF ribbon cables and Super-Flex NbTi ribbons cables for the lower stages of the cryostat Figure 364. Their Resito-Flex (CuNi-NbTi, BeCu-NbTi, CuNi-CuNi) and Atenu-Flex (SS-NbTi, SS-SS, SS-CuNi) ribbons are adapted to higher-temperature stages. It is optimized for 1,000 qubits QPUs.

Maybell Quantum also provides classical coaxial cabling and fiber optics connectivity. The whole cryostat fits into two 19" server racks formats with extra space available for 9U of electronics and computing. But it doesn't contain the compressor and the GHS (gas handling system) that controls the flow of helium in and out of the compressor and requires a space equivalent to their own system. The helium compressor can be cooled with air or water. On top of that, the Maybell Icebox experimental part is supposedly accessible with a simple door (Figure 363).

In 2023, Maybell Quantum launched its Big Fridge, a whole dilution refrigerator solution designed for scale. It has 130L of sample volume and 600L of total internal volume, and over 4,000 cm^2 of area on the mixing chamber plate, equivalent to a 71 cm diameter disk (Figure 365, *right*). In September 2023, Maybell Quantum set up a European headquarters and regional R&D center in Copenhagen, Denmark.

In 2025, Maybell Quantum announced it would procure ^{3}He from Intelune, a company that plans to harvest it on the Moon and that, in the meantime, sources it from terrestrial production. Lunar recovery remains prospective.

In 2026, it announced the Cold Cloud distributed architecture, which looks similar to Bluefors Modular Cryogenic Platform announced nearly simultaneously (Figure 366). Maybell targets a tenfold improvement in energy efficiency over conventional compressor and dilution systems, mainly through the use of a helium liquefier. Deployments should happen in 2027, probably at the DoE. A system supporting 25W cooling power at 4K and the associated dilution would cost $10M. This system could support up to one million superconducting qubits [3070].

Figure 366: Maybell Cold Cloud 3D rendering. Source: Maybell Quantum.

Montana Instruments

USA, 2009

Montana Instruments develops cryostats and vacuum pumps, used in trapped ions (including IonQ) and NV centers computers as well as photon-sources (Sparrow Quantum).

One of their added values is to reduce the vibrations coming from the pulse tube. They cover temperatures ranging from 3.2K to 4.9K.

MyCryoFirm

France, 2013

MyCryoFirm produces dry cryostats, running at 3K with a cold plate of 250 mm diameter with a 300 mW cooling power at 4.2K. They rather target the field of research in quantum optics, quantum physics and quantum sensing.

They propose various experiment decks/plates adapted to creating magnetic fields, spectroscopy applications and the like. In 2022, they did add a dilution option on

Figure 363: Maybell fridge in 2023. Source: Maybell Quantum.

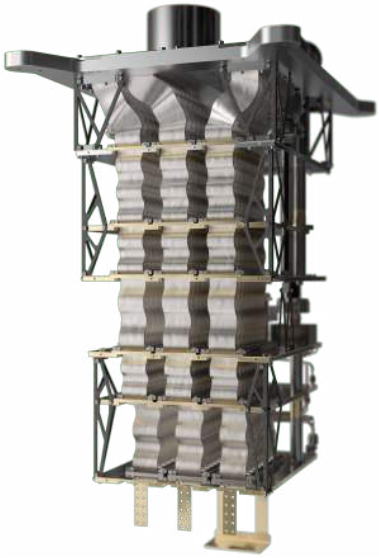

Figure 364: Maybell dense flexible cables setup. Source: Maybell Quantum.

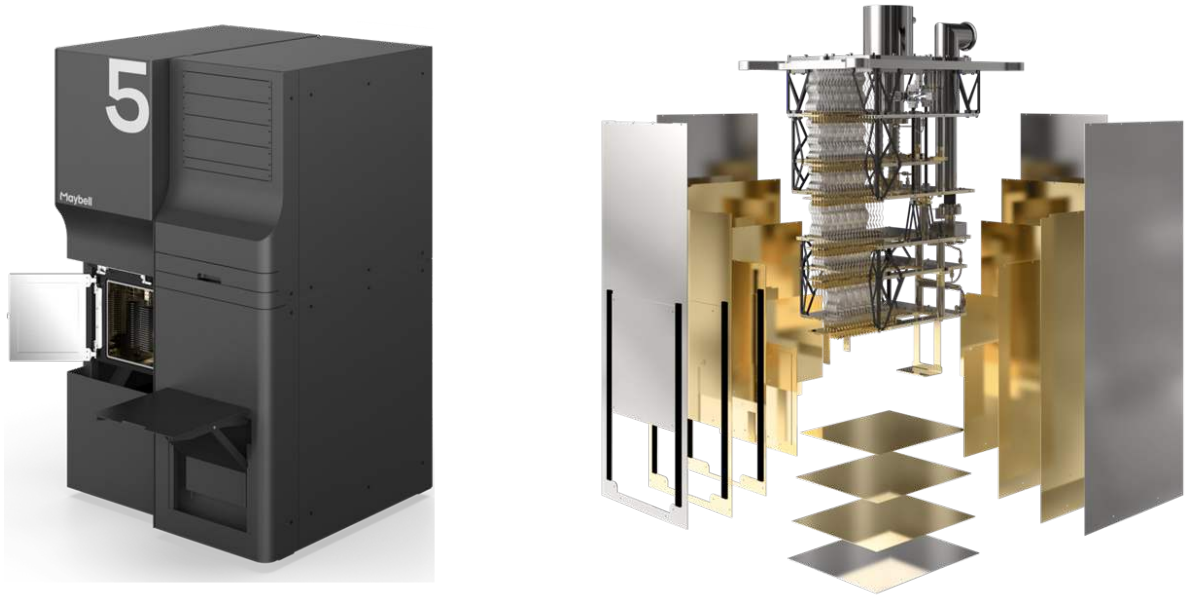

Figure 365: The Maybell Quantum cryostat unveiled at the APS March meeting 2022 in Chicago (left) and the Big Fridge announced in 2023 (right).

their Optidry250 cryostat and made it operate at 50 mK at Météo France. The company was acquired by Pasqal in 2022. Pasqal indeed needs 4K custom cryostats assemblies to cool its QPU ultra-vacuum pump and atom chamber.

Origin Quantum

China, 2017, $163.4M

Origin Quantum is producing since 2024 dilution refrigerators with the Origin SL400 and Origin SL1000, which can accommodate 336 and 840 coaxial cables. The SL1000 has a cooling power of 1 mW at 100 mK. Interestingly, the technology also seems to come from Anhui's Quantum Computing Engineering Research Centre.

In the China cooling realm, a research team led by Sun Peijie at the CAS Beijing National Laboratory for Condensed Matter Physics, in partnership with scientists from the Jülich Centre for Neutron Science outstation at the Institut Laue-Langevin in Grenoble, France, discovered a cobalt-based quantum magnetic super-solid material that could potentially be used to create ultra-low temperatures without the need for helium-3. This triangular lattice magnet $Na_2BaCo(PO_4)_2$ (NBCP) can behave as both a solid and a fluid [3071, 3072]. It is still far from being operational.

Separately, the Hefei Institutes of Physical Science, the Institute of Theoretical Physics (both CAS), and Shanghai Jiao Tong University discovered a metallic spin supersolid in $EuCo_2Al_9$ (ECA), a rare-earth alloy of europium, cobalt, and aluminum. Using adiabatic demagnetization refrigeration, the same technique as the one used by Kiutra in Germany, a compact solid-state module built from ECA reached a base temperature of 106 mK. This is a 2026 laboratory demonstration: no continuous heat lift, duty cycle, input power or payload is specified, so it is not yet comparable with a dilution refrigerator [3073].

Physike

China, 2007

Physike *aka* Beijing Feisco Technology Co, is a group based in Beijing and Shanghai with a broad offering in cryogenics.

Figure 367: Physike Qcryo two-stage with the first one supporting temperatures from 1.8 K to 2.3 K and a Ucryo sub-K cryostat supporting 950 mK.

It includes the IceCore dilution refrigerators, the Cryoclo He-3 refrigerators/inserts, sub-Kelvin refrigerators (Ucryo), 1.5K/4K refrigerators (Acryo), helium cycle cryogenic systems (Qcryo, in Figure 367), precision-fine optical microscopy cryostats (CryoAce), liquid helium cryostats (Scryo), dry variable-temperature superconducting magnet systems (CryoM), dry room-temperature bore superconducting magnets, ADR and SQUID sensors, liquid helium transfer lines and dewars, cryogenic temperature sensors (ZrON), temperature controllers (Cryocon), liquid nitrogen cryostats (Vcryo), and thermoelectric cryostats (Labcryo). The Icecore-400 and Icecore-500 support temperatures below 10 mK and have a cooling power above 12 μW at 20 mK and 500 μW at 100 mK with a single dilution unit. They support a cold plate of 400 mm and are fed by a 1.5 W pulse tube cooler.

Qinu

Germany, 2021

Qinu designs and sells mK and 4K cryostats. It was created by a former researcher from Institut Néel in Grenoble, which has its own cryostats design laboratory. Its range contains the L Eco, L Pro and XL Pro table-top cryostats that support temperatures at respectively 30 mK, 15 mK and 10 mK, with a fast cooldown time of 3 hours for the L Eco and 9 hours for the XL Pro (Figure 368).

Figure 368: Qinu L Eco cryostat interior (left) and seen onsite at Quobly (right).

QuantumCTek

China, 2009

QuantumCTek started to manufacture a dilution refrigerator in 2023, the ez-Q with a cooling power of 450 μW at 100 mK [3051]. It was achieved by a team led by Wang Zhehui, the deputy director of the Anhui Quantum Computing Engineering Research Center which partners with the company. It operates at 10mK and powers the Zuchongzhi superconducting qubits QPU from Hefei's research lab. Beforehand, China was relying on Bluefors, but Western country exports restrictions pushed China to become independent.

Quantum Design

USA, 1982

In 2025, Quantum Design acquired the NanoScience division from Oxford Instruments.

Oxford Instruments is a British company specializing in scientific instrumentation including cryogenic systems capable of reaching 5 mK [3074]. They provide CCD cameras to detect the state of trapped ion qubits, electron microscopes, vacuum deposition systems, X-ray sources and cameras, and nuclear magnetic resonance spectrographs. The company had acquired VeriCold Technologies (Germany) in 2007 to gain control of pulsed tubes used in the first stage refrigeration for dry dilution

cryostats. Their last product is the Proteox, a high-end and flexible dry dilution system with removable cabling.

In March 2021, they launched the ProteoxLX. It expands the qubits hosting capacity with a larger sample space and coaxial wiring capacity, low vibration and integration of cryo-electronics components. It offers a cooling power of 25 μW at 20 mK and 850 μW at 100 mK with twin pulse tubes providing up to 4 W cooling power at 4 K. They also designed a Q-LAN, a cryogenic link that could be used to connect two dilution fridges. The payload can reach 20 kg at 20 mK and 125 kg at 4K.

ULVAC Cryogenics

Japan

ULVAC Cryogenics provides various cryogenics solutions including 4K pulse tubes and also 4K cryopumps that can be used in cold atoms and trapped ions QPU settings.

There are many other cryostats and cryogenic devices vendors, but they are less specialized in serving the needs of quantum technologies providers [3075].

Zero Point Cryogenics

Canada, 2017, $2M

Zero Point Cryogenics is a company created by John P. Davis (CTO) from the University of Alberta. It provides compact dilution fridge designs including an inverted dilution (Model I, Figure 369) and a classical dilution (Model L).

Figure 369: Zero Point Cryogenics Model I inverted dilution. Source: Zero Point Cryogenics and Qnity.

ZL Cryogenic

China, 2023, $30M

ZL Cryogenics *aka* ZL Cryo and Zhileng was created by Wang Shaoliang, a cryogenic engineer at Anhui University, and Shan Lei, a professor at Anhui University's institutes of physical science and information technology. It was built with the help of the Hefei Technology and Innovation Group. The company started by creating dilution refrigerators, on the basis of the AHU-DR400 (Anhui University DR400), a prototype developed at Anhui University. It has two commercial models, the ZL-DR400 launched in 2024 that supports a temperature of 7.45 mK and a cooling power of 650 μW at 100 mK and 18 μW at 20 mK and a 300 mm cold plate. The ZL-DR1000 is a higher-power variant with unspecified cooling power.

2.1.4 Other cryogenics

For the other types of qubits, the cooling requirements are different: trapped ion qubits are not theoretically refrigerated, but Honeywell's prototype ion-trap chips announced in early March 2020 are cooled to 12.6 K, a temperature that can be obtained with ^{4}He based cryostats.

In photon-based quantum processors, the optical components traversed by the photons (mirrors, prisms, interferometers, whether miniaturized in nanophotonics or not) are not refrigerated, but the photon sources and photon detectors are, at temperatures between 1 K and 10 K. The associated cryogenics are much lighter and consume less energy compared to dilution cryostats.

Other techniques allow very localized cooling. This is the case of the **Doppler effect** which works on cold atoms suspended in a vacuum. Another solution developed by researchers from the VTT Technical Research Centre in Finland would cool silicon components with a phonon-based electronic cooling technique. It seems that this cooling capacity is very low, very localized, and still requires pre-cooling the system to at least 244 mK. It is therefore still necessary to operate a ^{3}He–^{4}He dilution refrigerator [3076].

Thales Cryogenics

France-the Netherlands

Thales Cryogenics, a subsidiary of Thales Group, designs and manufactures compact cryocoolers for military, space and commercial applications. Its includes rotary and linear Stirling coolers, linear pulse-tube cryocoolers, mini-coolers, high-pressure gas compressors and miniature rotary/linear DC/AC converters. Production is split between two complementary sites: Toulouse (France, 100 employees, 3,000 units/year, mostly rotary Stirling coolers) and Eindhoven (Netherlands, 80 employees, 1,000 units/year, linear Stirling, pulse-tube and space coolers).

Thales' NV-center-based quantum sensors use miniaturized cooling occupying only about 0.5 L (Figure 370). These are closed-cycle Stirling machines reaching the 77 K range rather than liquid-nitrogen dewars.

Figure 370: A small Stirling cooler for embedded systems. Source: [3077].

The RM2 cools a payload to 77 K for a mass of 275 g and a thermal budget of 400 mW at this temperature, and is notably used for cooling infrared cameras in embedded systems. Their rotary Stirling units deliver 0.4 to 0.9 W of cooling with up to 80,000 h of reliability, while linear Stirling and linear pulse-tube coolers reach 0.6 to 9.0 W and 1.4 to 5.7 W respectively, all operating in the 60 K to 150 K range.

For quantum applications, Thales Cryogenics is extending this above-50 K legacy on three temperature ranges: high (40 K to 80 K), medium (20 K to 40 K) and low (2 K to 4 K), covering both cooling and cryopackaging [3078]. A 2-stage pulse tube derived from its space coolers and developed with CEA targets 20 K to 80 K, with design goals of more than 3 W at 80 K, more than 200 mW at 20 K, and less than 200 W of input power. A new compact rack-mountable cooler, co-developed with DEMCON (the Netherlands), is designed to reach a 2.5 K base temperature with 15 mW of cooling for 250 W of input power, these being design targets rather than measured performance (19-inch 4U form factor MTBF > 60,000 h), adding a Joule-Thomson stage below a 2-stage pulse-tube pre-cooler. Part of these developments were funded by the CRYONEXT project from the French quantum plan.

This type of small cryostat can also be found at SunPower (USA), capable of cooling down to 40 K with a larger mass of 1.2 kg. Ricor (1967, Israel) is another manufacturer of such mini-cryostats, with a higher target temperature around 70 K, which remains hot compared to the 15 mK needed by many superconducting qubits. These cryostats are used for various breeds of quantum sensors.

2.1.5 Vacuum

Besides photon qubits, most other qubit types require some form of vacuum to isolate the qubits from their environment. We usually make a distinction between different levels of vacuum. The most stringent ones are used with trapped ions and cold atoms which require ultra-high vacuum (UHV) conditions whereas solid-state qubits like superconducting and electron spins are less demanding. UHV starts at 10^{-9} mbar.

One problem to avoid when creating vacuum is outgassing. It manifests with particles being ejected from the internal enclosure surfaces and materials, including residual water coming from the air. The phenomenon is avoided by carefully selecting the materials.

Cold atom qubits require a pressure of 10^{-10} mbar while trapped ions go down to 10^{-12} mbar. In both cases, low pressures and outgassing are obtained with heating the system enclosure above 200°C for several hours while the vacuum pumps are operating. This "bake-out" process removes water and other trace gases sitting on the chamber surface. Heating is done with heater stripes placed around the chamber. The chamber exterior can also be cooled with liquid nitrogen to contain any further outgassing.

One option is to use an ion pump cooled at 4 K, which explains why Pasqal acquired MyCryoFirm in 2024. It can also remove the entry of any thermal photons in the chamber although this can be avoided with simpler means. In 2025, IonQ announced having created an ion trap vacuum miniaturized prototype that can sustain extreme high vacuum (XHV) levels without cryogenics.

There are many vacuum and ultra-high-vacuum systems vendors. The most commonly seen in research labs come from **Pfeiffer** (Germany) as well as from SAES Getters (Italy). Some pumps must be cooled at low temperature, like the 4K pump used by Pasqal to cool their atoms.

Finally, measuring pressure in vacuum is also a challenge. Classical mechanical pressure measurement is of no use in the UHV to XUV (extreme ultra-vacuum) ranges covering 10^{-6} to 10^{-10} Pa. The NIST in the USA is proposing a solution applicable to cold atoms to cover these ranges of pressures [3079]. A dedicated part on quantum pressure sensors is located in the quantum sensing part of this book.

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This **Cryogenics and vacuum** subsection contains 71 bibliographical references and notes containing at least 707 pages.

2.2 Qubit-control electronics

Most of the time, driving qubits and reading out their state requires applying electromagnetic control and measurement signals (Figure 371). For superconducting qubits and electron-spin qubits, these signals are often in the microwave or radio-frequency domain. Transmon transition and readout frequencies are commonly in the few-gigahertz range, often around 4-8 GHz, while electron-spin-resonance frequencies are set by the magnetic field and g-factor and can range from a few to several tens of gigahertz. These coherent control pulses contain many microwave photons, rather than being single-photon pulses. They are usually carried by coaxial or on-chip transmission lines and are shaped in amplitude and phase, for example with Gaussian or DRAG-like envelopes. They are then filtered and attenuated in cryogenic environment to reach the qubit on a chip at the right energy level. Direct-current and baseband pulses are also widely used for flux biasing, tunable couplers and electrostatic gates [3080, 3081].

We will look here into two sorts of microwave generation technologies: those coming from room temperature electronics and those generated within the cryostat at cryogenic temperature, including cryo-CMOS, SFQ superconducting electronics and other discrete electronic components working at these low temperatures like the TWPAs used to amplify qubit microwave readout signals.

Direct current signals are also used to drive qubits, like with Z gates with some superconducting qubits and to drive some amplifiers [38, 3080]. To be complete, we'll then also look at cabling and filtering components and their vendors.

With photons, cold atoms and trapped-ion qubits, control techniques involve photons and lasers operating in the infrared and near visible spectrum which we don't cover here. There are probably missing elements in Figure 371 related to photonic and atom based qubits.

We'll try here to answer many questions: how are all these electronics affecting the quality of qubits? How is it scaling as you need to significantly increase the number of physical qubits to accommodate the requirements of fault-tolerant quantum computing? How do you optimize the existing cumbersome wiring? What are the solutions to run all or part of these electronic systems inside the cryostat? What is the power consumption of these various solutions [3082]? How can room temperature electronics and cryogenic electronics scale?

Wiring. How many wires are needed to control solid-state qubits? The number is architecture-dependent. A superconducting-qubit system may use dedicated or shared microwave drive lines, flux-bias lines for tunable qubits or couplers, and frequency-multiplexed readout lines. Spin-qubit systems add electrostatic gate electrodes and may share RF or microwave control. Current experimental setups can require several electrical connections per physical qubit before multiplexing and shared resources are accounted for. This becomes a major packaging and thermal-load problem as the qubit count increases.

Multiplexing. Work is being done to multiplex qubit drive and readout signals with several methods. Frequency-domain multiplexing is already standard for superconducting-qubit readout, with several resonators sharing one line. Supporting 4 to 16 qubits per readout chain is common, while the practical limit depends on resonator spacing, amplifier bandwidth and dynamic range, crosstalk and the required readout time. Frequency multiplexing can also be used for qubit control [3083]. Another option is microwave-to-optical conversion followed by optical multiplexing. Nanophotonic circuits close to the qubit chip could perform microwave-to-optical and optical-to-microwave conversion [3084–3086]. Proposed cryogenic optical links include VCSELs that have been demonstrated at a few kelvin [3087–3089]. Time-domain multiplexing reduces the number of physical lines but trades wiring for temporal sharing of the control resource. It can reduce the degree of simultaneous control when multiple qubits share the same switched path, which may lengthen circuits or QEC cycles depending on the architecture [3090]. A qubit-drive RF switching system studied in 2025 used commercial MEMS SP4T switches with a 1-to-4 ratio between the 4 K and millikelvin stages [3091].

To ensure scalability, multiplexing and demultiplexing components must be positioned where their wiring reduction outweighs their thermal dissipation cost, noise and complexity. For switched control lines this can favor demultiplexing close to the qubit chip, while frequency-multiplexed readout signals can remain multiplexed through much of the cryogenic amplification chain. In all cases, active circuits at the coldest stages must fit within a very small cooling-power budget. Optical readout links based on piezo-optomechanical transducers are also being investigated [3092].

Synchronization. As QPU scale in number of physical qubits, multiple control electronics components are used to drive the qubits and their readout. They must be synchronized using a common clock [3093].

Cryo-electronics options. Many options exist that we'll cover in this part. Cryo-electronics can operate at the 4 K stage, as with Horse Ridge II, down to lower stages in the 15-100 mK range as shown in Figure 388. What are their limitations? Also, what are the pros and cons of cryo-CMOS vs SFQ electronics? These solutions must be compared using sampling rate, DAC and ADC resolution, waveform-memory depth, frequency range, clock quality, noise, power dissipation and scalability. For Horse Ridge II, 16,384 points refers to the AWG waveform-memory depth, while the chip amplitude resolution is 11 bits and the sampling rate 2.5 GS/s. The electronic components must also be sufficiently isolated

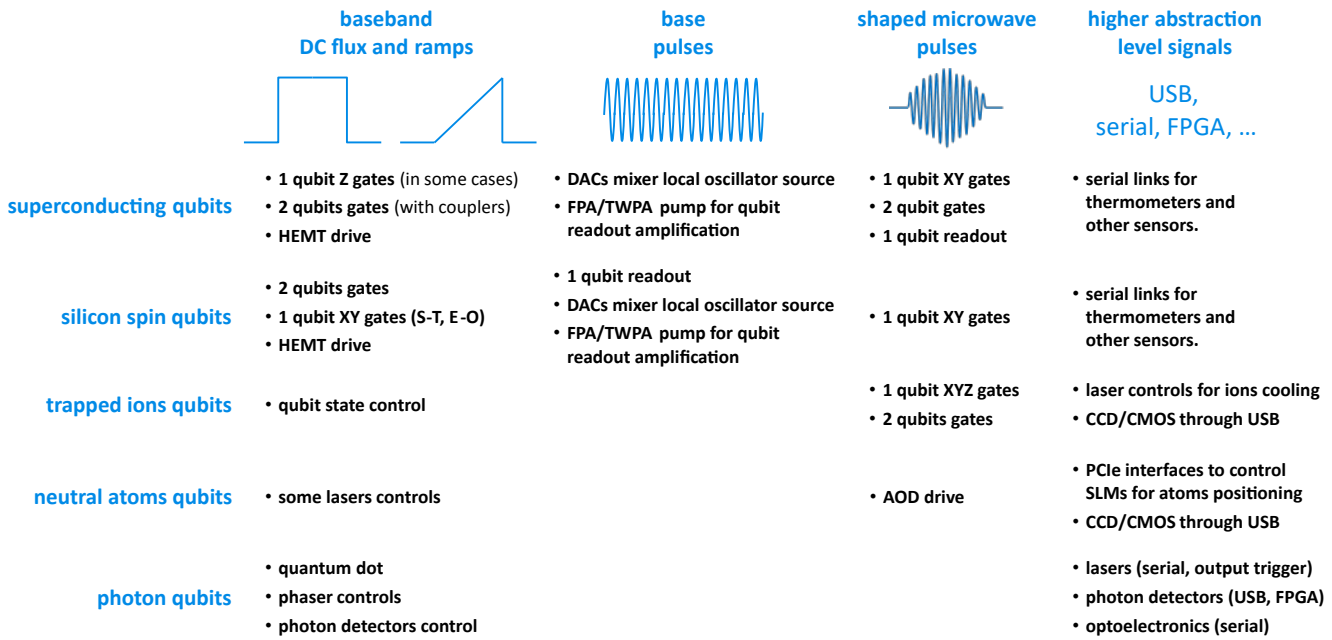


Figure 371: Compilation of the various electronic and photonic signals used to drive various types of qubits. This diagram will later be completed with more signals used to drive atoms and photon qubits. Olivier Ezratty, 2021-2023.

from the qubit chips to limit electromagnetic and thermal back-action.

Optimization. Cryo-electronics are an attractive solution in many respects: it potentially reduces the wiring burden as seen above, it creates miniaturized electronics that can help constrain the total size and weight of a quantum computer, it has the potential to minimize the control/readout/processing cycle latency and its energy consumption can be much smaller than room temperature electronics.

If the cryo-electronics components are not at the same stage as the qubits, you'll still need some (expensive superconducting) wiring. And it has a significant indirect energetic cost. These cryo-electronics components generate heat that must be extracted from the cryostat.

As one moves to the colder stages of a dilution refrigerator, the available cooling power falls sharply. At the mixing chamber, the low-temperature dilution process is approximately described by $\dot{Q} \simeq 84\,\dot{n}_3 T^2$ when the incoming ^{3}He is well precooled, so the ideal heat lift scales approximately as T^2, not T^4 [3094]. Commercial systems span a broad range, from a few or a few tens of μW near 10-20 mK to roughly watt-level cooling near 4 K. The values depend strongly on the dilution and its helium circulation rate. This explains why dissipative cryo-electronics are often placed at intermediate stages, typically around 2-4 K, rather than at the mixing chamber level where the available cooling power is very small. The optimum also depends on the qubit operating temperature and any potential electronic back-action on the qubit.

For superconducting qubits, the thermal constraint is generally stronger than for silicon spin qubits that can in some architectures operate at several hundred millikelvin or above. A 2023 full-stack resource model found that room-temperature control electronics can minimize the total energetic cost for superconducting-qubit systems under the assumptions explored in that study [3095].

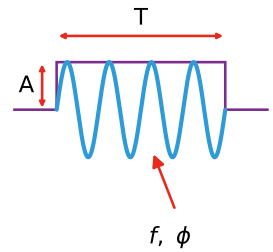
Control electronics and qubit fidelities. The relation between qubit fidelity and control-electronics precision has been studied quantitatively. Van Dijk et al. analyzed single-qubit gates, two-qubit gates and readout under static, dynamic, systematic and random control errors, and derived controller specifications corresponding to target fidelities such as 99.9% [3096]. Their numerical specifications were instantiated for single-electron spin qubits, although the methodology is more general. For solid-state qubits, both DC or baseband signals and shaped RF or microwave pulses may be required. Gate fidelity depends on pulse duration, amplitude, frequency and phase errors as well as on noise and leakage.

Control electronics can affect qubits through several mechanisms, including master-clock and local-oscillator phase noise and jitter, DAC quantization and nonlinear distortion, spurious tones and harmonics, mixer leakage, amplitude noise, and noise from DC-bias voltage or current sources, as illustrated in Figure 375 for superconducting qubits.

Various improvements are thus sought in qubit control electronics:

LO phase noise. Local oscillators and master-clock references used in the microwave upconversion and timing chain must have sufficiently low phase noise [3097, 3098] (Figure 374). Clock and oscillator phase noise becomes more important as other decoherence and control errors are reduced, and can become relevant for microsecond-scale operations such as trapped-ion gates.

	Nominal value	Errors		Infidelity
		Inaccuracy	Noise	
Frequency	10 GHz	11 kHz		125×10^{-6}
			11 kHz_{rms}	125×10^{-6}
Phase	0°	0.64°		125×10^{-6}
Amplitude	2 mV	14 µV		125×10^{-6}
			14 μV_{rms}	125×10^{-6}
Duration	500 ns	3.6 ns		125×10^{-6}
			3.6 ns_{rms}	125×10^{-6}
Wideband noise on oscillator			7 $nV/\sqrt{Hz}$	125×10^{-6}
Total				10^{-3}



Assumptions:

- π rotation at 1-MHz Rabi frequency
- Target fidelity: 99.9%

Figure 372: Specifications of a qubit control microwave pulse showing what signals defect affect qubit gate operations fidelities. Image reconstructed from [3096] in September 2026.

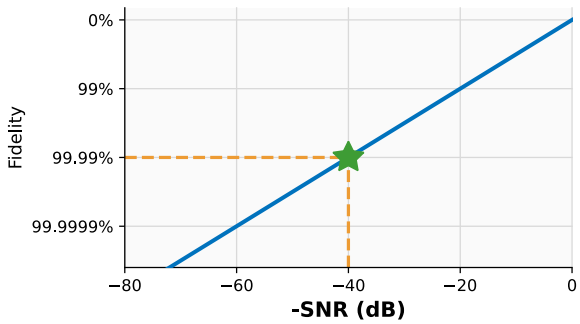


Figure 373: Specifications of a qubit control microwave pulse infidelity sources. Data source: [3096]. Updated in September 2026.

Table 2. Time until a qubit physical error rate p is reached solely due to phase fluctuations in the LO

Time to Reach LO-Induced Error Rate p					
p	10^{-3}	10^{-4}	10^{-5}	10^{-6}	10^{-7}
Lab-Grade LO	4.0 µs	900 ns	200 ns	30 ns	< 10 ns
Precision LO	> 100 ms	> 100 ms	> 100 ms	80 ms	600 µs

These times may be viewed as an upper bound on the allowable QEC cycle period. Achievable cycle periods will be reduced because of other error sources. Error rates are derived from free-evolution calculations presented in Figure 2b. Driven operation error rates (see Figure 2c) yield similar results.

Figure 374: Influence of local oscillator phase noise on single qubit gate error rate. Source: [3097].

Precision low-phase-noise sources can therefore be required instead of ordinary laboratory-grade oscillators.

The effect of oscillator phase noise depends strongly on the operation duration and control sequence. Ball et al. found that representative precision oscillators can reduce clock-induced residual error by roughly four orders of magnitude relative to representative laboratory-grade sources [3097]. For fast superconducting-qubit gates, the contribution can be much smaller than for microsecond-scale operations, but it becomes increasingly relevant as other error sources are suppressed.

Low-latency control/readout cycles. There is a need to minimize measurement, decoding and feedback latency because long delays can slow error correction operations and increase qubit exposure to decoherence. The relevant constraints depend on the QEC cycle time, decoder throughput, data backlog avoidance and when a decoded result is needed for conditional control. In a 2026 superconducting-qubit experiment, a scalable FPGA decoder achieved a sub-μs mean decoding time per round, while the measured end-to-end response was 9.6 μs for nine rounds, counted from the last measurement trigger to the availability of the decoded result at the controller output, for that decoder firmware and channel count [3099]. Latency figures are only comparable when the trigger point, processing path, output point, firmware and channel count are stated. Some techniques also optimize readout-pulse duration [3100]. The control system must be synchronized across qubits, which can be achieved with distributed clock and trigger architectures [3101]. Integrating waveform generation, digitization and feedback processing in the same FPGA or tightly coupled hardware can further reduce latency [3102].

From FPGA to ASIC. At this point, the most advanced qubit control systems are FPGA based. Their advantage is sound economics for small scale use cases but at an energetic cost. Using CMOS ASICs could bring some energetic advantage on top of further reducing control cycle latency, but it has a significant cost few qubit developers can afford at least in research labs. Also, the ASIC design and manufacturing cycle is much longer than with an off-the-shelf FPGA board.

Thus, the move from FPGA to ASIC is not only a technology choice but also an economic one. At some point, it will be conditioned by the volume of the quantum-computing market. FPGAs are also subject to classical soft errors and configuration upsets. Depending on the reliability target and radiation environment, mitigation can include ECC-protected memories, configuration scrubbing and redundant logic rather than a single generic "error-correction" mechanism [3103].

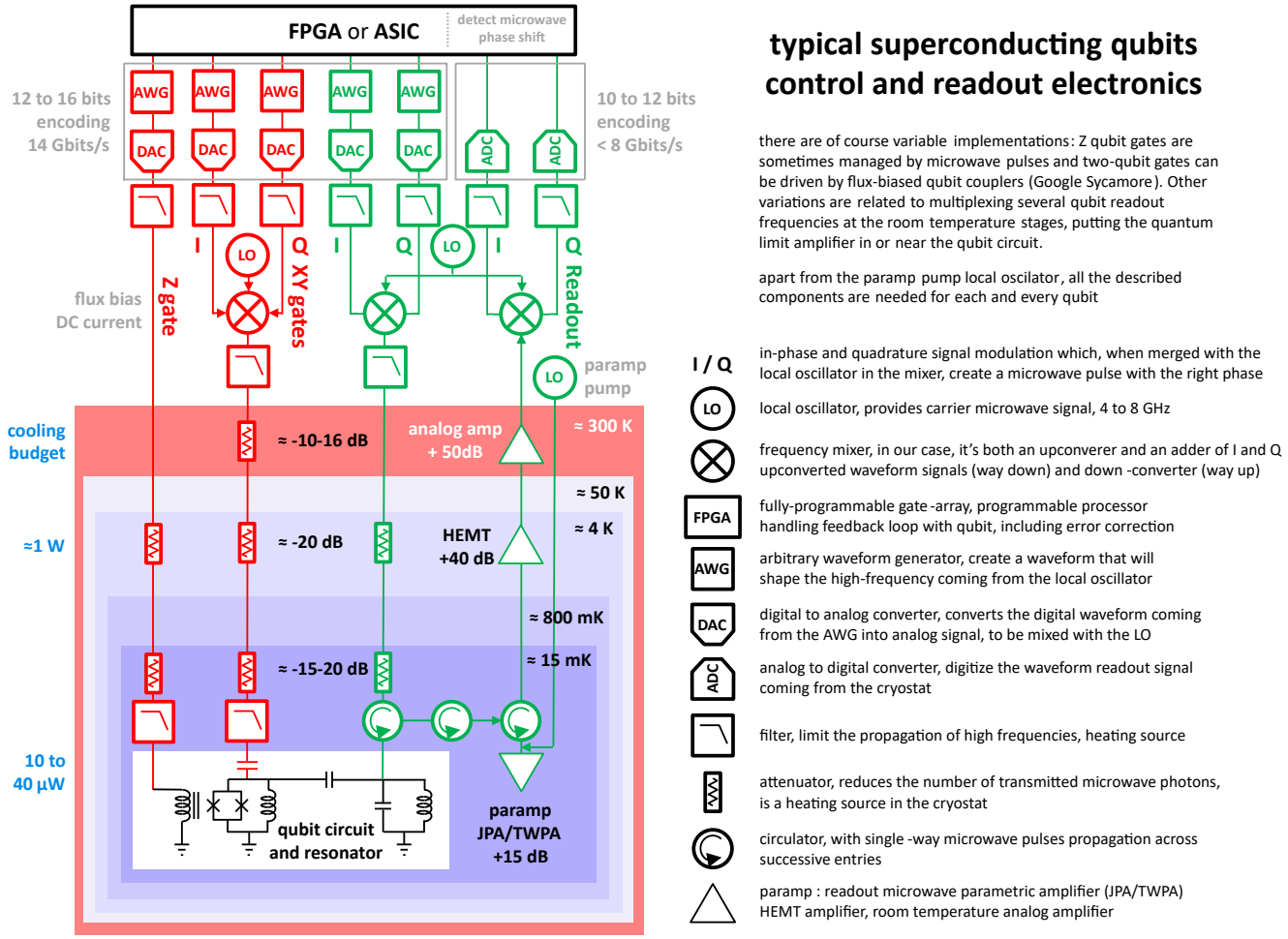


Figure 375: Description of the various electronic tools which control superconducting qubits. ⓒ Olivier Ezratty, 2022.

Memristors DC control. A Canadian French team proposed to control spin qubits quantum-dot gate biases with DC sources with a cryogenic solution using Al_2O_3-TiO_2-based tunable memristors with a ±1 V range and 100 μV resolution. Memristors are non-volatile systems with tunable resistance. It fits the need to tune these DC pulses due to qubit variability. It was demonstrated at 4.2 K [3104]. It doesn't support the other needed type of electronic controls, microwave pulses, that are needed to drive single qubit gates. This solution simplifies the DC wiring between room temperature control electronics and the 4 K stage in the cryostat, but it still requires DC lines between this stage and the qubits chip at below 1 K. These memristors are dissipating 1.77 mW. As a result, a current generation cryostat with 1.5 W cooling power at 4.2 K could accommodate about 800 such memristors. We are still far from the large-scale quantum (LSQ) realm, meaning here machines with a million or more physical qubits.

Pulse control optimization. At the software level, pulse control can benefit from some optimization techniques, requiring a verticalized approach crossing the usual layers between high-level gate-based code and pulse control. Such cross-layers optimizations are proposed by IBM and Q-CTRL [3105]. It is particularly useful in NISQ regimes since it makes use of many arbitrary single qubit rotation gates in variational algorithms. At the pulse waveform level, optimizations can also be made using some data compression which is important given that with many superconducting qubits, every qubit and couplers are driven by a unique waveform for each supported physical gate, which is tuned in calibration cycles to maximize gate fidelities [3106].

Topological qubit controls. Proposed Majorana-based architectures use electrostatic gate controls for tuning tunnel barriers and device configurations. Microsoft's 2025 interferometric fermion-parity experiment used RF dispersive readout of a gate-defined InAs-Al device [3107]. Future topological-qubit control stacks may combine relatively low-bandwidth gate-voltage control with RF or microwave resonator readout and other pulse sequences. Earlier proposals also use shaped time-dependent controls [3108, 3109].

Consolidated projects. Several qubit control and electronics research and development projects were launched in Europe. In Germany alone, you have three related projects:

QuMIC (Qubits Control by Microwave Integrated Circuits, €6.3M, 2021-2024) which involves four academic and two industry partners (Infineon, Supracon AG) and

deals with miniaturization of RF electronics to control superconducting and trapped-ion qubits.

qBriqs (€2M, 2021-2024) which also involves four academic and two industry partners (Rosenberger and Stahl Electronics) and deals with compact cryogenic connectors, qubit-readout TWPA and HEMT amplifiers, filters and attenuators, DACs and ADCs and DC flux current generators.

HIQuP (2021-2024, €2.2M) with, again, four academic and two industry partners (Supracon AG and IQM Germany) which works on superconducting and cryogenic qubit control electronic circuits.

In France, the **QRYOlink** project combines CEA-Leti and Institut Néel from Grenoble, Radiall, ATEM, Air Liquide, C12 and Alice & Bob to develop a scalable architecture for cryogenics and cabling aimed at supporting solid-state qubits. Other related projects also cover scalable control electronics targeting large scale quantum computing architectures.

2.2.1 Room temperature electronics

Room-temperature electronics remains the dominant control architecture in research laboratories and in many commercial systems. The following functional blocks are commonly present in the control and readout chain, although they may be shared across qubits through multiplexing and integrated differently in direct-RF architectures:

- **AWGs** (arbitrary waveform generators) which synthesize baseband, intermediate-frequency or direct-RF pulse waveforms. Sampling rates range from roughly 1 GS/s to several GS/s in many controllers, while direct-RF architectures can use much higher rates. These waveforms are used for single-qubit gates, two-qubit gates and qubit readout pulses depending on the architecture. Alternative pulse-width-modulation techniques have also been proposed [3110].

- **DACs** (digital-to-analog converters) which convert digital waveform samples into analog signals. Converter resolution is architecture-dependent and is commonly in the roughly 10–16-bit range for quantum-control hardware, with an effective number of bits lower than the nominal resolution at high frequency.

- **Mixers** combine in-phase and quadrature baseband or intermediate-frequency waveforms with a **LO** (local oscillator) to perform frequency upconversion into the qubit's microwave band. Heterodyne refers to a measurement or conversion scheme with a nonzero intermediate frequency, while homodyne detection uses a phase-coherent reference at the same carrier frequency.

- **Direct current** sources, to drive certain types of qubit gates *aka* bias drives. They must be stabilized [3111].

The distinction between homodyne, heterodyne and photon-counting detection is useful in both microwave and optical quantum systems (Figure 376). Homodyne detection measures one field quadrature selected by the phase of a coherent local oscillator. Standard heterodyne detection reconstructs both orthogonal quadratures by using an offset local oscillator or equivalent digital processing, at the cost of 3 dB quantum-noise penalty for conventional phase-insensitive heterodyne detection [3112]. Photon counting instead measures discrete excitation events or photon number and does not directly return a field quadrature.

On the way out of the cryostat, we have:

- A last-stage **analog amplifier**, following the cryogenic amplification stages (TWPA and HEMT).

- **ADCs** (analog-to-digital converters) digitize the down-converted or direct-RF readout signal. Sampling rate and nominal resolution vary widely by architecture, from about 1 GS/s with conventional IF acquisition to several or tens of GS/s in direct-RF systems, with typical nominal resolutions in roughly the 8-14-bit range.

- **SoC** (systems on chip)**, FPGA** or **ASIC** circuits used to interpret the output of the ADCs to get the qubit state, and which may manage a closed-loop control of the whole cycle to implement error correction (QEC). It can even implement machine learning tasks to improve qubit readout efficiency [3113].

All these components are integrated into one or several boxes, often with interchangeable modules. The FPGA fabric itself is normally configured with HDL, HLS or vendor-specific firmware toolchains. Python is commonly used at the host-software or experiment-control layer through APIs and libraries rather than as the native implementation language of the FPGA fabric.

This field is well covered by electronics industry vendors addressing research and commercial quantum computing markets. Beforehand, many quantum computing research laboratories were relying on generic micro-wave generator and readout systems coming from vendors like **Rohde & Schwarz**, **Tektronix** and **Keysight**. Over time, some of these vendors have developed specialized offerings for quantum computing, particularly through some acquisitions (for Rohde & Schwarz and Keysight). Specialized quantum computing electronics emerged like **Zurich Instruments**, **Qblox** and **Quantum Machines**. Large shops like **Google** also developed their own electronics.

Some hardware and software academic open-source control systems have also been proposed like the **QICK**

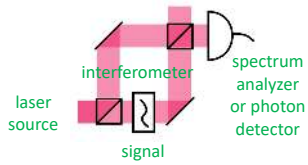
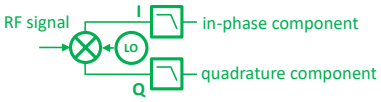
	homodyne measurement	heterodyne measurement	photon counting
definition	extracts information encoded as modulation of the phase and/or frequency of an oscillating signal with comparing that signal with a standard oscillation carrying no information.	extracts information along two orthogonal components in phase space like, for RF signals, the in-phase and quadrature signals coming out of an I/Q mixer, use a reference oscillator source (LO).	measure the excitation quanta as degree of freedom in an electromagnetic signal
process			
pros/cons	better precision	more information but less precision	photon losses
output data	signal phase or frequency, signal spectrum	signal quadrature (in-phase and quadrature)	number of superposed photons or the presence of photons
implementation	homodyne interferometry	RF I/Q mixer, heterodyne interferometer, I/Q components analysis with ADC+digital signal processing	photodetection with SPAD, SNMPD, FMCW lasers, …
use cases	QKD detection with balanced homodyne detection (BHD)	qubit microwave readout processing, CV photon qubits readout	DV photon qubits readout

Figure 376: Explanation of the various ways to detect a photon or electronic signal with homodyne and heterodyne measurement and photon counting. 🅭 Olivier Ezratty, 2022.

(Quantum Instrumentation Control Kit) from Fermilab [3114] and its Manarat multi-board extension [3115], **QubiC** from Lawrence Berkeley National Lab, both from the DoE [3116–3118], **FASQuiC** from CEA List and Institut Néel to control spin qubits [3119] and FIREQ proposed by Italian researchers in 2026 [3120].

They are cost-efficient compared with many commercial solutions and are adapted to research laboratories. Several use Xilinx or AMD FPGA platforms, but only RFSoC-class devices integrate high-speed DACs and ADCs on the same silicon. Conventional FPGA boards use separate converter ICs. Researchers from Chalmers and KTH in Sweden created **Presto**, an integrated room-temperature controller based on a Xilinx Zynq UltraScale+ RFSoC [3121]. Researchers in China also developed the **M²CS** (Microwave Measurement and Control System), based on AMD Xilinx Zynq FPGA technology, with a proposed architecture scaling toward large channel counts [3122].

Active Technologies

Italy, 2003

Active Technologies is a spin-off of University of Ferrara creating AWGs and Pulse/Pattern Generators. It can control experimental solid state qubits as well as electro-optical and electro-acoustic modulators used with cold atoms qubits. Its flagship product is the AWG-5000, a fast 16-bit AWG with 8 output channels.

AQSolotl

Singapore, 2024

AQSolotl is developing room-temperature hardware for superconducting qubits. The startup was created by Patrick Bore (CEO) and Rainer Dumke (strategic lead) with Yap Yung Szen serving as CTO. It spun out of Nanyang Technological University (NTU) and the National University of Singapore (NUS). They developed the Chronos-Q control system, a hybrid quantum-classical platform supporting up to 16 XY qubit drive lines, with a state classification latency of 20 ns after the last sample and a power consumption of approximately 10 W per qubit controller.

The system comes with a Python software stack supporting pulse-level control, standard quantum experiments (Randomized Benchmarking, Ramsey, Spin Echo), and Qiskit/Qasm circuit-level integration, running on embedded Linux for network-based operation.

Chronos-Q has been deployed at Singapore's National Quantum Computing Hub (NQCH), forming the backbone of the country's first operational quantum processor platform. In 2025, they published research on the impact of signal control noise on qubit errors [3123]. Their roadmap targets advanced error correction at the 1 MHz logical operation scale, higher-density channel configurations, and a price reduction to below $100 per qubit by 2030.

Figure 377: AQSolotl Chronos-Q control electronics.

Basel Precision Instruments (2022, Switzerland) is a spin-off from the University of Basel which creates low-noise amplifiers and microwave filters used in low-temperature quantum physics as well as room temperature DACs.

CIQTEK

China, 2016, $15M

CIQTEK, aka Guoyi Quantum, develops high-precision pulse generator (ASG) and arbitrary waveform generator (AWG) used in qubit control, electron parametric resonance spectroscopes and scanning electron microscopes. They also manufacture NV centers-based magnetometers and <Diamond I>, a 2-qubit computing system for educational purposes. It is based in Hefei and has 500 employees.

Creotech Instruments

Poland, 2008

Creotech Instruments is a satellite electronics developer which developed Sinara, an electronic system to drive trapped-ion qubits that implements quantum errors mitigation protocols. It was built as part of the European Flagship AQTION project led by the University of Innsbruck. The system contains ADCs, DACs, digital I/Os, RF amplifiers, clock distribution, AWG and other electronic controls. Creotech also created an ultra-precise time synchronization platform based on the White Rabbit technology developed at CERN. The company decided in April 2025 to spin-out its quantum business to a separate entity (QKD, QRNG, time synchronization, control electronics, high-speed cameras). Meanwhile, Creotech will focus its activity on satellite systems.

Intermodulation Products

Sweden, 2018

Intermodulation Products is a spin-off company of KTH, the Royal Swedish Institute of Technology. They market Vivace, a microwave generator in the 4 GHz band used to drive superconducting qubits.

Keysight Technologie

USA

Keysight Technologies is an electronics measurement company spun-out of Agilent in 2014, which itself was coming from Hewlett Packard in 2000.

It then expanded its portfolio through several acquisitions: Signadyne (FPGA-based PXI digitizers and AWGs initially used with trapped-ion qubits) in 2016, Ixia (software), Liberty Cal (calibration services) and ScienLab (test solutions in eMobility systems) in 2017, Labber Quantum in 2019 (MIT spun-out specialized in qubit control and software) and Quantum Benchmark in 2021 (quantum error diagnosis and suppression, and benchmarking software). The company has now a broad portfolio of measurement and control electronic systems widely used in the quantum real, in its three markets: computing, sensing and communications, including optical instruments (Figure 380). Most quantum research labs already have some Keysight test and measurement systems. In qubit-control electronics, they provide pulse laser controls, basebands pulse controls and pulsed microwaves controls (AWGs like the M3202A PXIe Arbitrary Waveform Generator with 1 GSa/s, 14 bit sampling, DAC) as well as ADCs for qubit readout (like the M3102A 14-bit PXIe Digitizer). Interestingly, they address one source of electronic signals quality variability: the fluctuating room temperature. Thus, a solution to control rack temperature with air flow operating at 35°C.

Their Quantum Control System assembles various software and hardware components to drive single and multi-qubit lab experiments. The hardware part is the Quantum Engineering Toolkit (QET) and contains a PC workstation with a PXIe Interface Module, a PXIe chassis containing an AWG, a DAC, an in-phase/quadrature (I/Q) modulator and demodulator, a Vector Signal Generator and other optional electronics (Figure 378). Among other places, this toolkit is used since 2020 at the MIT EQuS (Engineering Quantum Systems Group) testbed.

Keysight is involved in several quantum computing related projects like the Boulder Cryogenic Quantum Testbed launched in 2019, a joint effort of Google, the NIST and the University of Colorado Boulder, housed in the JILA laboratory on the CU Boulder campus. It helps US researchers working on superconducting qubits at the characterization level. The lab is equipped with a 10 mK Janis JDry 250 mini dilution refrigerator. They also participate to MATQu, an EU funded German project which ambitions to produce superconducting qubits on 300 mm silicon-based process flows.

Keysight hardware is also used in quantum sensing (AWGs, ADCs, DACs, analog signal generation, measurement of current-voltage ("I-V") and capacitance-voltage ("C-V"), oscilloscopes) and CV-QKD signal generation and detection (with waveform/pattern generation, oscilloscopes, lightwave detectors and variable optical attenuators). In the vendors space, they partner with IBM on Qiskit Metal, an open-source software solution to design your own superconducting qubits to understand qubits crosstalk effects.

Keysight's current QCS is a modular PXIe platform using FPGA-based real-time processing and direct digital conversion for control and acquisition, with a Python API at the experiment-control layer. Current product documentation specifies direct digital operation up to 16 GHz.

Keysight announced a new generation of its Quantum Control System (QCS) in 2022, moving more waveform-generation and acquisition functions into dedicated

Figure 378: Keysight PXIe Quantum Control System.

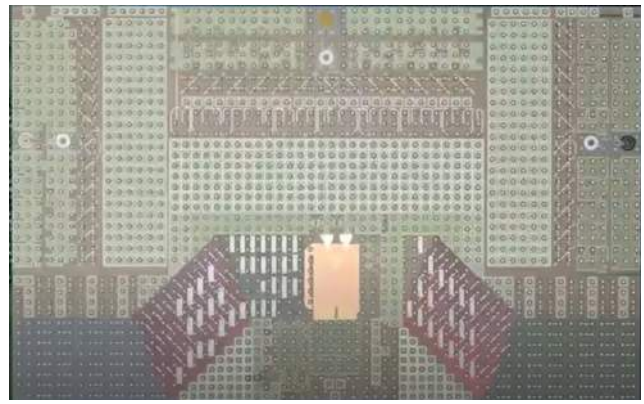


Figure 379: Keysight's first ASIC to control qubits.

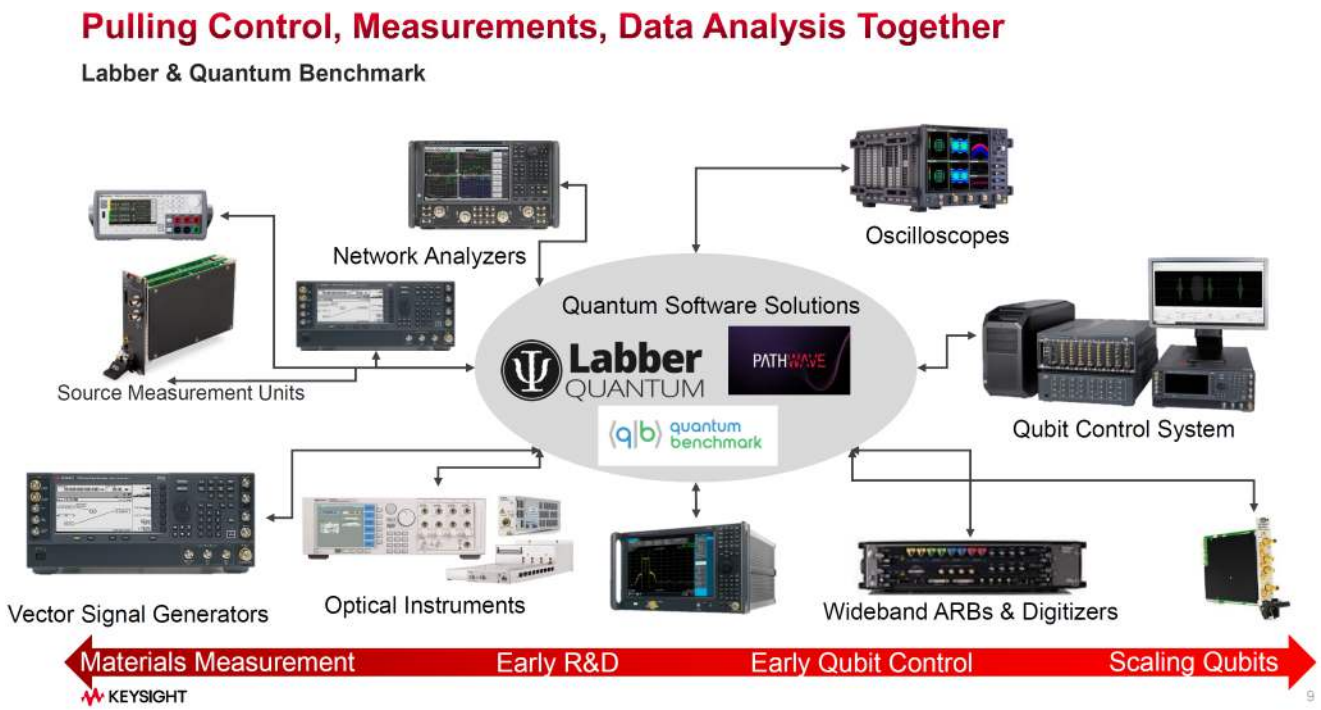


Figure 380: The Keysight control electronics family, mostly used in research laboratories. Source: Keysight. Added in 2022.

mixed-signal hardware (Figure 379). Current QCS generations use direct digital conversion and modular PXIe-based control and measurement hardware, with software APIs for experiment orchestration.

In August 2023, Keysight announced QuantumPro, an integrated EDA (electronic design automation) software tool for the design and simulation of superconducting qubits. It embeds five features into the PathWave Advanced Design System (ADS) 2024 platform with schematic design, layout creation, electromagnetic analysis, nonlinear circuit simulation, and quantum parameter extraction. The product was released in February 2024 [3124]. Keysight created a Quantum Circuit Simulation (Quantum Ckt Sim W3703B) along with Google in 2024, and extension of ADS.

Qblox

the Netherlands, 2018, $31M

Qblox is a spin-off from QuTech that develops scalable control electronics for superconducting qubits. As of late 2025, the company had a staff of 175 people.

Qblox Cluster systems combine qubit-control modules and qubit-readout/acquisition modules in a modular rack architecture (Figure 381). Their exact qubit capacity depends on how many drive, flux and multiplexed readout channels are allocated per qubit. The modules use FPGA-based real-time processing together with DACs and ADCs.

They also sell the desktop Pulsar QRM (quantum readout module) that handles a few qubit control in small factor format. As their Cluster modules, these can be

Figure 381: Qblox modular systems can control up to 60 qubits in a 4U chassis containing 20 modules. Source: Qblox, 2023. Added in September 2024.

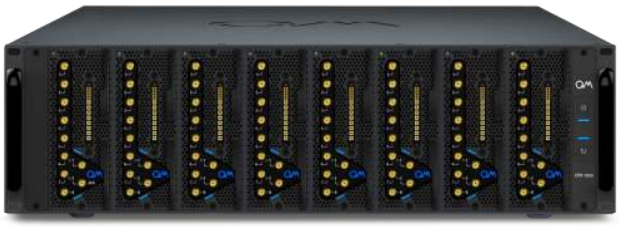


Figure 382: Quantum Machines OPX1000 is a full-stack solution for qubit control and measurement, enabling closed-loop error correction with 64 output lines for qubit control and 16 input lines for qubit readout, spread over 8 modules in this configuration, and packed in a 3U rack. Source: Quantum Machines. 2023.

coupled and synchronized together using their home-grown protocols SYNQ (synchronized start within «1 ns) and LINQ (distributing measurement outcomes in <200 ns).

Their architecture could scale up to control 1,000 superconducting qubits. Calibration is done with the help from **Orange Quantum Systems** and cabling comes from **Delft Circuits**, two other spin-offs of QuTech in the Netherlands.

Qblox developed in 2023 their Q-Profile benchmarking tool to benchmark and optimize control electronics. On a small scale QAOA implementation with up to 14 qubits, they used it to optimize the algorithm speed by x3 [3125].

Qblox is present in the USA through a manufacturing unit in Massachusetts which started production in 2026, in partnership with Prodrive Technologies, another Dutch company present in the USA, completing a support group in Boston. Among other customers, they work with the DoE's Fermilab.

Quantum Machines

Israel, 2018, $280M

Quantum Machines provides a qubit control layer for quantum computers that combines hardware and software [3126].

It is a spin-off from the Braun Center for Submicron Research Laboratory at the Weizmann Institute. The company had a staff of 150 and 250 customers throughout the world as of August 2023. The company was created by Itamar Sivan (CEO, who did a Master's degree at the ENS Paris between 2009 and 2011), Yonathan Cohen (CTO, former Weizmann Institute managing director) and Nissim Ofek (Chief Engineer, who had a post-doc position in Rob Schoelkopf's lab in Yale University where he developed a FPGA based control and QEC code).

They developed their own classic qubit control processor, an FPGA operating at room temperature, which generates the pulses for controlling qubit gates and readout either with microwaves or lasers. Packaged as their OPX/OPX+ systems, it supports superconducting (working for example with Rigetti), electron spin, NV centers, trapped ions and cold atoms qubits (working with QuEra). In March 2022, they announced the availability of Octave, a compact and rack-mountable all-in-one RF up/down-conversion module which completes their OPX systems. It contains its own built-in Local Oscillator (LO) sources and provides continuous self-calibration features. In August 2023, Quantum Machines announced its OPX1000 3U high-density controller. In the configuration described in the manufacturer material consulted in September 2026, it supports up to 64 outputs and 16 inputs, out of up to 80 analog channels per 3U chassis depending on the front-end modules fitted, compared with 10 outputs and 2 inputs in the OPX+ (Figure 382) [3127].

They partner with Q-CTRL which develops qubits firmware level control software. Their processor is integrated into their "Quantum Orchestration Platform", which also combines a software layer [3128]. In June 2020, they announced the creation of the **QUA** language, positioned as a language for creating hybrid quantum and classical algorithms, such as VQE and QAOA, which need rapid feedback between classical and quantum processors. This programming language works with all types of qubits, superconductors, silicon, cold atoms and trapped ions. The compiler thus takes into account the differences in the implementation of qubits: their connectivity, the homogeneity or heterogeneity of their coupling, the coherence times, the error rates, etc.

In March 2022, Quantum Machines acquired **QDevil** (Denmark) which gives them a foothold in the cryogenic electronics space with filters and a low noise DACs. In February 2023, QDevil introduced QCage.64, a superconducting test chip carrier enabling high-fidelity operations. The qubit chip is enclosed in a microwave cavity to minimize losses and decoherence. It has 64 transmission lines enabling testing of up to 30 qubits

(Figure 383). They also sell magnetic shielding and flexible cabling. In May 2026, they also acquired the TU Delft spin-off QHarbor created by Alberto Tosato and Stephan Philips, which developed a data storage and visualisation software platform for physics researchers. This enabled Quantum Machines to establish an EU R&D's base.

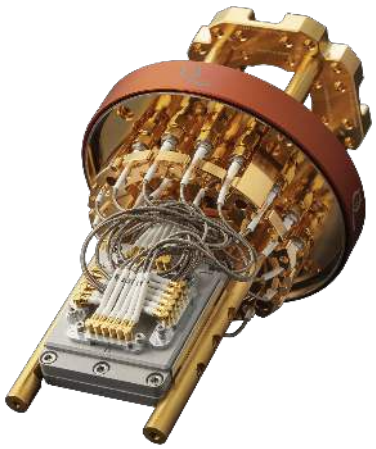


Figure 383: QDevil QCage.64 chip packaging for a superconducting qubit chip. Source: QDevil. December 2023.

Quantum Machines has a partnership with Nvidia to develop low-latency controls using Nvidia DGX servers with classical GPGPUs. In March 2023, they both announced the integration of Quantum Machines OPX+ with the latest Nvidia DGX using the Grace Hopper system through a PCIe bus enabling very low latency in the sub-microsecond scale between GPUs and QPUs [3129]. It will enable them to characterize quantum error correction experiments [3130].

Quantum Machines released in 2025 QUAlibrate, an open-source framework to reduce calibration times and streamline the calibration process for quantum computers across platforms. It can process multi-qubit calibration in under 3 mn, with upcoming support of NVIDIA DGX Quantum. Qolab is one of their first customers.

Also in 2025, Quantum Machines published a preprint for estimating the resources to implement Shor integer factoring algorithm with 5 logical qubits, 1,000 physical qubits, and to factor the integer 21 [3131]. It supported non-Clifford gates (T) but not in a fault-tolerant manner (aka: no magic state distillation). It would require 99.9% qubit fidelities. Surprisingly, if the paper provides some constraints on controller (100s ns) and decoder latency (10 μs), it didn't say anything on how much control hardware was required and how cabling would scale.

QuantrolOx

Finland-UK, 2021, $8M

QuantrolOx is an enabling technology company creating a deep learning software solution to optimize the automatic tuning and optimization of qubits settings [3132, 3133].

The company leadership includes Vishal Chatrath (CEO, UK), Andrew Briggs (Executive Chair, UK, Professor of Nanomaterials, University of Oxford), Natalia Ares (Chief Scientist, UK, with a strong background on quantum thermodynamics and machine learning, Professor at the University of Oxford), Dominic Lennon (Head of Quantum Technologies, UK, also from Oxford University) and Juha Seppä (CTO, Finland). It had about 35 employees as of mid-2026. Mostly based in the UK, the startup is positioned as a Finnish one, maybe to make it easier to get some EU funding! Their first investors are Nielsen Ventures, Hoxton Ventures, Voima Ventures, Remus Capital, Hermann Hauser (cofounder of Arm) and Laurent Caraffa.

Their solution Quantum Edge that was developed with the help from Google DeepMind is using small training data sets and works in two steps: one with coarse tuning and a second with fine tuning. It efficiently adjusts the parameters of many qubits and is applicable to all sorts of qubits but particularly with those who express the largest variability like superconducting and electron spins qubits. In August 2023, they integrated their solution with Qblox control electronics for the drive of superconducting qubits. As of late 2024, they also support Quantum Machines, Zurich Instruments and Keysight control electronics solutions. Quantum Edge is integrated into VIDYAQAR, a complete quantum platform with a Bluefors LD400sl cryostat, Qblox control hardware, and a 7-qubit quantum processor ConScience QiB2.

Among their various partnerships, they established one in March 2026 in India with Manipal Academy of Higher Education (MAHE), for the development of Quantum-Hub@MAHE (Q-HUB@MAHE) at Manipal Institute of Technology (MIT), Bengaluru. They will deploy there their VIDYAQAR platform with the goal to scale the platform to 50–150 and then 150–1,000+ qubits.

Quaxys

USA, 2020

Quaxys provides hardware and software solutions for superconducting and spin qubits electronic control, including Quantuware 4840, a compact qubit control and measurement unit, and mostly for educational tasks.

Teledyne E2V

USA/UK/France

Teledyne E2V is a designer, manufacturer and provider of DACs and ADCs circuits used for microwave processing with superconducting qubits, noticeably with IBM. These are designed and manufactured near Grenoble, France.

Socionext

Japan, 2015

Socionext is a fabless semiconductor company that works with Google to help them develop their next generation controller systems on chip.

SDT Quantum

South Korea, 2023, $7.5M

SDT is a startup created by Yoon Ji-won (CEO) which is specialized in QPU control equipment: photon counting, pulse generation, time tagging and a qubit controller. It is sort of a South Korean Quantum Machines. They announced a partnership with SemiQon in November 2024.

They also provide a QRNG and some QKD hardware, plus some sort of quantum cloud computing offering. They created the first South Korean quantum computer, in collaboration with KIST, KISTI (Korea Institute of Science and Technology Information) and Seoul National University. First, with a 20-qubit superconducting qubit QPU in 2026, then on cold atoms and silicon qubits to be released in 2027 and onward. Focus is not part of their tagline!

SynkTek

Sweden, 2015

SynkTek is an electronic system provided spun-out from the department of physics of Stockholm University. They flagship product is the multichannel lock-in amplifier MCL1-540. It synchronously measures up to 10 analog input voltages and 5 outputs currents.

Tabor Electronics (1971, Israel) is an electronics devices company (ODM) that manufacture products on demand. They developed various AWGs, PXIe chassis and signal amplifiers. They are collaborating with FormFactor and QuantWare.

WiMi Hologram Cloud

China, 2015

WiMi Hologram Cloud is a company working in the augmented reality space which markets an FPGA-based platform that it describes as a quantum coprocessor. The public documentation describes FPGA and RFSoC-based classical control and readout, as is the case for QICK and QubiC, so the quantum-coprocessor label is not supported by the available evidence.

Zurich Instruments

Switzerland, 2008

Zurich Instruments is a manufacturer of electronic test and measurement equipment, including a range of microwave generation and analysis tools.

The company was acquired by Rohde & Schwarz in July 2021. Their offer is built around their Quantum Computing Control System, which bridges the gap between the quantum computer software control tools and the associated electronic instrumentation.

This system consists of several components. First, the PQSC (Programmable Quantum System Controller, which is used to program and control all the devices. It is equipped with a Xilinx UltraScale+ FPGA that can be driven by the LabOne software using Python, C, MATLAB, LabVIEW and Microsoft's .NET framework.

It controls multiple HDAWG (High-Density Arbitrary Waveform Generator) instruments and can be scaled by synchronizing several instruments. LabOne became LabOne Q in October 2022 with extensions for configuring and optimizing Zurich Instruments hardware. These generators create shaped microwave pulses, for example Gaussian or DRAG-like envelopes as in Figure 385, in frequency bands adapted to superconducting-qubit drive and readout. A resonant transverse microwave drive induces coherent transitions and Bloch-sphere rotations between the qubit states.

This is complemented by the UHFQA (Ultra-High Frequency Quantum Analyzer) which can analyze the readout state of 10 qubits. In the diagram, F_{LO} is the frequency of the microwave signal to be modulated and F_{IF} is the modulation waveform (Figure 386). On the UHFQA side, the system detects the modulation or phase modification of the signal recovered through a resonator associated with the qubits, l_g and l_e respectively for ground states and excited states.

In April 2021, Zurich Instruments launched a new signal generator, the SHFSG with better micro-waves signal spectral purity and stability. It can handle up to 144 qubit control channels and is accommodated with 4 or 8 channels, controlling up to 8 qubits. In August 2022, they introduced their SHFPPC (Super High Frequency Parametric Pump Controller), a room temperature tone pulse generator that feeds the parametric amplifiers like the TWPAs sitting at the lowest stage of the cryostat.

Figure 387: An SHFQC can control up to 16 qubits.

It was then completed by the software reconfigurable and programmable SHFQC launched in November 2021 (Figure 387), which bundles 6 signal generator control channels and a readout channel analyzer supporting up to 16 qubits. Several SHFQC can be combined to support up to 100 qubits and "beyond".

Launched in August 2023, the QHub Quantum System Hub coordinates these various devices assembled in several QCCS (Quantum Computing Control System,

Figure 384: Zurich Instruments QCCS containing a PQSC (program and control), two HDAWG (arbitrary waves generators) and three SHFQC (signal generators and readout) and one SHFPPC (tone pulse for parametric amplifier) for qubit control and readout.

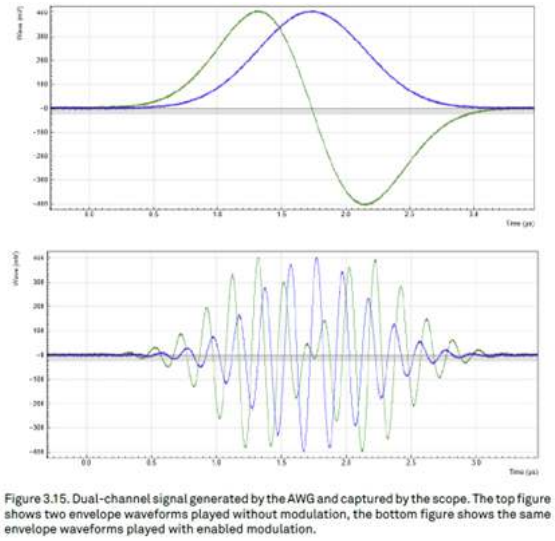


Figure 385: Types of microwave pulse signals generated. Source: Zurich Instrument product documentation. 2023

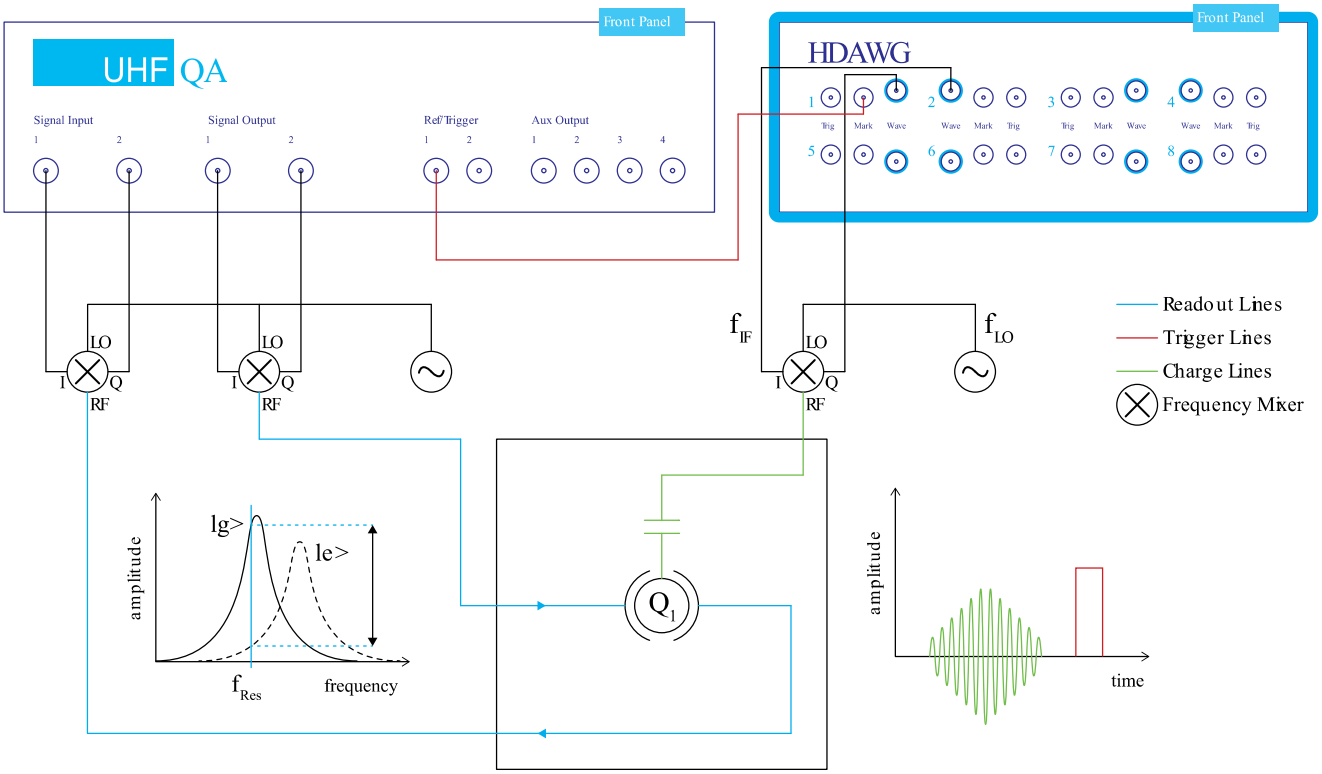


Figure 386: UHFQA and HDAWG cabling. Source: Zurich Instruments.

shown in Figure 384). It can synchronize up to 448 microwave channels, enabling the control of over 100 superconducting qubits.

In March 2024, Zurich Instruments launched its SHF+ series for superconducting-qubit control and readout, including the SHFSG+ Signal Generator, SHFQC+ Qubit Controller and SHFQA+ Quantum Analyzer, with improved analog signal quality. Higher SNR and lower phase noise can improve control and readout fidelity. During spring 2024, Zurich Instruments also announced integration of its QCCS and SHF+ family with QuantrolOx's Quantum EDGE automation tools. QCCS is also used by Photonic Inc., while QuantWare's Crescendo-S TWPA can be pumped using the Zurich Instruments SHFPPC.

In March 2026, Zurich Instruments introduced the ZQCS Quantum Control System, a control plat-form adapted to large scale systems and handling direct RF synthesis. FPGA-based, it supports more than a thousand control channels per 19-inch rack and water-cooling.

Zurich Instruments is also developing a TWPA (traveling wave parametric amplifier) for qubit readout, along with EPFL, Withwave (South Korea), and SKKU through the Q-LAEP project [3134].

NF Corporation (1959, Japan) provides low noise power supplies, **Seiken Co** (1984, Japan) provides sockets for quantum chip mounting, **Kawashima Manufacturing** (1953, Japan) provides high-frequency connectors and **Nitsuki / Japan Communication Equipment** (1949, Japan) provides low noise amplifiers and HEMT.

Origin Quantum also develops its own control electronics, the latest being Tianji 4.0, which supports over 500 qubits.

There is also a project in China for a superconducting microwave generator for the control of superconducting qubits based on a Xilinx FPGA [3135]. In other similar and older projects, China's research teams showcased scalability claims that were not really sustained by a real scalable architecture [3136].

2.2.2 Cryo-CMOS

Cryo-electronics sit inside the cryostat, control the qubits and manage their readout in place of some of the external electronic devices we have just covered, totally or partially depending on the systems generation.

Many research teams and industry vendors are working on this set of technologies which may help to unlock qubit scalability. They include the **University of Sydney**, **TU Delft** in the Netherlands [3137], **VTT** in Finland, **CEA-Leti** and **CNRS Institut Néel** in France, **POSTECH** in South Korea, **ITRI** in Taiwan and research teams in China [3138], as well as industry vendors such as **Intel** and **IBM**. Cryo-electronics could reduce expensive and cumbersome cabling, filters, attenuators and some amplification or conversion functions, while shortening control and feedback paths. The trade-off is the electrical power dissipated inside the cryostat and the resulting refrigeration overhead.

Figure 389 describes the variety of component functions that can be integrated in the 1 K to 4 K stages and even, when possible, at the qubit chip stage at less than 20 mK [3139]. These components must be certified to operate at these temperatures. These are data multiplexers and demultiplexers, local oscillators, AWGs, DACs, ADCs, low-noise amplifiers, DC flux bias generators, thermometers and other various sensors. The trend is to put within the cryostat a maximum of these electronic components.

All these components should be integrated in a minimum number of chips, preferably one, and working as close as possible to the qubit chip. But not too close to avoid heating the qubits. It is another trade-off between thermal considerations and cabling requirements. So far, the best level of integration has been obtained with **Intel** Horse Ridge 2 announced in 2021 at the 4 K stage, and the coldest operation was achieved with the Gooseberry chip from **Microsoft** and the **University of Sydney** as well as with a cryo-CMOS from **CEA-Leti** sitting next to the qubits. These two placements, at the 4 K stage and at the qubit level, are the two main approaches followed so far.

Cryo-CMOS operating at 4 K. The first approach was to miniaturize these circuits at the 4 K stage of the cryostat. It was studied in 2019 at **TU Delft** for silicon qubits state readout with their QuRO, for Quantum Read-Out, using microwaves photon reflectometry [3141]. The technique allows multiplexing qubit readout before sending the information out of the cryostat, which simplifies the output wiring. The prototype relied on standard market off-the-shelf passive and active components operating correctly at 4 K and did not deal with the waveform generation and DAC circuits driving qubit gates. **IMEC** (Belgium) developed in 2020 a cryo-CMOS RF MUX multiplexing the in and out microwave signals used in qubit readout and working at up to 10 GHz, suitable for superconducting qubit readout [3142]. They created a similar solution operating at 15 mK in 2022 that is suitable for time-domain microwave multiplexing for the drive of superconducting qubits [3090].

A similar approach was initially adopted by **Intel** in collaboration with **QuTech** for its 2020 HorseRidge superconducting and silicon qubit driver, capable of handling microwave pulses from 2 to 20 GHz and sitting at the 4 K stage of the cryostat [3143]. Introduced in 2021, **Horse Ridge 2** improved cryo-electronics integration to an unprecedented level (Figure 390). It added multigate pulsing making it possible to control several qubits simultaneously, qubit readout and a programmable microcontroller. Gate pulsing creates multi-qubit gates with square DC signals controlling the barrier and plunger gates of the quantum dots while single-qubit gates use modulated RF signals and qubit readout use regular RF signals. The chip uses frequency multiplexing to reduce the number of RF cables for qubit drive and readout. It drives up to 16 spin qubits with frequency ranges between 11 and 17 GHz, reads the state of up to 6 qubits simultaneously, and contains 22 DACs to simultaneously control the gate potential for many qubits. The chip was manufactured in a 22 nm low-power FinFET technology (22FFL), operates at 4 K and contains 100 million transistors [3144]. In May 2021, Intel and QuTech demonstrated high-fidelity two-qubit control with this HorseRidge 2 control chip.

In June 2024, Intel presented a solution to multiplex qubit control signals between the 4 K and 10-20 mK

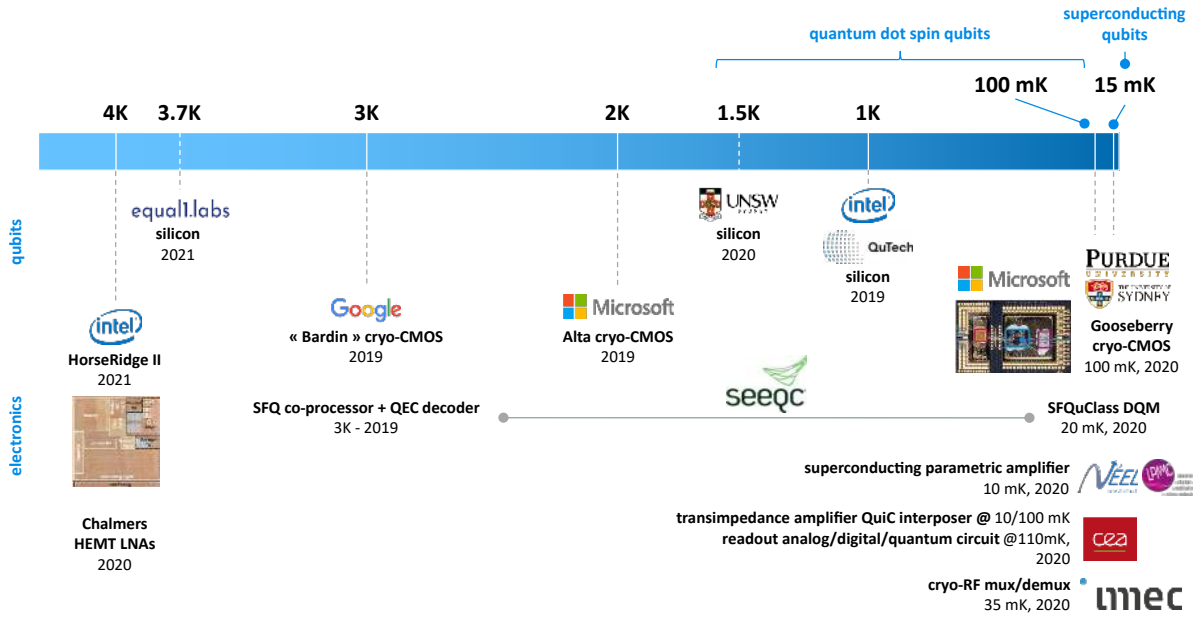


Figure 388: Comparison of the temperature and feature of various qubits and cryo-electronic chips operating at various temperatures from 15 mK to 4 K. ⓒ Olivier Ezratty, 2022.

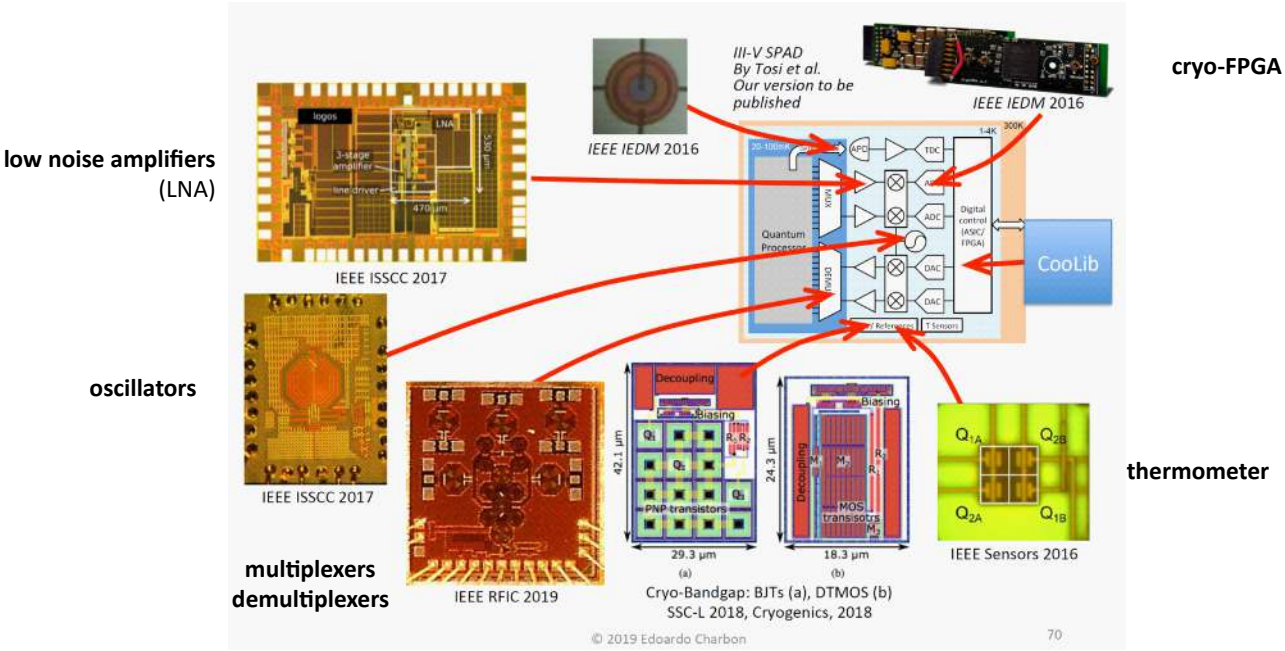


Figure 389: Initially, research labs tried to build specific cryogenic component chips for many qubit control functions. Then, players like Intel tried to consolidate these in fewer components. There are still many components around, even with integrated cryo-CMOS for qubit control and readout, like the parametric amplifiers and HEMT. Source: [3140].

stages, Pando Tree [3145, 3146]. As shown in Figure 391, Intel's Pando Tree is a cryo-CMOS chip that sits at the same 10 to 20 mK temperature as its experimental qubit chip Tunnel Falls, introduced in 2023. Both are integrated into the same PCB (printed circuit board). Pando Tree demultiplexes control signals coming from the 4 K stage which contains the Horse Ridge II chip. Currently using a single signal line and nine addressing digital control signals, it delivers both DC voltage bias and microwave pulses to up to 64 qubit terminals. The system scales well as multiplexing N lines requires only log(N) signal lines, with only 20 cables needed to control one million qubits.

In 2022, **POSTECH** from South Korea proposed a similar architecture to HorseRidge 2 with a CMOS SoC sitting at 3.5 K and adding local oscillators. It was prototyped in 40 nm TSMC bulk CMOS and consumes about 15 mW per qubit [3148]. **IBM** is also designing cryo-CMOS components. They prototyped the first one manufactured in a 14 nm process. It supports 4.5-to-5.5 GHz RF AWG for pulse control generation and does not rely on TDM or FDM (time or frequency multiplexing)

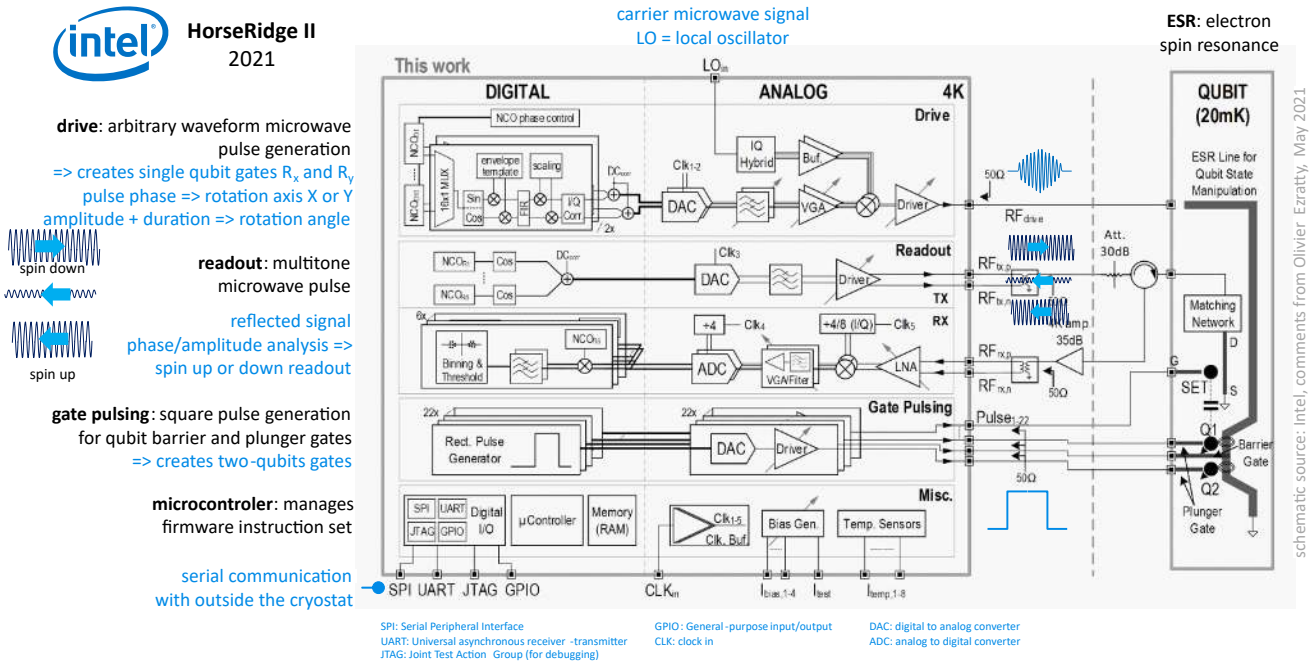


Figure 390: Intel HorseRidge 2 presented in 2021 was then the most integrated cryogenic qubit control chip being developed. Source: [3144].

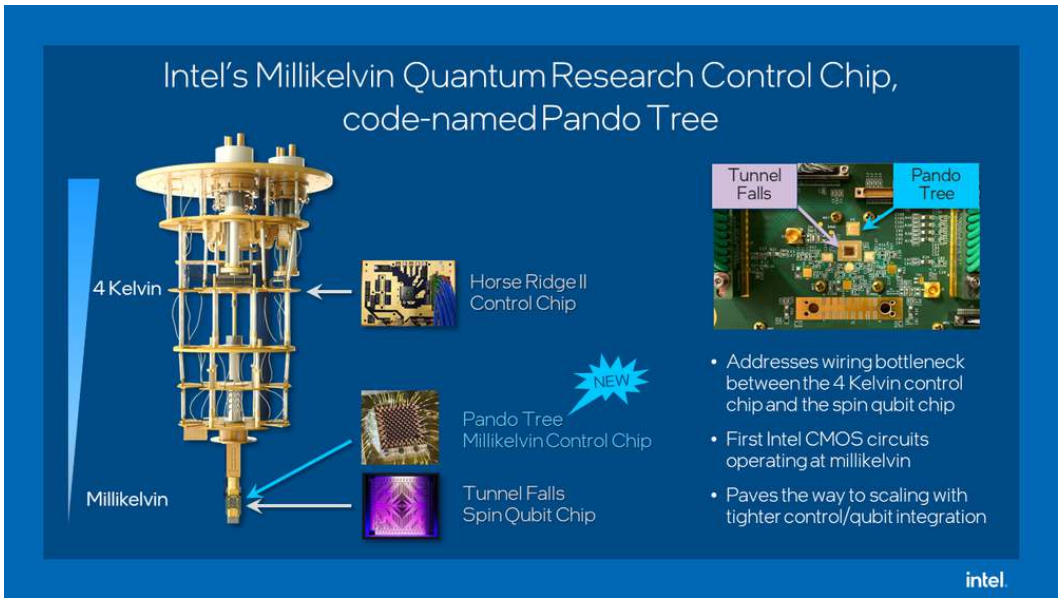


Figure 391: How Intel Pando Tree presented in 2024 fits in the Intel control chain that includes the Horse Ridge II signal-generation chip at 4 K and the Tunnel Falls qubit chip at millikelvin temperature, between 10 mK and 20 mK. Source: [3147].

[3149]. However, it seems that LO (local oscillator) leakage negatively impacts gate fidelities and will need some work. IBM created blueprints to integrate all readout features in such chips in the future [3150]. In another work published by an **EPFL** team in January 2021, a 40 nm CMOS chip operating at 50 mK hosted both 9 silicon quantum-dot qubits organized in a 3x3 array and some digital electronics using analog LC resonators implementing time- and frequency-domain multiplexing for qubit readout [3151]. Another 2023 iteration of the chip added a full implementation of a cross-resonance two-qubit gate drive with the same energy consumption per qubit [3152]. It contains a SRAM based AWG, a technique that IBM also prototyped in 2022 to drive spin qubits [3153]. Some academic teams are even studying the integration of cryo-CMOS and silicon quantum-dot spin qubits on a single chip, at this stage, only for qubit drive signals demultiplexing [3154, 3155].

The most complete 4 K-stage demonstration as of 2026 came from **HRL Laboratories** (Malibu, owned by Boeing and General Motors, and being acquired by IBM in

2026) with a fully digitally controlled silicon quantum processing unit. It assembles three pieces in one package: a cryo-CMOS controller, a high-density superconducting ribbon cable, and an 18-qubit SiGe silicon spin qubit chip holding a three-rail array of 54 exchange-coupled quantum dots. The controller is a mixed-signal SoC in 130 nm RF CMOS with about 70 million transistors on a 21×19 mm^2 die. It sits at the 4 K stage and generates all qubit control signals. It draws less than 3.5 W at the 4 K stage and routes around 150 control waveforms down to the mixing chamber hosting the qubit chip with less than 10 μW of added thermal load, keeping the qubit temperature near 150 mK. The system reached average single-qubit gate errors of 1.7×10^{-4} and CNOT errors of 3.5×10^{-3}, and it ran a distance-5 repetition code and a quantum error-detecting code [1341] (HRL-Lab-CryoSIGe).

Cryo-CMOS at qubit temperature. The second approach brings the electronics down next to the qubit chip, at millikelvin temperature. In 2019, an American-Australian team from the **University of Sydney**, **Purdue University** and **Microsoft Research** designed Gooseberry, a CMOS circuit to control superconducting, electron-spin or (yet to be seen) Majorana-based qubits (Figure 393). Designed by David Reilly's team from the joint Microsoft Quantum Laboratories at the University of Sydney, it is operating at 100 mK, just next to the qubit circuit on the same PCB support but without supposedly disturbing the qubits. It uses a round-robin scheme to distribute modulated microwaves sequentially to each qubit, with the microwave carrier signal source (LO or local oscillator) positioned outside the cryostat and qubit readout done here with external circuits (ADC and FPGA). It was a bit the opposite of Harald Homulle's solution from TUDelft. The test CMOS was realized in FDSOI in 28 nm and this low-power chip generated control pulses of 100 mV at 18 nW per cell [3156]. A team from **Diraq** tested the Sydney/Purdue/Microsoft cryo-CMOS chip next to their silicon qubit chip in 2024 and found out that it didn't impact their qubit gate quality [92].

In 2020, **CEA-Leti** in Grenoble created a mixed analog, digital and quantum cryo-CMOS circuit manufactured in 28 nm FDSOI and operating at 110 mK. It handles all the qubit driving and readout cycle with charge pumping, generating continuous tone GHz microwaves and measuring the induced current with a multiplexed transimpedance amplifier (TIA). At this experimental stage, it drives only a couple qubits but looks promising with regards to the ability to control quantum-dot qubits at their operating temperature. And the quantum dot qubits were in the circuit itself! One key technology to master when assembling electronic components at the qubit level is packaging and connectivity. That's where a French team from **CEA-Leti**, **CEA LIST** and **CNRS-Institut Néel** made progress in February 2021 with building a prototype interposer named QuIC (Quantum integrated circuits with cryo-CMOS), operating at below 1 K and using a 3D flip-chip process, with control electronics made on standard FDSOI 28 nm by STmicroelectronics [3157]. The integrated packaging avoids chip wire bonding since qubits and control electronics are coupled by routing lines on the interposer, and it allows thermal decoupling between the quantum chip and the electronics control chip. CEA is also replacing indium bumps with other materials that are compatible with existing CMOS manufacturing processes, like SnAg microbumps and directly bonded Cu pads from Cu/SiO_2 [3158].

Another use case came from **Fujitsu** (Japan) who created a cryo-CMOS circuit to drive NV-center chips at 4 K, along with QuTech (The Netherlands) [3160]. As a result, a NV-center based QPU could assemble an NV-center circuit and its control electronic circuit in the same location in a cryostat.

Cryo-CMOS for error correction. A recent role for cryo-CMOS is to handle part of the quantum error correction pipeline inside the cryostat, upstream of the room temperature decoders and after cryo-CMOS based qubit readout. In a large fault-tolerant machine, the syndrome data coming out of the qubits saturates the 4 K to room temperature link in both bandwidth and power, and this becomes a scaling bottleneck of its own. The idea is to place lightweight predecoders at the 4 K stage that handle the common and sparse errors locally and only send the rare complex events up to the full decoder outside, which cuts the outgoing data rate while preserving logical fidelity. IBM and G. S. Ravi proposed such a lightweight cryogenic decoder for trivial errors [3161], an approach later refined in cryo-CMOS with Pinball, a surface-code predecoder characterized under realistic circuit-level noise [3162]. Other options include approximate in-fridge correction [3163] and a cryogenic CMOS-memristor neural decoder [3164]. A complementary path compresses the syndromes instead of decoding them: CryoZip, realized in 22 nm FDSOI at 4 K, reaches up to 48× syndrome compression with 4 to 26× energy savings, and over 14,000× bandwidth reduction when paired with a predecoder [3165].

Cryo-CMOS could also be potentially connected to the outside of the cryostat using short range 28 GHz wireless communications [3166–3168]. Optical links are another candidate, with high data rates, low attenuation and no thermal conduction along the fiber. CO-QLink demonstrated a 4K heat-insulated transceiver reaching 56 Gbps at 1.6 pJ/bit between the 4 K stage and room temperature, co-packaged with a PIN photodiode and a C-band laser [3169].

Thermal dissipation. The heat released by cryo-CMOS is constrained by dilution refrigeration system cooling power [3170–3172]. It conditions at which cold plate stage these components can operate. There is a complicated trade-off between the cryostat power overhead and what is saved by reducing cabling and filters between room temperature and the 4 K cryostat stage where most of these Cryo-CMOS circuits are installed. Bringing chips closer to the qubits also shortens the

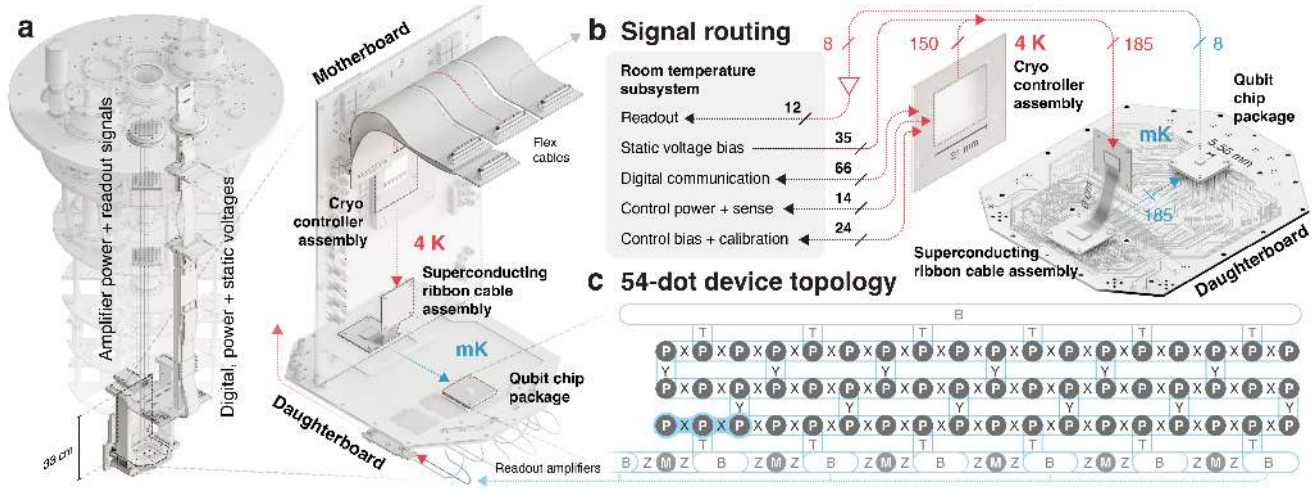


Figure 392: HRL Lab setup presented in Nature in 2026 just before its announced acquisition by IBM. It shows (a) the processor installed at the bottom of a dilution and connected to room temperature with flex cables and coaxial lines. It contains a controller motherboard operating at 4 K, a qubit daughterboard operating at 150 mK, and superconducting ribbon cable connecting the two boards. It also uses transimpedance amplifiers operating at 4 K but located below the daughterboard. (b) the room temperature control subsystem provides digital signaling and static current and voltage biases, qubit readout signals digitization, a ribbon cable transmitting all 150 qubit control signals from 4 K to mK with minimal thermal load. (c) topology schematic of the quantum chip with its 54 quantum dots supporting 18 physical SiGe qubits in a 3×6 square lattice with nearest-neighbor coupling. Source: [1341].

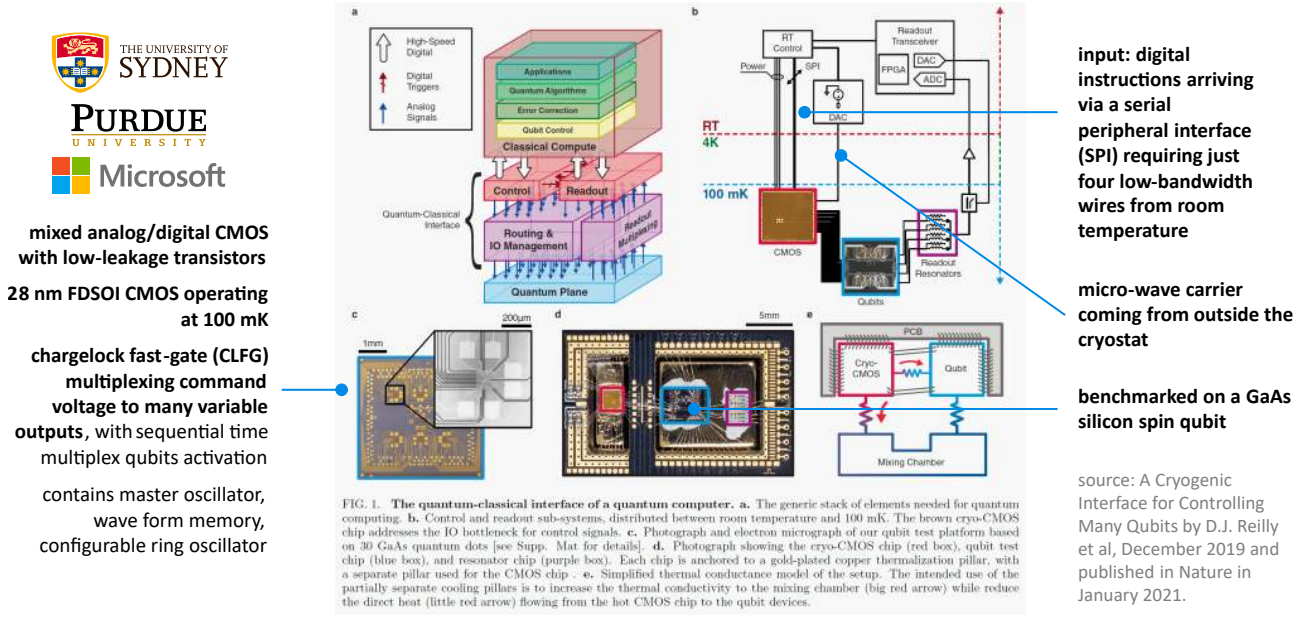


Figure 393: Microsoft prototyped in 2021 a control chip that supported fewer functions than HorseRidge but it could run next to the qubit chip at lower temperature, suitable for silicon spin qubits. It closed its Australian team handling this project in 2024, which led to the creation of the startup Emergence Quantum in 2025. Source: [1744].

wiring and the readout latency, but too close a placement heats the qubits, which is why packaging matters, as with the CEA interposer that thermally decouples the quantum chip from its control chip.

Energetics. Cryo-CMOS dissipation must be converted into wall-plug power through the refrigerator's temperature-dependent coefficient of performance. As an order-of-magnitude illustration, 25 mW dissipated at 4 K combined with a 200× wall-plug overhead would correspond to about 5 W at room temperature, and one million such independent 25 mW loads would therefore correspond to about 5 MW. This is an illustrative extrapolation, not a universal per-qubit requirement, because practical controllers share functions across many qubits and refrigerator overhead depends on the cryogenic architecture. Other power drains include decoding, data movement and room-temperature control. One research avenue is more energy-efficient or partially reversible digital logic [3173]. Cryo-CMOS is generally thermally easier to integrate with spin qubits operating at several

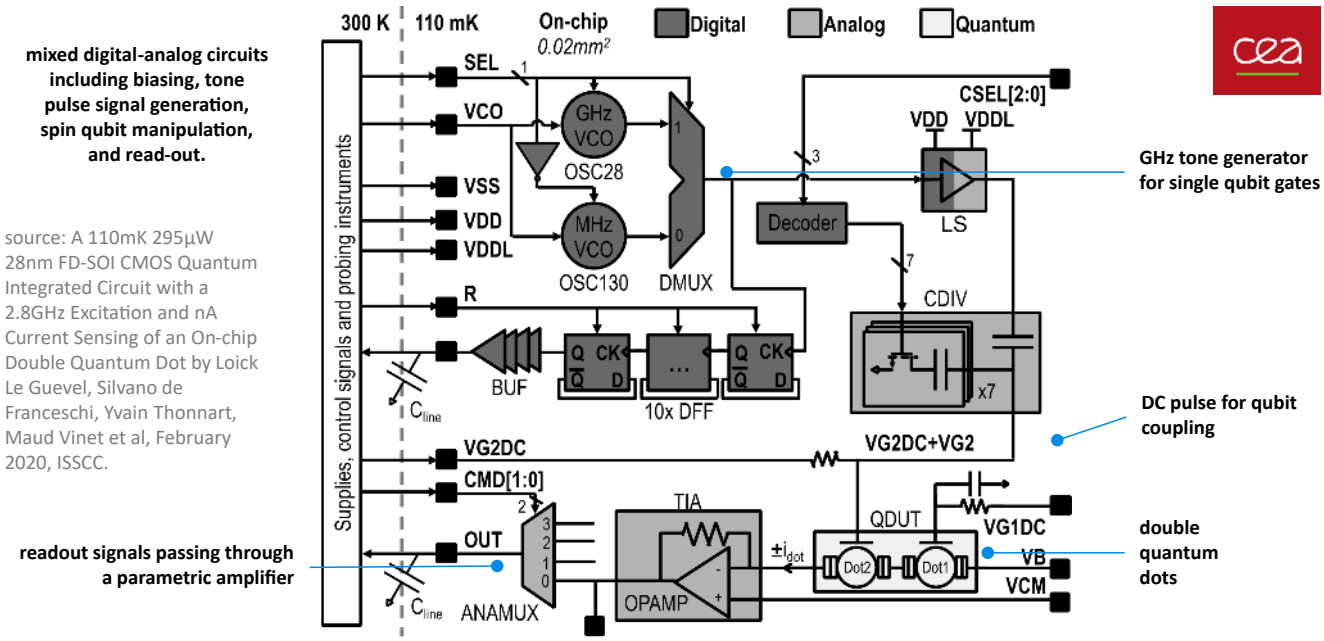


Figure 394: This chip from CEA-LIST created in 2020 did operate at the same temperature as Microsoft's chip seen in Figure 393. It was tailored for silicon spin qubit control. Source: [3159].

hundred millikelvin or above than with superconducting qubits near 10-20 mK, although the optimum remains architecture-dependent.

Table 14 contains a detailed comparison of the various cryo-chips studied in the section and the next on superconducting logic. It shows a discrepancy of power consumption per qubit which is explained by several factors: the different electronic features supported by the chips, their mutualization across a given number of qubits and the manufacturing node technology. It is completed by Figure 395 which shows which part in the table corresponds to which function in the pulse management sequences from qubit drive to qubit readout.

Emergence Quantum

Australia, 2025

Emergence Quantum is a contract research company created by Microsoft's lab in Australia alumnis, David Reilly (CEO) and Thomas Ohki. Their activities cover control and readout cryogenic electronics applied to scaling quantum computers regardless of qubit modality (spins, trapped ions, atoms, photonics, superconductors), energy-efficient and cryogenic classical computing for data centers and edge platforms (including neuromorphic, reservoir, and analog approaches), and scalable cryogenic sensing interfaces with quantum-limited amplification [1744, 3186–3188]. It works with companies like Diraq, IonQ, Archer Materials, PsiQuantum and Maybell Quantum.

Frostbyte

the Netherlands, 2025, €1.3M

Frostbyte was created at Delft by James Kroll (CEO) and Luc Enthoven (CTO) with the scientific backing from Fabio Sebastiano and Masoud Babaie. It is designing cryo-CMOS. Its first products are a family of cryogenic RF switches with the plan to extend it to qubit control and read out.

Irréversible Inc

Canada, 2024

Irréversible is a spin-out of Sherbrooke University that is developing a hybrid ASIC cryo-CMOS and memristor component to handle syndrome decoding in quantum error correction using a recurrent neural network at low temperature with in-memory processing. It can operate at 1.2 K [3164].

IceCirc

Germany, 2026

IceCirc is a spin-off of FZ Jülich created by Stefan van Waasen, Lotte Geck Patrick Vliex and Dr. Dennis Nielinger, and coming from the Institute for Integrated Computing Architectures (ICA / PGI-4). It develops low-power cryogenic ASICs to control and read out large numbers of qubits. They want to scale from 1,000 to a million qubit. They tailor electronics to specific qubit physics, notably spin-qubit shuttling, and leverage their track record of PGI-4 in cryogenic readout, control, multiplexing, and automated qubit tuning. They collaborate with ARQUE Systems, another Jülich/RWTH Aachen spin-off [3189].

Kelvin Quantum

UK, 2024

	DC pulses	LO	AWG	DAC or ADC	I/Q mixers	I/Q demod	readout parametric amplification	readout ADC	readout signal analysis	temp	power qubit
cryo-CMOS											
Google - Bardin [3174] 2019			for X and Y gates	yes	yes					3 K	2 mW
Microsoft/Sydney/ Purdue [3175], FD-SOI 28 nm, 2019	yes	yes	only external signal routing to qubit							100 mK	N/A, low power
CEA List/Leti [3159] FD-SOI 28 nm 2020	yes	yes					yes TIA amplification			110 mK	295 μW
QuTech & Intel [3176] FinFET 22 nm 2020			yes, 8-10 bits	yes	yes						12 mW
HorseRidge 2 [3144] FinFET 22 nm, Intel 2021	yes		yes, 11-bit amplitude, 16,384-sample memory	yes	yes	yes	only LNA between paramp and HEMT	yes		4 K	27 mW (to check)
Pando Tree [3147] Intel, 2024	signals demux			signals demux						10-20 mK	N/A
EPFL [3177], CMOS 40 nm, 2021						yes	time and frequency domain readout signal multiplexing			50 mK	N/A
POSTECH [3148] Korea CMOS 40 nm 2022		2	yes, 4 bits	yes, 4 bits	yes	yes	LNA	yes		3.5 K	15 mW
IBM [3149], FinFET 14 nm, 2022			yes		yes					3.5 K	23 mW
IBM [3178], FinFET 14 nm 2023			yes (adds two-qubit cross resonance gate)		yes					4 K	23 mW
Hitachi & Kobe Univ. [3179] CMOS 40 nm, 2025	yes, gate biasing			11-bit DAC & ADC				environ-ment monitor-ing		DAC, 100 mK (ADC)	5.8 μW (DAC), 35 μW (ADC)
Hitachi [1437, 3180] 2025-2026	mK switch matrix (bridge chip)		from DC levels and low-pass filters	yes, at 4 K						4 K & mK	
SFQ (single flux quantum)											
SEEQC, SFQ 2019 [3181] **DigiQ**, USC, Chicago, Nvidia 2022 (*) [3182]	yes		replaced by series of single amplitude pulses				yes			3 K/600 mK (SFQ copro) & 20 mK (DQM)	0.24 mW (*)
IBM QEC [3161], SFQ, 2022									partial surface code QEC	4 K	10 μW to 500 μW per logical qubit
SEEQC, Maryland University [3183], 2023											passive
AIST & NEC ASFQ [3184] June 2024			multitone signals ADC demultiplexing								81.8 pW per qubit
SEEQC [3185] March 2025	ext. clock signal		full single and two qubit drive with SFQ pulses		not needed	not needed	only with HEMT at 4 K	ext.	ext.	15 mK	3.25 nW per qubit

Table 14: Compilation of various cryo-chips developed so far, with control functions on the left and readout functions on the right. Green cells flag an on-chip function, light green a partial one, grey an absent or externally provided one. 🅭 Olivier Ezratty, 2022-2026.

Kelvin Quantum is a startup specialized in the development of cryo-electronic ASIC components for qubit control and readout ASICs to scale quantum processors. It is spin-out from Glasgow's engineering and semiconductor research groups.

Qifrost

Singapore, 2026

Qifrost is an A*STAR spin-out created by Eric Cao (CEO) and Leonid Krivitsky (CSO) [3190]. It develops QELVIN, a cryo-CMOS control and readout stack

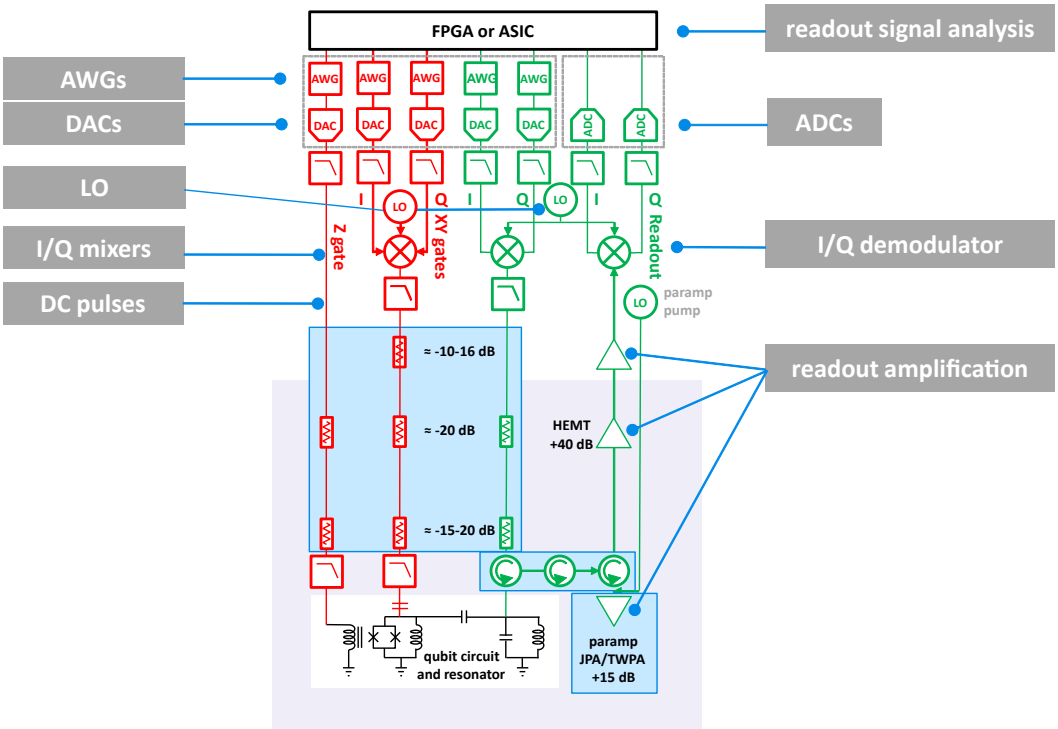


Figure 395: Feature list chosen for the table in Table 14. Olivier Ezratty, 2022.

designed to operate at 4 K, combining 22 nm FD-SOI ASICs with multiplexing that makes wiring scale as $\log(n)$. It uses TSV-based superconducting cryo-packaging. The company has five circuit blocks validated at 4 K, 77 K and 300 K, including a 16-bit DAC/ADC running at 1 to 2 GS/s for 0.2 mW, and targets a budget of about 1 mW per qubit. They target the support of 10^3 qubits between 2027 to 2030 and 10^6 qubits beyond 2030.

Rhonexum

Switzerland, 2025, $1M

Rhonexum is a startup created by Vicente Carbon (CEO) and Hung-Chi Han (CTO, former PhD/post-doc at EPFL in the team of Edoardo Charbon). It is developing cryo-CMOS chips design tools with SPICE-compatible models that capture unique cryogenic transistor behavior. It enables the simulation of circuits down to 4 K. Rhonexum also prototypes a modeling service, called RX-Model, involving transistor compact modeling and parameter extraction.

SemiQon

Finland, 2023, €36M

SemiQon spun out of VTT with Himadri Majumdar (CEO), Mika Prunnila (Chief Research Officer), Janne Lehtinen (CSO) and Markku Kainlauri (Fabrication lead). The company is based at the Micronova research facility for nano- and microtechnology located in Espoo Finland. They were initially planning to create silicon qubit chips, with the goal to support a million qubits with ultra-low charge noise quantum dots operating at 1 K and driven by some cryo-CMOS control electronics built on the same chip as the quantum dots [3154]. Their first prototype wafer presented in April 2023 contained 32 QPUs with 48 qubits and its CMOS embedded multiplexers and amplifiers control electronics (Figure 396).

The company has a fast 4-months design-to-test chip cycle thanks to using a research fab next door to their office run by their own operators and to using 150 mm wafers with only 11 layers [3191]. The future Quantinova fab in Espoo will support 300 mm wafers and is to be funded by the EU CHIPS Act. They worked jointly with Dominik Zumbühl of the University of Basel in Switzerland, who works on SiGe hole-spin qubits [3192], and with Natalia Ares from Oxford University and QuantrolOx.

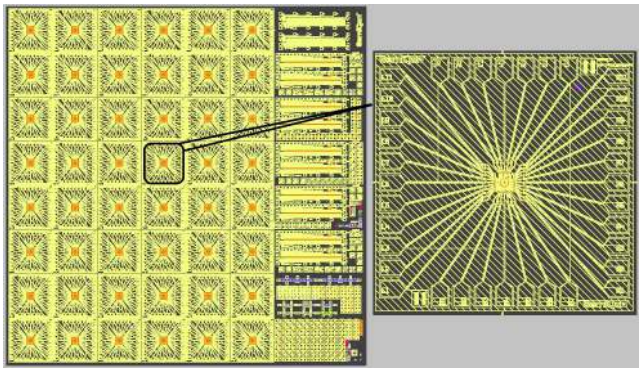


Figure 396: SemiQon first chip prototype sampled in April 2023. Each square is a quantum dot qubit. The circuits on the right are the cryo-CMOS control signals multiplexer and amplifiers. Source: SemiQon web site. 2023.

In 2026, the company made a pivot out of the silicon qubit domain and decided to focus entirely on building cryo-CMOS components driving solid-state qubits, using an energy efficient implementation of FD-SOI MOSFET [3193].

2.2.3 Superconducting electronics

The other option for qubit control and readout at low temperature is to rely on superconducting logic based on Josephson junctions [3194, 3195]. The most common one is SFQ, for "single flux quantum", RSFQ for "rapid SFQ", and RQL for "Reciprocal Quantum Logic".

SFQ-related superconducting logic families can be distinguished by their clocking and bias schemes. Reciprocal Quantum Logic (RQL) and Adiabatic Quantum Flux Parametron (AQFP) use AC or multiphase clock/bias schemes [3196], while conventional RSFQ and its ERSFQ/eSFQ derivatives use DC bias distribution. Conventional RSFQ can operate at very high clock rates, but its resistive DC bias network causes substantial static dissipation. ERSFQ and eSFQ were introduced specifically to suppress this static bias dissipation, while RQL and AQFP make different trade-offs in clock distribution, speed and adiabaticity [3163].

Their potential benefit is very low switching energy cost for some functions, together with native cryogenic operation and the possibility of simplifying wiring inside the cryostat. Reported energy advantages over CMOS can reach orders of magnitude for particular logic operations and assumptions [3197]. The economic pressure from cryogenic cabling is nevertheless substantial in architectures that scale linearly with qubit count.

The eSFQ variant can potentially be much more energy-efficient than cryo-CMOS for selected digital functions [3198]. However, superconducting control logic has important shortcomings. SFQ switching can generate quasiparticles, broadband spectral content and electromagnetic back-action that must be isolated from the qubits [3199, 3200]. In direct SFQ qubit control, shaped microwave pulses are replaced by trains of quantized voltage pulses with picosecond-scale duration, which creates its own pulse-sequence synthesis and filtering overhead (Figure 397). Josephson-junction density, biasing, clocking and cryogenic memory are also system constraints. SFQ logic can store data using superconducting loops, latches, shift registers and dedicated memory cells, but dense, scalable random-access memory remains a major weakness relative to CMOS [3201]. In D-Wave annealers, superconducting control circuits generate programmable biases and readout signals close to the qubit circuitry.

SFQ control electronics requires careful spectral filtering and isolation because picosecond switching pulses contain broadband harmonics and can generate back-action on nearby qubits. Readout-oriented SFQ circuits can move digitization and processing closer to the quantum chip, but they are not exempt from these coupling, quasiparticle and thermal constraints. The relative advantage of SFQ for drive versus readout depends on their implementation specifics.

Many cryogenic memory solutions are investigated but are still in the making: cryogenic spintronics, magnetic tunnel junction (MTJ) [3203], RQL (reciprocal quantum logic) [3204], SQUID-based, hybrid Josephson–CMOS, JMRAM and OST-MRAM memories and even classical SRAM [3205]. We pass on the whereabouts of these various technologies [3206].

There are many interconnected research fields here, and SFQ-based qubit-drive logic is often a by-product of broader research into superconducting digital logic.

Since the 1970s, there were many ups and downs with research in using superconducting electronics to override the apparent limitations of Moore's law with classical semiconductors. Also, superconducting electronics have other use cases like with single photon detection, magnetism sensing with SQUIDs and analog amplifiers working at the quantum limits (JPAs, SPMs, TWPAs).

Qubit readout function can also be implemented with SFQ with readout signal generated through a JPM amplifier [3207, 3208] and converted with ADCs [3209, 3210]. Tone signal generation can also be implemented in SFQ logic [1132, 3211].

Still, the SFQ variants are not the only option to implement superconducting control electronics. You could also potentially do that with InAs-on-insulator (InAsOI) and aluminum on GaAs wafers, implementing JJs and gate-tunable JJs, aka Josephson Field Effect Transistors (JoFETs) which are developed in Italy [3212, 3213] and also at VTT in Finland [3214].

IBM studied classical electronics based on the Josephson junction from the 1960s to 1983, using lead and then lead/niobium. The technology was only supported by IBM and could not compete with CMOS processors, drive by Moore's law and the whole semiconductor industry, particularly with Intel. Japan's MITI had also launched a superconducting computing initiative throughout the 1980s leading to a 4-bit machine using 1 Kbits of RAM. The Bell labs also worked on niobium/aluminum oxide Josephson junctions.

Hypres. Then, the invention of the more efficient and energy efficient RSFQ in USSR in 1985 led to its transfer to the USA via its coinventor Oleg Mukhanov when he joined Hypres in 1991. It led to a short lived superconducting supercomputing project (1997-2001).

Starting in the early 2000s, attention then turned to superconducting qubits with investments throughout the world (USA, France, Japan, ...) leading to major developments from IBM, Google and others. Hypres did use superconducting electronics for non-quantum use cases, particularly in the defense industry and with radars, and quantum sensing using SQUIDs. Interestingly, some of the interest in classical electronics made

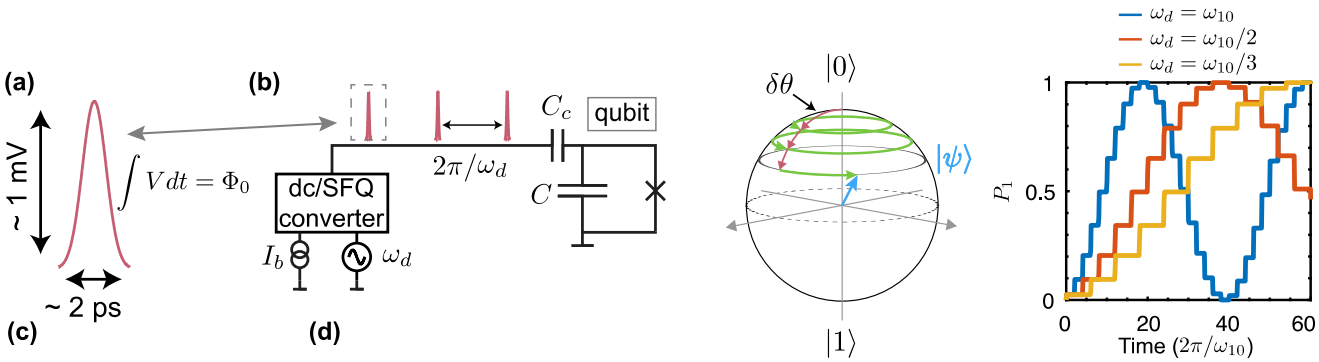


Figure 397: SFQ based wave pulse generation process. Source: [3202].

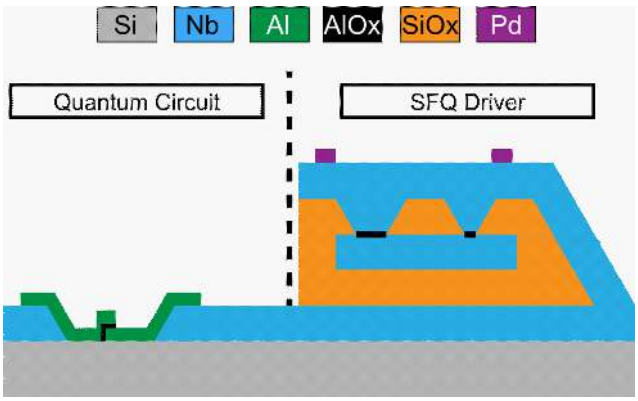


Figure 398: A side-by-side comparison of the stacking of elements in a superconducting qubit (left) and with SFQ logic (right). Source: [3202].

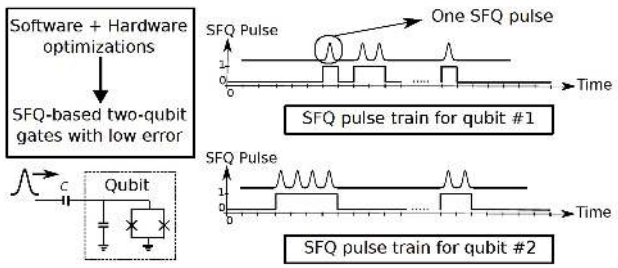


Figure 399: SFQ wave packet optimization developed at the University of Chicago in 2022. Source: [3215].

with SFQ and RSFQ came with quantum computing and the need for energy efficient control electronics.

D-Wave was probably the first to use SFQ electronics in its systems and since its inception. At their beginning, they hired skilled engineers coming from IBM, Stony Brooke University in New York and coming from Stellenbosch University in South Africa having a good experience in superconducting physics and electronics. D-Wave's quantum annealers contain flux superconducting qubits and superconducting SFQ circuits handling signals control generation, control and qubit state readout, and for up to 5,000 qubits. This is a little-known technological feat from D-Wave. It allows them to greatly simplify the wiring that leads to the quantum processor since all their SFQ electronics sits in the same chip handling the qubits. Figure 398 shows how it looks like.

Who else is working with SFQ electronics to control solid state qubits? Let's start with the USA who are the most active here.

- **SEEQC**, a spin-off / split-off from Hypres that we'll detail later and is specialized in superconducting electronics for qubit control.
- **QuamCore**, an Israeli startup that develops its own superconducting qubits and control electronics.
- **Raytheon BBN** (USA) is investigating the usage of SFQ systems and a mix of SFQ and spintronics for controlling qubits [3216]. They have a wide-ranging partnership with IBM and some IBM researchers worked with BBN on SFQ back in 2018.
- **University of Wisconsin-Madison** has a Department of Physics run by Robert McDermott that investigates SFQ logic. He pioneered qubit control with trains of SFQ pulses [3198, 3202, 3217, 3218]. They authored the paper with Raytheon BBN on SFQ qubit control mentioned with Raytheon above. They are working to fix various SFQ problems like quasiparticles qubit poisoning and the antenna effect in the qubit chip [3199].
- **MIT Lincoln Labs** has been working for a while on SFQ logic in the "beyond CMOS" roadmap funded by IARPA as part of the Quantum Enhanced Optimization (QEO) and Logical Qubit (LogiQ) programs [3219, 3220]. In 2017, they developed a 3D Integrated Superconducting Qubit Platform using three layers: the qubit chip, an interposer with through-substate vias and a supporting chip with a routing layer and a TWPA for qubit readout microwave amplification. They are also leveraging their own superconducting cleanroom. The Lincoln Lab is even providing many

labs across the world with their own custom TWPA and for free.

- **University of Chicago** is also involved in the design of SFQ-based qubit control electronics. In 2022, they demonstrated low-error two-qubit operations using SFQ pulses drive working with fluxonium superconducting qubits [3215] (Figure 399). They also led the DigiQ project launched by the NSF. It was funded as part of the Enabling Practical-scale Quantum Computation (EPiQC). The project is run with Amazon, Nvidia, Super.tech and USC. The qubits are driven by series of small SFS pulses, not by arbitrary waveformed pulses. Theoretically, SFQ logic could still create these waveforms thanks to clock speed exceeding 100 GHz. It could create waveforms with basebands of 4 to 25 GHz. But this would require superconducting DACs and ADCs which happen to need resistances, thus being irreversible and dissipative, creating some thermal constraints [3221].

- **Northrop Grumman** is also working on SFQ for qubit controls and even patented one related solution back in 2008 [3222]. They also developed RQL techniques. At the 2026 APS Global Physics Summit in Denver, Tony Przybysz from Northrop Grumman presented a H, S, and CZ qubit gate set and readout controlled by RQL chips sitting on top of the qubits. It consumes ≈100 pW at a 1 GHz clock and contains 1.5 million Josephson junctions. The chip controlled flux superconducting qubits and obtained 99.9% single-qubit and 97% two-qubit fidelities on 282 qubits. Related papers were published in September 2026 [3223, 3224]. Northrop Grumman is also working on cryo-CMOS DAC component for qubit readout operating between 600 mK and 4 K [3225].

- **IBM** together with the Universities of Chicago and Southern California, and Super.tech (from ColdQuanta) presented in August 2022 the development of an SFQ-based cryogenic circuit to implement part of the logic of the most common errors in quantum error correction for surface codes [3226]. The decoder could support between 2000 and 100,000 logical qubits depending on the code distance.

And in the rest of the world:

- **China** launched a €200M project on SFQ electronics. The Shanghai Institute of Microsystem and Information Technology's (SIMIT) Laboratory of Superconducting Electronics is studying SQUIDs (Superconducting quantum interference device used in sensing), SNSPD (superconducting nanowire single-photon detectors) and Superconducting large scale integrated circuits with a 50 persons team. They ambition to create a 64 bits SFQ-based microprocessor. They have their own cleanroom. A side project could well become SFQ-based qubit control chips. Other academic teams in Shanghai published in 2026 some work on a SFQ-based DAC driving fluxonium qubits [3227] and on a full SFQ controller for transmon qubits obtaining 99.9% Clifford gate fidelities [3228].

- **Japan** has a very active group in SFQ, the group of Nobuyuki Yoshikawa from Yokohama National University. They are working in the field of superconducting electronics, SFQ and adiabatic circuits mostly as "beyond than Moore" solutions [3229]. He participated in the development of AQFP (Adiabatic Quantum-Flux-Parametron), an energy-efficient superconducting logic element [3230] and started to publish work on its implementation for qubit control in 2023 [3231]. Their ASFQ circuit produced multi-tone microwave signals for qubit control with an extremely small power dissipation of 81.8 pW per qubit, plus signal multiplexing. A single LO line could transmit 4000 microwave tones, assuming a bandwidth of 2 GHz. Multiplexing was done at room temperature. The chip is doing signals demux from analog to digital [3232]. Jaw-Shen Tsai's team at RIKEN is also working on SFQ control electronics and developed a digital frequency divider in 2025 [3233].

  RIKEN also has a team working on using SFQs [3234, 3235]. They developed the C3-VQA, an SFQ-based control circuit operating at 4 K to control not only superconducting qubits, but also, in a customized way to optimize the execution of NISQ variational quantum algorithms like VQE and QAOA, with consolidating the results from successive circuit shots [3236].

- **Canada** has a team spread over Sherbrooke, the University of Waterloo and 1Qbit working on improving SFQ qubit drive [3237, 3238].

- **Germany** has a couple labs and fabs looking at superconducting electronics and their potential usage in qubit control. You can count with Per J. Liebermann and Frank K. Wilhelm from Saarland University who work on improving qubit fidelities with varying the time distance between SFQ pulses in the train using control theory and (classical) genetic algorithms [3239]. The Leibniz-IPHT in Jena, Thuringia, has a cleanroom that works, among other things, on producing RSFQ circuits and SQUIDs for quantum sensing. Leibniz-IPHT is coordinating the German project HIQuP dealing specifically with superconducting qubit control electronics and partnering with IQM Germany and Supracon AG, itself a spin-out of the Leibnitz-IPHT that is specialized in SQUID based magnetometers. The PTB has also investigated SFQ circuits in the past [3240]. There was also the EU project RSFQubit from 2004 to 2007, involving many German players and coordinated by Chalmers University, Sweden, with a funding of €2.6M.

- **France** with Pascal Febvre from CNRS Chambéry working on a project funded by ODNI and DARPA [3241].

- **Finland** also conducts some research in SFQ logic at VTT under the leadership of Matteo Cherchi [3242]. Their aCryComm project develops converters and input/outputs for simple SFQ processors [3084]. This work could also lead to some potential collaboration with IQM.

- **Russia** has some researchers working on superconducting electronics and even on SFQ qubit drive electronics, particularly at Lomonosov Moscow State University and Lobachevsky State University of Nizhny Novgorod [3243–3247].

On top of SFQ, **SQUIDs** are another superconducting electronics that is proposed to play a similar role in the control of qubits. It is mainly proposed by researchers in China. First for qubit drive and readout, using microwave photons generation from a vacuum with a SQUID-embedded coplanar waveguide (rf-SQUIDs CPW) [3248]. This creates a lot of questions, on how the pulses are calibrated in phase and photon number, how their chip is connected to the qubit chip (required distance, side effects, TSVs (through-silicon-via) if flip-chip bonding is used, signal demultiplexing …). Second, for handling tunable couplers, which can also reduce the number of qubit control lines [3249].

SEEQC

USA, 2017, $64.2M

Company. SEEQC was created initially as a subsidiary of Hypres, an American company specialized in the creation of superconducting electronics, by John Levy, Matthew Hutchings and Oleg Mukhanov. By setting up offices in Milan and the UK, the startup found a way to secure European funding for its research. Otherwise they collaborate with Robert McDermott's team at the University of Wisconsin and the Syracuse team in upstate New York. Its parent company Hypres (1983, USA, $50K) is a long-time specialist in superconducting electronic circuits. It was created by Sadeg Faris, a Libyan who invented the quiteron at IBM, a superconducting transistor. He created Hypres the same year IBM pulled the plug on superconducting electronics and used IBM patents under license.

SEEQC has been the only superconducting electronics company for three decades and lived out of SBIR funding and some defense business, like with radars and spectrum analysis. They are a mix of nationalities with Indians, Russians, and a Lebanese. Hypres split in two in 2020. The RF business did stay at Hypres working mostly for the DoD, and SEEQC specialized in SFQ based qubit drive while keeping Hypres's 230 m^2 cleanroom based in Elmsford, New York State near White Plains. It uses an aluminum-niobium 9-layer process. Hypres now relies on the MIT Lincoln Labs which is itself funded by the DoD. But SEEQC also manufactures superconducting chips for the DoE, NASA and DoD as well as other commercial and academic teams.

In January 2026, SEEQC announced it would make a SPAC-based IPO with an expected value of $1B and an incremental funding of $65M.

Technology. SEEQC stands for "Superconducting Energy Efficient Quantum Computing". It focuses on the creation of superconducting circuits completed with spintronic technology memories [3250]. It also worked on TWPAs [3251]. The company was initially funded under IARPA's C3 project launched in 2016. Then SEEQC created a lab at Federico II University of Naples, Italy, and the UK, mostly to capture EU/UK public funding.

SEEQC's architecture was initially based on two chips: a classical SFQ control chip and the SFQuClass DQM, both using Josephson junctions in SFQ superconducting circuits. The first chip runs at 3 K or as low as 600 mK and uses an energy efficient ERSFQ or eSFQ variant of RSFQ logic. It removes a lot of wiring clutter thanks to digital control signal multiplexing (Figure 400). SFQ qubit drive is not using microwave pulses but SFQ square pulses. As a result, there is much less crosstalk between qubit drive. But this signal must be filtered, which generates some thermal dissipation. It controls the DQM and handles error corrections without requiring an external classical computer. The SFQuClass DQM (Digital Quantum Management) includes the microwave generators used to drive the qubits (with DACs, digital-to-analog signal converters) and for qubit readout (with ADCs, analog to digital microwave signal converters) (Figure 400).

SEEQC quotes a power drain of 0.0002 mW per qubit, against over 20 mW per qubit for some cryo-CMOS designs. Such comparisons are only meaningful when the two implementations cover the same set of electronic functions at the same stage, which is rarely the case. The loop between the SFQ coprocessor and the DQM also reduces the latency of qubit control and is particularly interesting for implementing error correction codes. When we can generate qubit control signals inside the cryostat, it still must be exchanged both ways digitally with the outside of the cryostat. This can be done through signals multiplexed on copper, fiber optics, or even, it is under study, radio waves at very high frequencies (in THz). It also helps maximize thermal and vacuum insulation with the outside [3202, 3252–3254]. An optical fiber has the advantage of being made of glass, which does not generate thermal expansion and is a weak heat conductor.

SEEQC has scalability plans that will require using a growing number of wires with the number of qubits, with a better "Rent's rule" than with classical control. Rent's rule computes the math of connections needed to control an electronic system and how it scales with size [3255, 3256].

In April 2023, SEEQC demonstrated an SFQ-based QPU in its laboratory in Naples, Italy, System Red with a 5 superconducting qubits chip from QuantWare, quite fast two-qubit gates at 39 ns, but with a paltry 98.4%

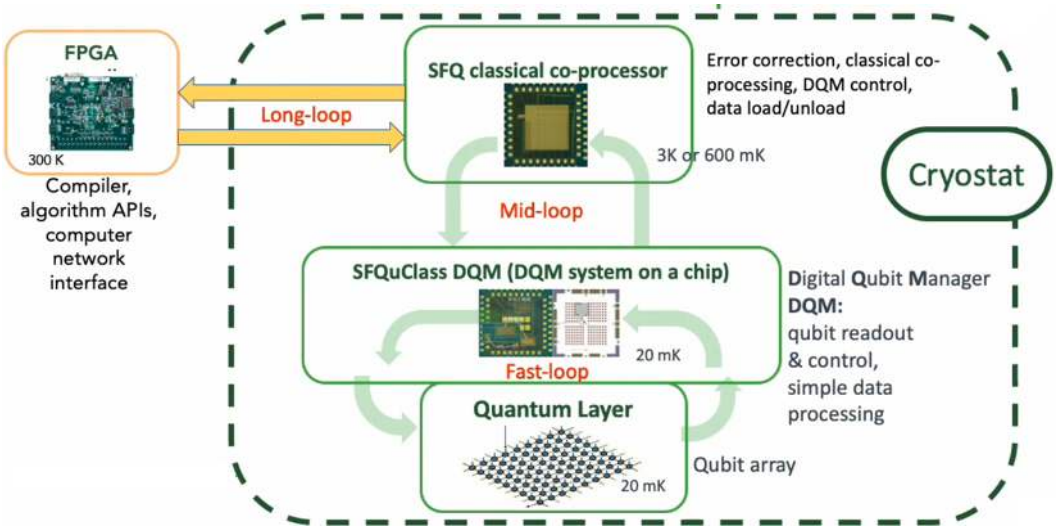


Figure 400: SEEQC overall architecture with a classical coprocessor running at 3 K / 600 mK and the DQM located close to the qubit chip at 20 mK. Source: SEEQC.

two-qubit gate fidelity. It assembled QuantWare's chip and SEEQC's SFQ chip for qubit drive as well as digital demultiplexing features. The SFQ features were not complete though.

"Quantum" Rent's Rule			
	Qubit Control Wiring Overhead		
Qubit Count	G	seeqc	Application
2	4	3	Prototype
10	20	3	Prototype
100	200	31	Prototype
1k	2,000	76	Optimization / chemistry
10k	n/a	330	Optimization / chemistry
100k	n/a	~1,600	Big data / ML
1m	n/a	~6,000	Encryption

Figure 401: How many wires are necessary for controlling qubits comparing Google's Sycamore system and SEEQC's solution. Source: SEEQC.

In 2024, along with QuantWare and the University of Glasgow, they created multi tone digital signals, using complex pulse train sequences based on a Circular Shift Register (CSR) and a comb filter stage [3257]. In 2025, they implemented the drive of single and two-qubit gates with respectively 99% and 97.4-99.5% fidelities, all this at qubit temperature. These were not stellar but showed real progress in the SFQ realm [3185].

SEEQC also tested a simple signal routing SFQ chip that was flip chip bonded with a fluxonium qubits chip from Maryland University and EPFL [3258]. At this point, they use a single cable to control four RF signals with future version controlling 16 signals. Future system iteration will support SFQ based qubit readout which in the first edition seems implemented classically at room temperature [3259].

UK projects. It fared better with the UK than with the EU. They got grants from Innovate UK's Industrial Challenge Strategy Fund as part of four consortiums.

- The first, announced in April 2020, totaling £7M, was led by OQC and included Oxford Instruments, Kelvin Nanotechnology, University of Glasgow (Martin Weides' team) and the Royal Holloway University of London, to create a superconducting qubit computer. This may be behind the installation of a prototype system at the NQCC in March 2025.

- The second, launched in September 2021, was NISQ.OS, totaling £5.363M, is focused on building an operating system and an hardware abstraction layer is led by Riverlane and includes, Hitachi Europe, Universal Quantum, Duality Quantum Photonics, Oxford Ionics, OQC, arm and the UK National Physical Laboratory, another SEEQC partner in the UK. SEEQC and Riverlane announced in June 2021 that they had integrated Riverlane's operating system Deltaflow.OS with SEEQC's qubit driving components.

- The third consortium was launched in November 2021 in partnership with Merck who is also an investor in SEEQC as well as with Riverlane, Oxford Instruments, the University of Oxford and Medicines Discovery Catapult, with a total funding of £6.85M grant from Innovate UK's Industrial Strategy Challenge Fund (ISCF) to build a "*commercially scalable application-specific quantum computer designed to tackle prohibitively high costs within pharmaceutical drug development*" (aka QuPharma project). A bit like IQM's strategy, SEEQC is to create "*an application-specific quantum computer*" to simulate quantum chemistry, an idea that I found a bit questionable. The announcement didn't mention either a number of qubit or expected fidelities, but the project was due for completion "*in 18 months*". We're far from it now.

- The fourth consortium was led by sureCore, with £6.5M to support the integration of SEEQC's tech-

nology with cryo-CMOS components for qubit controls. SEEQC's role is to "*determine what IP blocks the project will need to create for the Cryo-CMOS chips*". Other partners are Oxford Instruments, SemiWise, Synopsys, Universal Quantum and the University of Glasgow.

Partnerships. In December 2021, SEEQC announced a partnership with QuantWare (the Netherlands) for the development of a QPU containing QuantWare's superconducting qubits and SEEQC's SFQ cryogenic control electronics. It adds another superconducting vendor to SEEQC's partners, on top of OQC (UK). The difference here is that QuantWare will embed SEEQC's technology in its QPU in multi-chip modules. QuantWare chips were used in the 5-qubit SEEQC prototype released in Italy in 2024. In September 2023, SeeQC and Nvidia announced a partnership for the integration of SEEQC's chip architecture with Nvidia GH200 Grace Hopper GPUs. It would enable SFQ on-chip, real-time quantum error correction. The public material does not specify the interconnect between the Nvidia and SEEQC chips; confirmation is required. As a result, SEEQC and Nvidia announced in 2025 the integration of their technology in a prototype system [3260].

Roadmap. SEEQC long-term roadmap is to run all SFQ functions at qubit temperatures up to handling quantum error correction. Their SFQ chips are labelled with color names (Red, Orange, Yellow, Green). The ultimate Green chip planned after 2028 should handle error correction and syndrome error decoding, enabling run-time QEC. The company expects to package a whole 100K (silicon based) qubits QPU in a half rack and a Maybell dilution refrigerator. If it worked, SEEQC superconducting electronics would be a real game changer. It would drastically reduce the cost and price of large scale solid-state qubit QPUs, reduce their energy footprint and make it more affordable for the market.

S-Transistors

Finland, 2026, €2.6M

S-Transistors is a VTT spinout created by Heorhii Bohuslavskyi (CEO), Andrey Generalov (CTO) and Markus Lehtisalo which develops integrated circuits based on graphene Josephson field-effect transistors made on 150 mm wafers [3261]. Its first product is a cryogenic superconducting multiplexer, with commercial multiplexers and demultiplexers planned for 2027 and a mk quantum motherboard as a long-term goal. It positions itself between cryo-CMOS (SemiQon) and SFQ logic (SEEQC), combining transistor-style gate control with near-zero dissipation.

2.2.4 Circulators and isolators

Circulators and isolators are used in the qubit-readout signal chain at the lowest stage of a cryostat.

The generic role of an N-port circulator is to send the microwave from port i to port $i+1$ in a directional *aka* non-reciprocal way [3262]. The signal from port $i+1$ cannot be sent back to port i, or is sent back with strong attenuation (Figure 402). It is used to convey the readout microwave from their AWG/DAC source to the qubit resonator and its response microwave to the first amplification stage. The amplified microwave is sent upwards to the next amplification stage, without being sent back to the resonator. There are settings variations based on using between one and four circulators to improve the isolation between components in the readout signal chain.

The reverse isolation of a single cryogenic ferrite component is finite, often of order 15-25 dB over its useful band. Cascading isolators or circulators can provide several tens of decibels of reverse isolation. The required isolation is set by the complete back-action and noise budget of the measurement chain, including amplifier reverse noise, loss and thermal occupations. Circulators and isolators protect the qubit and readout resonator from reverse-propagating noise and amplifier back-action. This improves readout fidelity and qubit lifetime.

Isolators are similar symmetry breaking devices, but with only two connectors they enable a one-way microwave circulation. Conceptually, these are like "microwave diodes", letting microwaves be transmitted in only one direction [3263].

Traditional microwave circulators use magnetically biased ferrites whose gyromagnetic, non-reciprocal permeability breaks time-reversal symmetry. Depending on the device geometry, the operation can be described through non-reciprocal phase shifts, mode splitting and interference. Faraday rotation is one related ferrite effect [3264]. Their permanent magnetic bias and physical size make integration directly beside magnetic-field-sensitive qubits difficult. Frequency-multiplexed readout allows one circulator or isolator chain to be shared by several resonators [3265].

Readout systems commonly multiplex several qubits, often in the 4-16 range, while larger factors are possible with sufficient resonator spacing, amplifier bandwidth, dynamic range and digital processing. A simple 2 GHz allocation with 10 MHz channel spacing contains 200 nominal frequency slots before guard bands and collision constraints, and this division is only an idealized upper bound. In practice the usable number is much smaller because resonator linewidths, fabrication spread, crosstalk, amplifier intermodulation and the required readout pulse duration all impose constraints. Shorter readout pulses have broader spectra, which increases these frequency-packing constraints, and also, can increase qubit leakage out of the computational space.

Existing ferrite circulators used with superconducting qubits are relatively bulky components, often centimeters in size (Figure 403). The free-space wavelength

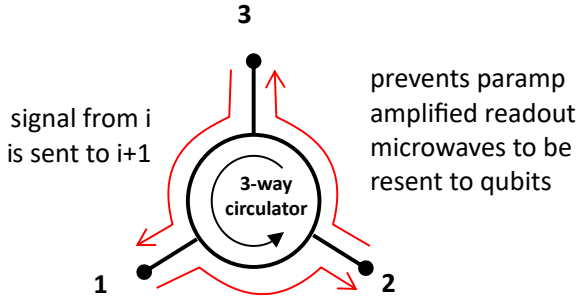


Figure 402: Principle of operation of a circulator which circulates microwaves in a one-way fashion.

Figure 403: A typical commercial bulky circulator. QuinStar Technology.

at 6 GHz is about 5 cm, but component size is set by the guided wavelength, ferrite resonator geometry, magnetic bias structure, bandwidth and packaging rather. Together with cabling, filters and attenuators, these components occupy significant cryostat volume and motivate integrated non-reciprocal alternatives.

Ideal circulators would fit into the qubit chips and use compatible (superconducting) circuits, have a high protection (in the 20 dB region), a large and controllable bandwidth (between 500 MHz and up to 2 GHz, to enable qubit readout multiplexing) and low power dissipation at their operating temperature if they are active, whether the 15 mK or the 4 K stage. They'd also be combined with the first stage quantum-limit low-noise amplifier like a TWPA.

These new types of circulators can be segmented by their underlying physical process. I will simplify this and have, first, classical electronics systems:

- **Hall effect circulators** as developed by David DiVincenzo in Germany and whose size is not constrained by the readout microwave wavelength [3266, 3267].
- **LC based cryo-CMOS circulators** as prototyped at TU Delft. It uses resonant LC circuits level combining inductance (L) and capacitors (C). The circuit provides an 18 dB isolation and consumes a total of 10.5 mW. It runs at 4.2 K and not at the lowest 15 mK. It was tested with a 40 nm node with an active area of 0.45 mm^2 in an experimental 1.5 mm wide square circuit [3268].

And then, various superconducting circuits using Josephson junctions like:

- **Interferometric and parametric Josephson circulators**, developed at IBM [3269–3271], RIKEN [3272], Google AI (as shown in Figure 405) [85] and in France [3273], with the advantage of very low power dissipation.
- **Superconducting quantum tunnelling capacitors**, developed by Clemens Mueller at ETH Zurich and the University of Queensland. This circulator uses a small superconducting capacitor, using the quantum tunnelling of the magnetic flux around it, allowing a flow of microwave energy in one direction [3274]. These are passive systems or can be controlled with just some DC (direct current) input, as shown in Figure 404 [3275]. This led to the creation of Analog Quantum Circuits (Australia). These could be potentially directly implemented in superconducting qubit chips.
- **Annular long Josephson junction** was a proposal for an alternative on-chip DC-controlled circulator from Analog Quantum Circuits in 2025, in which a DC-bias-driven train of moving fluxons breaks time-reversal symmetry through the effective synthetic motion of the propagation medium [3276]. It was a theoretical proposal without experimental validation.
- **On-chip microwave circulators** with a wide tunable frequency, developed in 2017 at the University of Colorado in Boulder [3277–3279], a variation with SQUIDs superconducting components.
- **Josephson based quantum diodes**, also named superconducting diodes, are being developed using similar designs [3280–3282], and also with Al-InAs nanowires [3283].

While there are many such prototype solutions, and we've not covered them all, it seems they have not yet reached the commercial stage at this point, although some have use cases beyond qubit control like in the telecom and radar markets.

Analog Quantum Circuits

Australia, 2022, $2M

Analog Quantum Circuits is a company created by Tom Stace (CEO) and Arkady Fedorov (CSO) that is developing on-chip circulators for solid state qubits, based on the work of Fedorov [3284]. They also have plans to develop other components like TWPAs and attenuators.

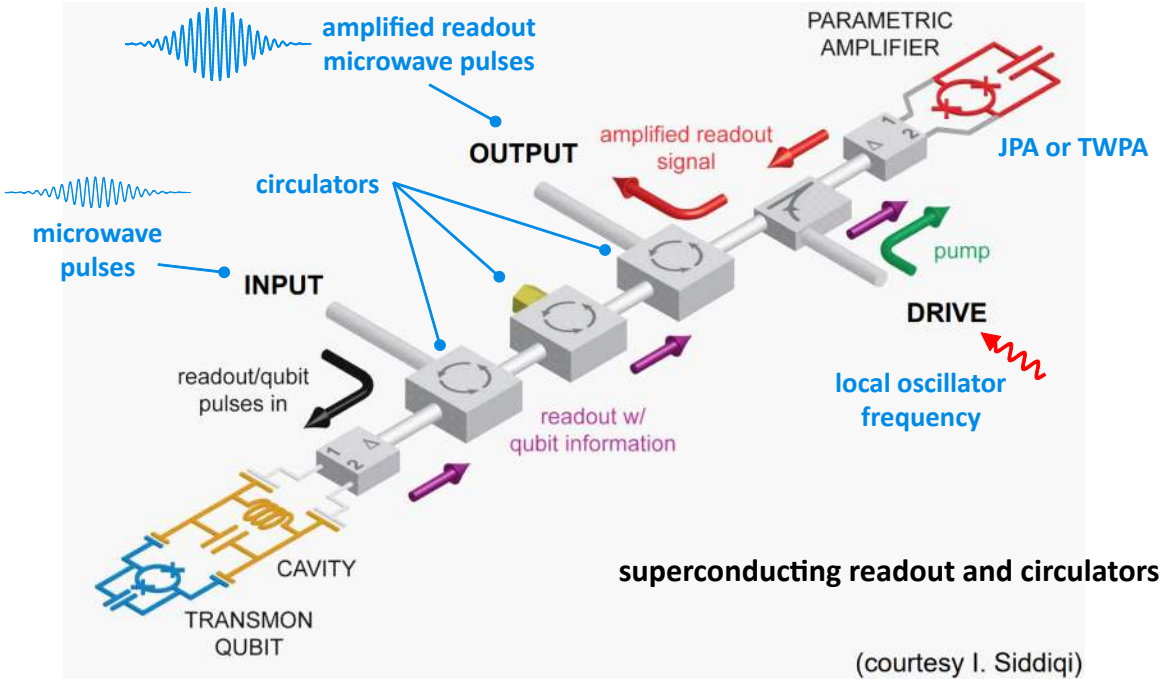


Figure 404: Several circulators are actually used for each set of qubit controlled through frequency multiplexing. Source: Irfan Siddiqi.

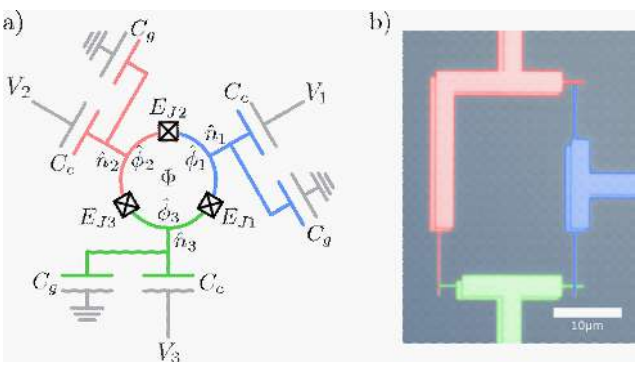


Figure 405: A prototype passive superconducting circulator that could potentially be integrated in a superconducting qubit chip. Source: [3275].

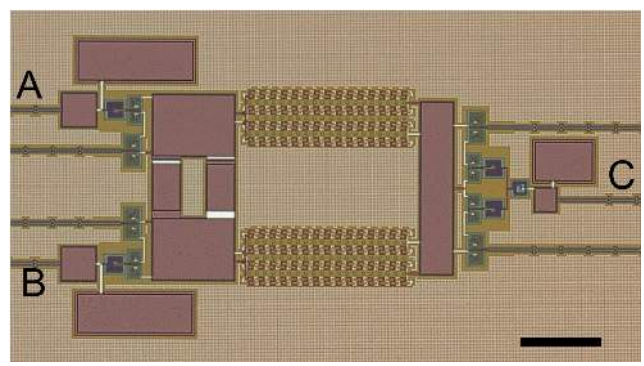


Figure 406: A parametric Josephson junctions based circulator proposed by Google. Source: [85].

2.2.5 Amplifiers

Analog superconducting-qubit readout signals are usually amplified before digitization and digital classification. A common chain uses a near-quantum-limited parametric amplifier at the millikelvin stage, followed by a cryogenic HEMT LNA near 4 K and one or more conventional room-temperature RF amplifier stages. Typical gains are of order 15-25 dB for the parametric stage and 30-40 dB for a cryogenic HEMT, with additional room-temperature gain chosen to match the ADC input range. The exact number of stages and gains are architecture-dependent. The mK parametric amplifier is important because sufficient first-stage gain suppresses the noise contribution of the following, noisier HEMT in the system noise budget.

Two main generations of parametric amplifiers have been used for qubit readout. They are based on exciting and pumping a material with nonlinear polarization using an intense electromagnetic field. A weak microwave signal can then get amplified via the interaction with the medium.

JPAs. The first paramps used for superconducting qubit readout were the JPAs (Josephson Parametric Amplifiers) [3285]). These are simple amplifiers, using one or two Josephson junctions, easy to manufacture, with a good gain of about 15 to 20 dB. A team in Japan reached a gain of 40 dB with a JPA in 2022, at the cost of a narrow bandwidth: at 20 dB of gain that particular device had a bandwidth of 400 kHz [3286]. This gain-bandwidth pair belongs to that device and operating point and does not characterize JPAs in general (Figure 407).

Their main shortcoming is their narrow bandwidth which prevents their implementation with frequency-domain qubit readout multiplexing, where a single amplifier processes a readout signal coming from several chained qubits using different resonant frequencies [3287]. It is due to JPAs being based on cavities. Some variants using Josephson based FET transistors (JoFET) are frequency tunable but have a low bandwidth as well [3288]. In its 2024 processors with its first break-even logical qubits, Google used a Lumped Element Snake Amplifier (LESA), a variation of a JPA [3289]. Wireless JPAs operating at 20 GHz have been prototyped [3290]. They are adapted to superconducting qubits operating at this regime and at a temperature of 200 mK, developed by the University of Chicago [3291]. Higher frequencies and a higher operating temperature may help fit more qubits in a cryostat, but they do not solve the cabling problem on their own. The 3 GHz bandwidth of these wireless JPAs is in fact broad relative to conventional resonant JPAs, while the number of qubits that can share one readout chain still depends on resonator spacing, crosstalk and amplifier linearity.

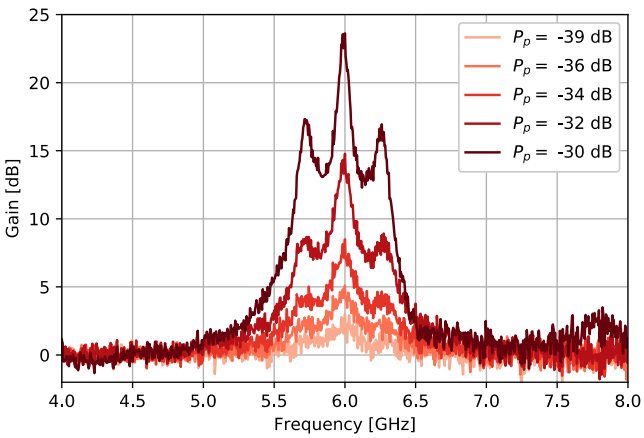


Figure 407: The typical narrow-band response curve of a JPA. It is the gain curve for a JPA as a function of applied pump power in three-wave mixing mode. Source: [3292].

In the commercial domain, **Google** is improving JPAs with their in-house SNIMPA or 'snake impedance matched parametric amplifier' which has a high dynamic range, large bandwidth, high saturation and where the active nonlinear element is implemented with an array of rf-SQUIDs [3293].

TWPAs. Traveling-wave parametric amplification has important precursors in Josephson-junction arrays, including the series-array Josephson parametric amplifier studied by Yurke et al. in 1996 [3294]. A major experimental milestone for broadband superconducting traveling-wave amplification was the kinetic-inductance TWPA demonstrated by Eom et al. in 2012 [3295]. Near-quantum-limited Josephson traveling-wave amplification over gigahertz bandwidths was then demonstrated by Macklin et al. in 2015 [3296].

There are several variations along different lines:

- Regarding the **parametric process**, with three-wave mixing (3WM) using one pump photon yielding one signal photon and one idler residual photon [3251, 3297] and four-wave mixing (4WM) using two pump photons yielding one signal and one idler photon. The pump microwave usually comes from a local oscillator source outside the cryostat. It can generate some phase noise, as characterized by Keysight in 2026 [3298]. A variant is the rf-SQUIDs based TWPAs, operating in the three-wave mixing (3WM) regime and with a large 4 GHz bandwidth, developed in Germany [3299].

- Related to the **superconducting materials**, with either Josephson-junction nonlinearities, often based on aluminum or niobium processes, or nonlinear kinetic inductance in materials such as NbN and NbTiN.

- Then, with **phase-matching** techniques [3300]. Josephson TWPAs use long nonlinear Josephson-junction transmission lines, frequently with hundreds to thousands of junctions, and require engineered dispersion or phase matching. Kinetic-inductance TWPAs, usually abbreviated KI-TWPAs or KITs, use the nonlinear kinetic inductance of a superconducting transmission line and are a distinct device family. "Kerr-reversal" or reverse-Kerr engineering refers to a nonlinear phase-matching strategy [3301]. Floquet-mode TWPAs provide another route to broad bandwidth, low added noise and improved directionality [3302] (Figure 408).

- The integration of other bias circuitry **rf elements** [3303] and, potentially, of isolators and circulators.

Optical traveling-wave parametric amplifiers are analogous nonlinear devices operating, for example, near the 1,550 nm telecom band and are relevant to optical communications and CV-QKD [3304]. They are not superconducting microwave TWPAs used for qubit readout.

TWPAs are used for qubit readout, in high-energy particle physics, radio astronomy and astrophysics [3305], like for the detection of dark matter and in quantum sensing [3306]. Their broader bandwidth could potentially enable up to 10-20 qubit readout multiplexing. TWPAs however generate undesired mixing processes between the different frequency multiplexed tones [3307] and unwanted echo signals, that can be mitigated [3308].

TWPAs other figures of merit are saturation power, dynamic range, gain flatness and added noise. For quantum-limited microwave amplification it is often better to express noise in added quanta rather than only as a noise temperature, since one photon at 6 GHz corresponds to $h\nu/k_B \approx 0.29$ K and half a quantum corresponds to about 0.14 K.

Both JPAs and TWPAs require a coherent microwave pump, although pump frequency and power depend

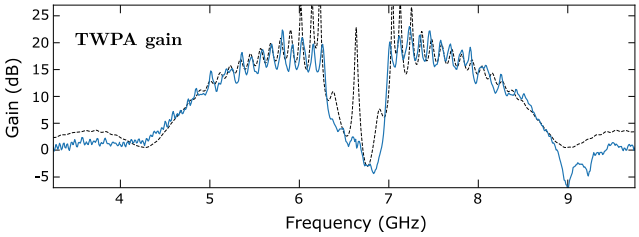


Figure 408: The typical frequency response curve of a TWPA that has over 2 GHz available with a gain superior to 15 dB in two parts, below 6.2 GHz and above 7 GHz. Typical TWPA circuit, with 2000 series of Josephson junction bridges, as described on the right. Source: [3292].

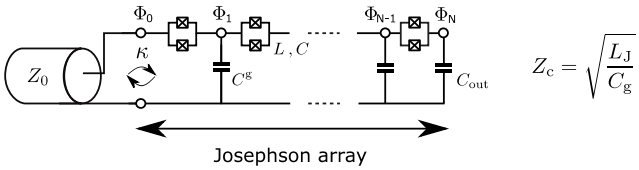


Figure 409: TWPAs are frequently made with a Josephson array. Source: [3292].

strongly on the amplifier design. Pump power must be expressed in dBm or watts, not in dB. For reference, −70 dBm is 0.1 nW and −80 dBm is 0.01 nW at the device input. The room-temperature source power is higher because cable loss, attenuation and couplers reduce the pump before it reaches the millikelvin stage.

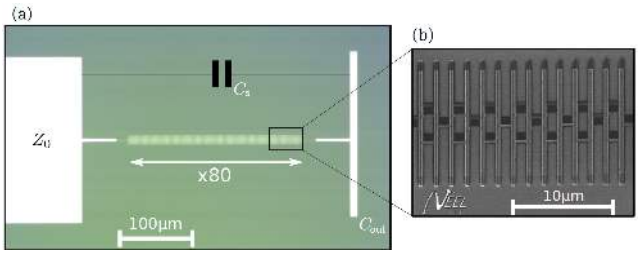


Figure 410: How a TWPA Josephson array is embedded in a circuit. Source: [3292].

Alternative readout techniques. Other qubit readout options are investigated, including:

- **Low-noise cryo-CMOS amplifiers**, prototyped in 2020 by **CEA-Leti** that operates at 10 mK [3309]. In another recent work involving the UK and CEA-Leti in France, quantum-dot-based readout amplification is studied and is adapted to silicon spin qubits. With some improvements, it could reach gains of classical JPAs (15 dB) although on a small bandwidth [3310].
- **KIMPA**, or kinetic-inductance impedance engineered parametric amplifiers are developed at RIKEN by Yasunobu Nakamura's team, which have higher operating temperatures [3311], on top of regular TWPAs [3312].
- **Semiconducting nanowire amplifier** developed in the Netherlands, working at near-quantum-limited performance, with more than 20 dB of gain and a 30 MHz instantaneous bandwidth at that gain, a saturation input power of −120 dBm, magnetic field compatibility up to 500 mT and frequency tunability over a range of 15 MHz [3313]. However, its bandwidth is limited compared to TWPA, making it difficult to multiplex the readout of several qubits with a single cable and amplifier.
- **Double quantum dot (DQD) photodiodes** that achieve a photon-to-electron conversion efficiency of 25% in the microwave domain, still not sufficient for qubit readout [3314].
- **Superconducting amplifier running at up to 1.5 K**, which may be useful for silicon spin qubits, with near-quantum-limited added noise [3315].
- **Nanobolometers** operating in the gigahertz regime could also be of some use here, but more for metrology [3316, 3317].
- **GaAs LNA** amplifiers with microwatt power consumption and operating at millikelvin temperatures [3318].
- **Microwave photon counters** using Josephson Photo Multiplier (JPM) that can be directly embedded in the qubit chip. It does not require low-noise amplification with a JPA or a TWPA, and the cited device reported a readout fidelity above 98% with a 500 ns readout time under its own operating conditions [829]. Microwave photon counters were experimented in Benjamin Huard's lab at ENS Lyon [3319–3321], in Jérôme Estève and Julien Basset's team at LPS in Saclay [3322], and at CEA SPEC in Saclay using a SQUID connected to a coil [3323].
- **Single microwave photon counters** with an operational solution designed by CEA at Saclay in 2022 [3324].
- **Single microwave photon multipliers** with a prototype created in Germany and Canada in 2025 [3325].

Before looking at cryogenic amplification commercial vendors, let's mention the **MIT Lincoln Lab** team from William D. Oliver who has been pioneering TWPAs for a while, and has supplied many laboratories with its own TWPAs since 2015, free of charge, as a research distribution rather than a commercial product (pictured in Figure 411). His team developed a Floquet-mode TWPA in 2025, achieving nearly quantum-limited noise performance, low dissipation, and broadband operation [3326].

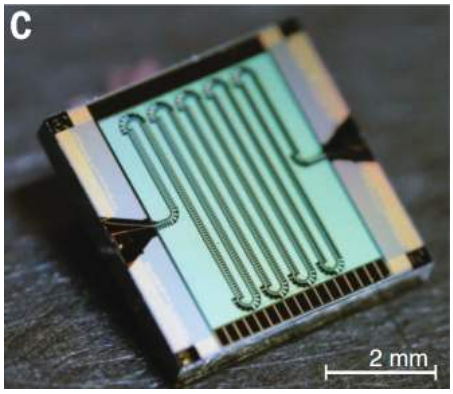


Figure 411: An MIT Lincoln lab TWPA. Source: [3296].

In Finland, **VTT** manufactured Josephson TWPAs containing large junction arrays. In Sweden, **Chalmers University** researchers are working on optimized three-wave-mixing TWPAs [3327].

In Italy, various labs launched DARTWARS, for designing a TWPA with very large bandwidth covering 5 to 10 GHz with low noise temperature of 600 mK. It will use two techniques with Josephson junctions (JTWPAs) and kinetic inductances (KITWPAs) [3328, 3329]. There was also a 4-year EU TWPA project named **ParaWave**, run by German, Italian and British partners from 2018 to 2021 [3330].

On the QPU vendors side, **IBM** and **Rigetti** developed their own TWPAs while **IQM** uses TWPAs from VTT, now commercialized by Arctic Instruments.

HEMT amplifiers. At the 4 K stage, a second microwave readout amplifier is typically used. It is usually a HEMT (high-electron-mobility transistor). A representative cryogenic HEMT provides about 40 dB of gain with a bandwidth greater than 6 GHz and a high dynamic range, for the inbound microwave readout signal coming from the parametric amplifier at the millikelvin stage, which has already applied 15 to 20 dB of low-noise gain at or near the quantum limit. Gain, bandwidth, noise temperature and dissipation are specific to a given device and bias point rather than common to all cryogenic HEMTs.

HEMT are manufactured using various semiconductors like indium phosphide (InP), gallium arsenide (GaAs, for large scale QPUs [3331]), and gallium nitride (GaN) grown on substrates like silicon carbide (SiC), sapphire (α-Al_2O_3), or silicon.

Many labs and vendors produce HEMTs for qubit readout, like Chalmers University of Technology in Sweden using indium phosphide (InP) transistors which are very efficient at 4 K [3332]. The main vendor here is **Low Noise Factory** (described later, below) as well as **Cosmic Microwave Technology**, with HEMTs designed at Caltech.

Commercial HEMT amplifiers typically dissipate of the order of 10 mW at their nominal bias, which becomes a problem as the qubit count grows, even though the cooling power at the 4 K stage, around 1 W to 2 W, is far above what is available at 15 mK. One solution would be to use a variety of weakly dissipative TWPAs sitting at the 4 K stage, using superconducting materials operating at this temperature like NbTiN and put an HEMT at the 70 K cryogenic stage [3333–3336]. This would reduce the heat generated at 4 K.

RT amplifiers. Additional room-temperature RF gain is applied after the 4 K HEMT to match the signal level to mixers or ADCs. These stages are typically conventional low-noise or gain-block MMIC amplifiers. Shorter readout pulses occupy broader spectra, while longer pulses consume more of the QEC-cycle time. This creates a trade-off among readout speed, resonator spacing, amplifier bandwidth and the number of multiplexed qubits.

Microwave routing. It could help handle dynamically the connectivity between distant superconducting chips though waveguides [3337].

Now let's look at the amplification vendor space.

Low Noise Factory

Sweden, 2005

Low Noise Factory (LNF) designs and produces low-noise amplifiers (HEMT) operating at ambient or cryogenic temperatures as well as circulators and JPAs, including double circulators.

They are part of the European **OpenSuperQ** project, led by the University of Saarland in Germany, VTT in Finland and Chalmers in Sweden, to create commercial TWPAs. The consortium demonstrated in 2019 a TWPA with a maximal gain of 10 dB over a 1.4 GHz bandwidth.

Qanova Tech

Switzerland, 2026

Qanova Tech span out of a collaboration between EPFL and ETH led by Simone Frasca who did his PhD in Edoardo Charbon's AQUA lab on high-kinetic-inductance superconducting sensors, and is now a post-doc in Pasquale Scarlino's Hybrid Quantum Circuit lab. The venture is a consortium effort with Andreas Wallraff (ETH Zurich) as principal investigator and Scarlino and Vincenzo Savona (EPFL) as academic partners. Their first product will be a TWPA.

Qubic Technologies

Canada, 2020

Qubic Technologies is developing JPAs and TWPAs, their aim being to produce more correlations and better filtered noise. They also use this technology to improve radars. The company was created by Jérôme Bourassa (CEO), a former researcher from the Institut Quantique at the Université de Sherbrooke. He also collaborates with the Institute for Quantum Computing from the University of Waterloo. They started commercializing

their TWPA in 2026, including first sales to Quantum Machines.

QuantumCore

Canada, 2025, $7M

QuantumCore is a Toronto spun out of the Institute for Quantum Computing (IQC) at the University of Waterloo created by Eugene Profis (CEO) and Christopher Wilson (CTO). Their product is a kinetic-inductance traveling-wave parametric amplifier (KI-TWPA) that uses the nonlinear kinetic inductance of a superconducting transmission line to amplify superconducting readout microwave signals at around 10 mK. The company has access to Waterloo University's Quantum-Nano Fabrication and Characterization Facility (QNFCF).

QuantWare

The Netherlands, 2020

QuantWare sells the Crescendo TWPA, a commercially available product that provides more than 18 dB of gain over a bandwidth above 1.5 GHz. Launched in 2024, the Crescendo-S J-TWPA is half the size of their initial TWPA and packaged in a 6-unit array form factor in the Concerto product [3338].

Silent Waves

France, 2022

Silent Waves spun-out from CNRS Institut Néel in Grenoble. It was founded by Luca Planat, Nicolas Roch and Baptiste Planat.

Figure 412: Silent Waves's ZEPHYR TWPA in its packaging, including a pump coupler. Source: Silent Waves. 2026.

Their offering is a very efficient TWPA, based on the research conducted by CNRS-Institut Néel-UGA and the LPMMC in Grenoble [3339]. Their commercial TWPA added noise is near the quantum limit of noise (Figure 412). It enables high-fidelity single-shot qubit readout on a wide frequency band and with a gain that can exceed 20 dB [3340]. Based on a patented fabrication process, Silent Waves' amplifiers are currently being manufactured in the Grenoble CNRS Institut Néel clean room. They address both superconducting and silicon spin qubit readout, as they can be tuned to operate under magnetic fields [3341]. As a first stage, they will enable multiplexed readout of five to ten qubits. TWPAs could have applications beyond superconducting qubit readout, in microwave photonics, quantum sensing and quantum information with continuous variables [3342].

In 2024, the Silent Waves team, CNRS and KIT researchers in Germany proposed the design of an isolator that can replace some of the bulky circulators usually connected to TWPAs [3343]. A similar design associating a TWPA and an isolator was created by NIST in 2024 [3344] and at the MIT in 2025 [3345]. In Silent Waves, this technology is now named TWPAI (for isolator + TWPA). In 2026, Silent Waves also launched Zephyr, a two-in-one amplifier combining their TWPA with a pump coupler.

Withwave Co

South Korea, 2018

With Wave develops cryogenic RF/microwave components, including InP HEMT low-noise amplifiers for C-band (4-8 GHz), cryogenic attenuators and infrared filters. They also design TWPAs [3346].

BlueFors also sells an integrated TWPA and HEMT module with its whole cabling since 2024 [3347].

Finally, let's mention again **Cosmic Microwave Technologies** (2016, USA) which produces cryogenic LNAs (low noise amplifiers) used for qubit readout and is a spin-out of Caltech.

2.2.6 Cabling, connectors and filters

In current quantum systems based on superconducting qubits, copper coaxial cables carry microwave photon pulses at frequencies between 5 and 10 GHz that act on the qubits for their reset, for implementing quantum gates and handling qubit readout. Other cables are dedicated to continuous-wave pump delivery (powering the TWPA) and DC current (like for generating the flux bias used in tunable couplers, and for powering HEMT amplifiers).

Control chain. Microwave control signals are usually generated at room temperature and conveyed down the cryostat through lines that are thermalized, attenuated and filtered at different temperature stages. A total input attenuation around 50-70 dB is commonplace for superconducting-qubit microwave drive lines, often distributed over several stages, with different values and placements. Each 20 dB attenuator reduces incident power by a factor 100 while replacing upstream thermal noise with the thermal noise of its own stage. The dissipated power must be removed through the corresponding cold plate [3348, 3349].

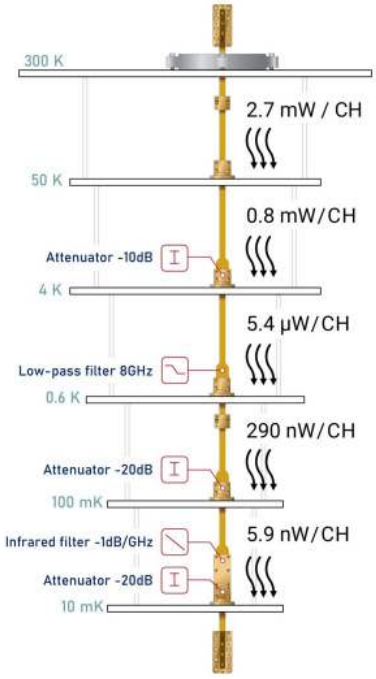


Figure 413: Cables heat load by level in the cryostat. Source: Delft Circuit, 2025.

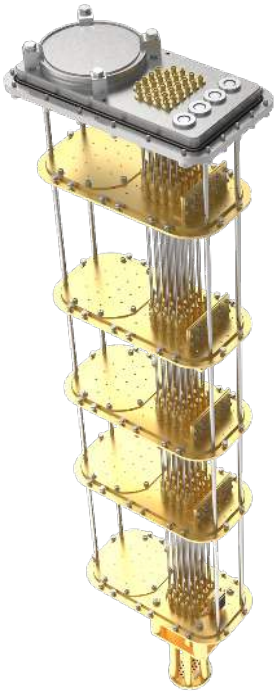


Figure 414: BlueFors optimized cabling system. Source: Bluefors, 2022.

The steady-state conductive heat leak of a cable is obtained by integrating the temperature-dependent thermal conductivity $k(T)$ over the temperature span. For a uniform cable of cross-section A and length L,

$$\dot{Q} = \frac{A}{L} \int_{T_1}^{T_2} k(T)\, dT$$

The familiar $\dot{Q} \approx kA(T_2 - T_1)/L$ expression is only an approximation when k can be treated as constant over the relevant temperature interval, which is often a poor assumption across cryogenic stages.

Control cables. Microwave input lines use materials such as stainless steel, CuNi, CuBe or phosphor bronze to reduce thermal conduction, together with staged attenuation that thermalizes room-temperature noise. They are not universally replaced by superconducting cable below 4 K. In many superconducting-qubit systems, lossy normal-metal coax remains useful on input and control paths, while low-loss superconducting NbTi cables are used on output and readout paths after the first amplification stage. DC wiring is used for flux bias, tunable couplers, thermometry and powering selected cryogenic electronics. Cable conduction and attenuator dissipation consume part of each stage's cooling budget and create a substantial scaling challenge (Figure 413).

Flexible cables. It is possible to miniaturize some of this, especially with flat ribbon flexible cables. These various cables cost several thousand dollars per unit, so the full input, output and DC wiring set of a system with a few tens of qubits represents a significant share of its cost. A meaningful comparison with the cryostat price requires naming the system, listing the cable assemblies and passive components included, and stating the price date and currency, which is why no single figure is quoted here. Bluefors sells their own optimized cabling system, such as a 168-cable High-Density Wiring, which supports 56 qubits (Figure 414). The same is true with the removable cable system of the Oxford Instruments (Quantum Design Oxford since late 2025) Proteox (Figure 415). Vendors like Delft Circuits are selling flat flexible superconducting cables also made of NbTi. Superconducting flexibles can also be made of yttrium barium copper oxide (YBCO) and magnesium diboride (MgB_2) [3350] but are seemingly not used in quantum computing applications [3351].

Readout cables between the millikelvin and 4 K stages are often low-loss superconducting coaxial cables, commonly using NbTi. In the superconducting state they have zero DC resistance in the ideal limit, but microwave transmission still has finite insertion loss from conductor surface impedance, dielectric loss, connectors and impedance mismatch. Their static conductive heat leak and their RF dissipation are separate quantities that both matter in cryogenic design [3352]. Frequency multiplexing allows one readout cable to serve several resonators, with the multiplexing factor depending on the full readout chain. The signal is commonly amplified first by a JPA or TWPA near the millikelvin stage and then by a HEMT near 4 K. CoaxCo is the leading supplier of NbTi coaxial cables, but it is not the only one. KEYCOM, for example, also supplies NbTi–NbTi su-

Figure 415: Oxford Instruments (Quantum Design) removable cabling system.

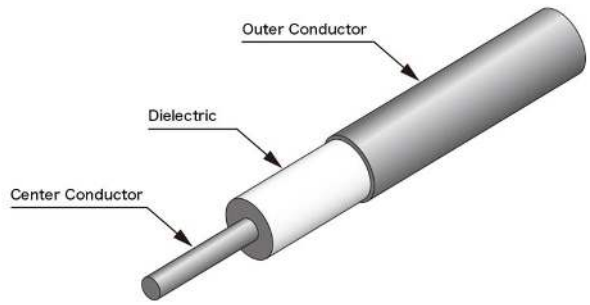


Figure 416: A typical CoaxCo niobium-titanium cable. Source: CoaxCo.

perconducting coaxial cable assemblies. The dielectric is typically PTFE or another low-loss polymer.

So, how can we reduce cable clutter by multiplexing signals? Various options are on the table, bearing in mind that the achievable multiplexing factor depends on the qubit modality, resonator spacing, resonator linewidth, readout time, crosstalk, amplifier linearity, switching topology and the fidelity that is considered acceptable, rather than on a single fixed number:

- **Time multiplexing**, which is done at the expense of longer computing times since you execute fewer quantum gates in parallel [3353]. It can be based on a qubit row-column addressing technique, like in a classical memory [3354], but with the same caveat. In 2026, IMEC prototyped a FDSOI CryoCMOS chip handling time division multiplexing at 10 mK and consuming only 200 pW (for 4 channels). It can be used for both multiplexing and demultiplexing [3355].
- **Frequency multiplexing** which is troublesome due to spectral crowding in narrow bandwidths, in the 5 to 6 GHz zone. It is currently used mainly in the qubit-readout chain, with a typical 4 to 16 readout signals sharing one coaxial chain depending on resonator spacing, linewidth and amplifier linearity, passing through circulators, a TWPA and a HEMT.
- **Optical conversion of drive and readout signals** separates the delivery of control pulses (downlink) from the extraction of qubit states (uplink) using optical fibers to mitigate the heat load of conventional coaxial cables. On the downward qubit control path, room-temperature electronics can generate shared optical pulse templates that are sent down to a 4 K hybrid photonic/CMOS controller. At the 4 K stage, local cryo-CMOS circuits can perform transmission control, microwave pulse shaping, and local microwave mixing to generate the final single- and two-qubit control drives [3356]. This reduces active power dissipation by keeping high-speed waveform DACs at room temperature [3356]. On the upward readout path, 5 GHz microwave signals must be frequency up-converted to 200 THz optical photons. This can be achieved using phonon-based mechanical resonators, cavity optomechanics, and optomechanical crystal resonators [3357–3359], coplanar waveguides and optical cavities using the dark state protocol [3360], or electro-optic transducers such as a flip-chip microwave LC circuit resonator coupled to a high-quality factor silicon nitride membrane, built by NIST and the University of Colorado [3361]. One must account for the full-stack thermal cost of demultiplexing, continuous photodetection, and switching within the cryostat, as well as the microwave signal quality after its dual transduction to and from optical wavelengths. A China team experimented uplink and downlink multiplexed control in 2026 [3362], associated to a thin-film lithium niobate (TFLN) based traveling-wave Brillouin M2O transducer for qubit readout (from 9 GHz microwave photons to 1550 nm telecom band optical photons) [3363]. IBM is investigating such optical links for scaling its superconducting computer systems [3364]. Above 4 K, conventional coax cables use materials like copper alloys, but their collective thermal load fundamentally limits the number of physical qubits, explaining why optical pathways and alternative electrical solutions using cryo-CMOS or SFQ control running at 4 K or below [3365] are so heavily investigated.
- **Upconverting readout microwave signals** to optical photons for multiplexing. QPhoX experimented in 2025 such a conversion with their piezo-optomechanical transducer, along with Rigetti and Qblox. The reported 81% single-shot readout fidelity, for that transducer, conversion efficiency, added noise and bandwidth, is below the level assumed here for fault-tolerant operation. It could potentially reduce the cable clutter in cryostats although with a relatively low impact given readout microwaves are

already multiplexed by an order of magnitude thanks to the use of TWPAs [3366].

In general, a system's cabling design is an optimizing problem under constraints, where different factors are accounted for like the selection of the number of cold plates and operating temperature, the placement of attenuators and filters, total heat dissipation cryogenic cost, available space in the cryostat, system costs and impact on qubit operation fidelities [3367].

Now, onto the vendors in this space. Funding, acquisitions, product ranges, partnerships and corporate status were updated as of September 2026.

Arctic Instruments

Finland, 2024, €2.35M

Arctic Instruments is a spin-out from VTT which sells a TWPA with a tunable central frequency.

Figure 417: Arctic Instruments TWPA.

Atem

France, 1990

Atem is a coaxial cables designer and manufacturer. It wants to enter the quantum computers space with the collaborative Qryolink project to propose superconducting coaxial cables, in collaboration with Radiall.

Bifrost Electronics

USA, 2025, $2.5M

Bifrost Electronics is a Colorado-based quantum readout startup that is developing scalable, magnetically insensitive quantum amplifiers. It was created by Zenith Tillemann-Dick (CEO), Connor Denney (R&D) and Logan Pauli (CTO).

Connor Denney is the coauthor of [3368] which describes a chip-scale device that generates a broadband optical frequency comb using a triply resonant electro-optic (EO) architecture. This comb spans over 60 THz and contains more than 2,000 distinct frequency lines which can be used as independent optical channels usable for frequency-division multiplexing including upconversion of microwave readout signals. It uses thin-film lithium tantalate, rather than the more common lithium niobate, which helps mitigate birefringence and improves spectral coverage.

CryoCoax

UK/USA

CryoCoax is a division of Intelliconnect providing RF interconnect assemblies based on NbTi , cupro-nickel, beryllium-copper, stainless steel and brass.

They provide high-density multiway connectors using the SMPM interface (created by Carlisle Interconnect Technologies) which supports a 4.75 mm pitch instead of the roughly 15 mm pitch of conventional SMA connectors. They develop their own flexible cables [3369] and also distribute cabling solutions from Delft Circuits and passive components from OmniSpectra.

Delft Circuits

the Netherlands, 2016, €20M

Delft Circuits was created by Sal Jua Bosman (CEO), Daan Kuitenbrouwer (COO) and Paulianne Brouwer (CFO), the first two coming from TU Delft. They had a staff of 45 as of December 2025.

Their offering consists of cables and flexible mats made of cables that carry microwave control pulses to superconducting qubits, such as CF3 (Cri/oFlex) and supporting frequencies ranging from 2 to 40 GHz with 8 embedded cables, with no impact on qubit fidelities [3370] (Figure 418). Their cables combine NbTi and silver. They include attenuators, low-pass filters and infrared filters. The Cri/oFlex range covers qubit microwave pulse drive lines while the Cri/oFlex Flux line covers DC drive.

Figure 420: Delft Circuit flexible cables and their SMP coaxial end connectors. Source: courtesy of Delft Circuit, 2025.

Delft Circuit also introduced in March 2022 their Tabbi, an ultra-high density modular flexible microwave interconnect that consolidates the equivalent of 8 SMA cables in about 10 mm and embeds its own filters. In 2025, they launched a High-Density Input/Output (HD I/O) system supporting 256 channels per module (Figure 419). They also provide side loaders.

Their roadmap Figure 421 is inline with various vendors plans to scale superconducting qubits into the FTQC realm with loaders supporting 1,024 to 4,096 channels by 2027 and 2029, support for thousands of physical

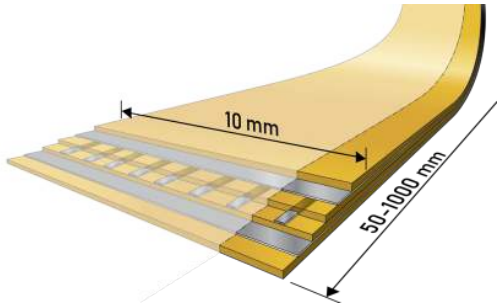


Figure 418: Delft Circuit flexible cable internal architecture. Source: courtesy of Delft Circuit, 2025.

Figure 419: Delft Circuit High-Density Input/Output (HD I/O) system launched in 2025. Source: courtesy of Delft Circuit, 2025.

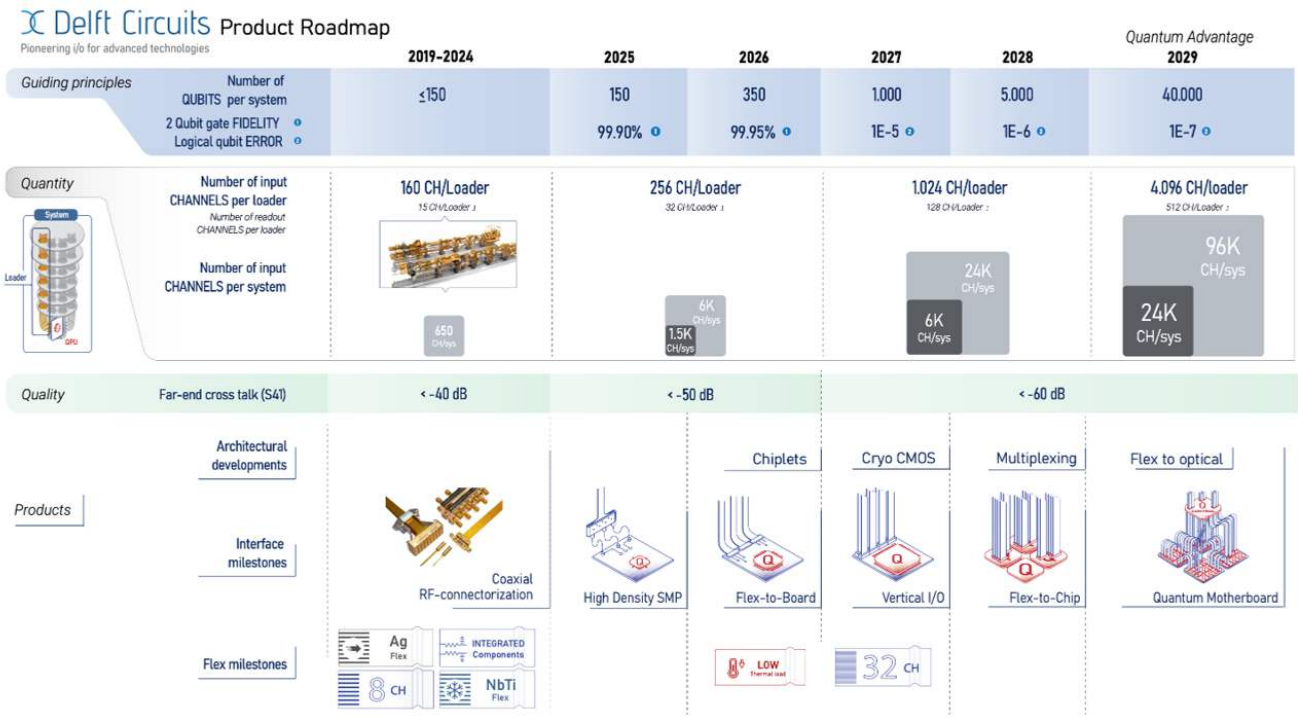


Figure 421: Delft Circuit roadmap as of December 2025. Source: courtesy of Delft Circuit, 2025.

qubits with high density SMP connectors (SubMiniature Push-On RF coaxial connector, Figure 420), vertical I/O in-line with QuantWare's VIO plans and flex-to-chip (Figure 421).

They manufacture their products out of a 150 m^2 lab located at the Delft Quantum Campus. The company got financial support from many EU programs (AVaQus, MATQu and SPROUT).

Dimira Technologies

India, 2024

Dimira Technologies is a spin-off from IIT Mumbai which develops flexible RF/microwave cryogenic cables. They seem to also work on unrelated quantum cybersecurity (PQC).

Isentroniq

France, 2025, €7.5M

Isentroniq is a spin-off from Alice&Bob created by Paul Magnard (CEO) and Théodore Amar (COO). They plan to develop several yet undisclosed technologies to better scale cabling and connectivity for solid-state qubit control.

QDevil

Denmark, 2016-2022, €1M

QDevil sells filters used in cryostats including the QFilter, based on a collaboration between Harvard University and the University of Copenhagen. It is a cryogenic filter reducing electron temperatures below 100 mK.

They also sell the QDAC, a 24-channel low noise DAC, the QBoard, a PCB-based fast-exchange cryogenic chip

carrier system, and the QBox, a 24-channel breakout box. They are partnering with Bluefors. The company was acquired by Quantum Machines (Israel) in March 2022.

Quantum Logic

the Netherlands, 2025

Quantum Logic is developing active cryogenic microwave electronics, starting with a demultiplexing module operating at cryogenic temperatures. Their know-how is in nonlinear frequency conversion and cryogenic-optimized multiplexing.

QTREX Quantum

Israel, 2018, $105M

QTREX is a company led by Dagi Ben-Noon (CEO), Avi Shabtay (COO, R&D Manager) and Daniella Yeheskely-Hayon (CTO). It was initially a medtech company developing cardiopulmonary bypass system and blood monitoring platforms, created as Clearx Medical, renamed as Insense Medical in 2018, then Inspira Technologies Oxy in 2020, and finally QTREX Quantum in May 2026. Listed on the Nasdaq, the company pivoted on quantum through the acquisition in April 2026 of Nano Dimension's additively manufactured electronics (AME) business.

Their product line comprises 3D electronic printing systems, conductive and dielectric inks, design and simulation software, and ink manufacturing. Their quantum interconnect is based on a monolithic architecture integrating conductor, RF dielectric, shielding, thermal management, and mechanical routing into a single printed structure that can replace discrete cryogenic cabling. They can pack 20 shielded conductors per square centimeter with good signal transmission from 10 MHz to 20 GHz, although all this technology's thermal characterization has not yet been detailed in a scientific paper. They plan to support 17,280 coaxial lines in a regular cryostat. One of their partners is Qarakal Quantum, the Israeli superconducting qubit startup.

Radiall

France

Radiall is an industry company specialized in connectors and cabling, very active in the aerospace vertical. They have been addressing quantum technology needs for over a decade.

Radiall creates solutions for the quantum industry, including ultra-miniature microwave board-to-board connectors, 3D cabling and cryogenic switches. Radiall product portfolio supports various quantum computing technologies that require microwave components meeting strict electromagnetic compatibility/electromagnetic interference (EMC/EMI) constraints, cryogenic, non-magnetic and density specifications (Figure 422). It develops side loaders and high-density cabling solutions.

Rosenberger Group

Germany

Rosenberger Group is involved in the German qBriqs projects to build connectors, attenuators components, niobium-titanium and stainless cables assembly to be incorporated in 80 channel multiport connectors and flat cables (with a 1 mm pitch) developed by **Supracon AG** and **LPKF**. They plan to produce these flat cables with 3D printers.

VIQTHOR

France, 2022

VIQTHOR created an optical-based fiber multiplexing solution for microwave drive.

Sweden Quantum

Sweden, 2023

Sweden Quantum is a spin-out from Chalmers University created by Simone Gasparinetti which develops infrared filters, the latest being the HERD-2. It attenuates electromagnetic signals above 70 GHz. It is used in cryostats in the connectivity chain controlling solid-state qubits.

XMA Corporation

USA, 2003

XMA Corporation provides the OmniSpectra product line comprising adapters, attenuators, couplers and other passive cryo-electronic components used in quantum computing.

Maybell Quantum is also present in the cabling market with its LF CryoTrace flexible cable announced in 2026 that is based on a licensed technology developed at the MIT Lincoln Laboratory Quantum-Enabled Computation Group. The cables are built using phosphor bronze and operate at the 15 mK stage. They remain flexible at this temperature. The stripline configuration uses conductive layers between flexible polymer layers that shield the conveyed signals against electromagnetic interference, which would otherwise generate crosstalk. At this point, the cables convey only direct current (DC) for tunable couplers, thermometry, heaters, and sensors.

Outside the commercial space, **SuperCables** was an IARPA-funded US program launched in 2019 aimed at high-data-rate, low-power links between room-temperature and cryogenic electronics, including electro-optic conversion and fiber transmission.

2.2.7 Other electronics vendors

Let's now look at other commercial vendors in the cryogenic electronics area, given they don't create any cryo-CMOS at this point.

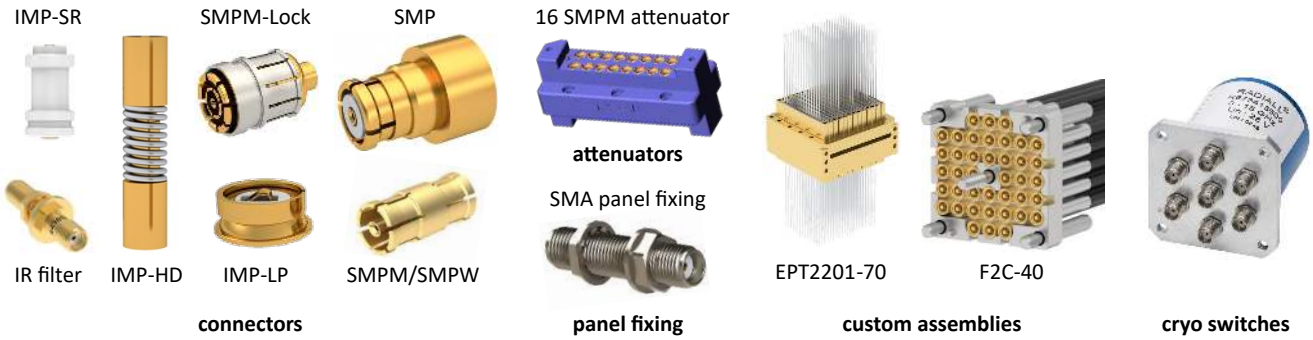


Figure 422: Examples of Radiall connectors, attenuators, panel fixing, custom assemblies and cryo switches. Source: Radiall. August 2024.

AnaPico

Switzerland, 2005

AnaPico is a provider of low phase noise RF signal generators, for the local oscillators used in qubit control and readout, running up to 6.1 GHz.

apitech

USA, 1999

apitech is a provider of cryo-attenuators targeting the quantum computing market and covering signals from DC to 40 GHz, and with SMA, and SMPM connectors.

Atlantic Microwave

USA, 1989

Atlantic Microwave produces and markets radiofrequency and microwave components operating at cryogenic temperatures.

They are used to control superconducting and silicon qubits in cryostats. This includes microwave attenuators, filters, microwave amplifiers and bias tees. It is a subsidiary of the British group ETL Systems, founded in 1984.

ConScience

Sweden, 2025

ConScience sells the QiB1 and QiB2 couplers, which can be used to test one or two qubits respectively, at fixed frequency.

CryoHEMT

France, 2019

CryoHEMT is a company created by Quan Dong and Yong Jin in Orsay, France. It designs and manufactures low-noise HEMT microwave amplifiers that amplify microwaves at the 4.2 K cryostat stage. Their technology is based on the PhD thesis from Quan Dong done under the supervision of Yong Jin in France in 2013. It does not appear to be used in quantum information systems.

Diramics

Switzerland, 2016

Diramics is a spin-off from ETH Zurich creating ultra-low noise transistors in III-V materials (InP, indium-phosphorus) with a technology named pHEMT (pseudomorphic high-electron-mobility transistor, using junctions with two semiconductors with different band gaps). It can be used in low temperature electronics. It is currently mostly used in astronomy applications.

Holzworth Instrumentation

USA, 2004

Holzworth Instrumentation is a provider of multi-channel RF sources and AWGs. They also provide phase noise analyzers. The company was acquired by Wireless Telecom in 2019.

Marki Microwave

USA, 1991

Marki Microwave is a supplier of microwave control components: amplifiers, bias tees, couplers, mixers and filters.

Ohtama

Japan, 1964

Ohtama is a magnetic shields vendor some of which could be used to protect qubit chips in the cryostat.

Paragraf

UK, 2018, $85M

Paragraf is a spin-out of Cambridge University that manufactures graphene electronics, including sensors for cryogenic applications that monitor the ambient magnetic field and enable magnets and magnetic shielding calibration.

QETSweden

Sweden, 2025

QETSweden is a spin-out from Chalmers University created by Per Delsing (CSO). Their offering contains a TWPA with 4 GHz of gain bandwidth that was launched at the APS in March 2025, the QET Vidar Model S, a single-amplifier and the QET Vidar Model D with two TWPAs into a single package.

QSculptor

USA, 2026

QSculptor provides a qubit diagnostic platform that detects microscopic material defects in superconducting circuits, that limit coherence, yield, and manufacturability. It uses controlled electric fields applied to the qubit environment to probe and spatially localize decoherence-inducing defects inside cryogenic systems. It converts invisible fabrication variability into actionable data for process and yield optimization. The company was created by George Zoidze. The scientific foundation comes from the TLS characterization technique developed by the group of Alexey Ustinov at KIT in Germany, specifically the Electric Field Spectroscopy (EFS) technique [3371].

Quantcore

UK, 2025, £2.5M

Quantcore Technologies is a University of Glasgow spin-out founded in August 2025, operating from the James Watt Nanofabrication Centre in Glasgow. It designs, manufactures, and tests niobium-based superconducting processors, resonators, and sensors for quantum computers, precision sensing systems, and secure communications infrastructure. The four co-founders come from the University of Glasgow Quantum Circuit Group: Jack Brennan (CEO) and Valentino Seferai (CTO), with Martin Weides being a scientific advisor.

Their product range covers three markets: superconducting processors and resonators supplied as foundry components to quantum computer builders and national laboratories, medical imaging quantum sensors and secure communications.

They use niobium rather than aluminum. Niobium has a critical temperature of about 9.2 K versus about 1.2 K for aluminum, so within weak-coupling BCS scaling its superconducting gap is roughly 7-8× larger. The higher gap can suppress thermal quasiparticle populations at a given temperature and can enable higher-frequency, higher-temperature circuit designs, but it does not imply a universal fixed operating-temperature ceiling or an eightfold usable frequency range. A niobium platform has demonstrated superconducting qubits above 20 GHz operating above 200 mK [3291]. All-niobium transmons have reached $T_1 \approx 62\,\mu$s [3372], while tantalum-encapsulated niobium devices have median $T_1 > 300\,\mu$s and maxima approaching $600\,\mu$s [3373]. Niobium surface oxides remain an important loss channel [3373].

Quantum Microwave

USA, 2016

Quantum Microwave (2016, USA) creates microwave components operating at cryogenic temperatures for quantum computers, including JPA amplifiers, attenuators, frequency couplers, multiplexers, bias tees, diplexers, filters, image reject mixers and directional couplers.

QuEL

Japan, 2021

QuEL is a startup that provides room temperature qubit control electronics that came out of Osaka University. The QuEL-1 is an all-in-one 3U rackable solution to control qubits from gates to readout. In its published configuration it has 8 output channels at 16-bit and 4 input channels at 12-bit, covering 7–11 GHz. They collaborate with RIKEN on the development of QuBE/Qubex, an integrated control hardware–software platform [3374].

QuinStar Technology

USA, 1993

QuinStar Technology is a vendor of cryogenic circulators, coming from the acquisition of Pamtech (USA) in 2010.

Raditek

USA, 1993

Raditek is a designer and provider of RF signal-processing systems, including the circulator magnet-based filters used between the first-stage microwave amplifier at 15 mK and the second-stage amplifier at 4 K used usually with superconducting qubits.

Raytheon

USA

One main applied research domain for **Raytheon** is related to superconducting qubit control. They work on arbitrary pulse sequencers (APS) creating superconducting qubit control microwaves, an FPGA readout system using low noise parametric amplifiers and a custom made three-wave-mixing JPAs with 20 dB gain as shown in Figure 423.

They are also exploring SFQ based control logic (Josephson gate-based logic) and spintronics based low-power memories. They are mainly found in superconducting qubits quantum computers (IBM, Google, Rigetti, D-Wave). However, they do not push forward the miniaturization of these components like what SEEQC is doing. In October 2021, they announced a technology partnership with IBM, with not many details [3375]. On top of that, they also develop Josephson junction based infrared photon detectors [3376].

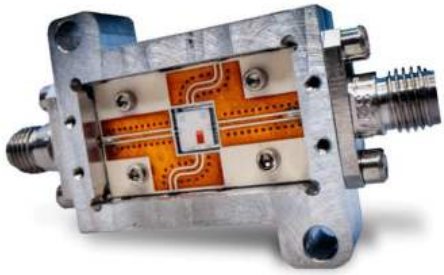


Figure 423: A Raytheon BBN JPA.

RF-Lambda

USA, 2003

RF-Lambda also provides circulators and low-noise amplifiers.

Scalinq

Sweden, 2022

Scalinq was created by a team coming from Chalmers University with Zaid Saeed (CEO), Lisa Rooth (VP) and Robert Rehammar (CTO).

They want to help superconducting quantum computers companies design larger QPUs. Their offering is a QPU chip sample holder named LINQER, with 16, 36 and 80 connectors. It provides low crosstalk, an innovative magnetic shielding technology, and supports chip sizes up to 20×20 mm^2 in this configuration.

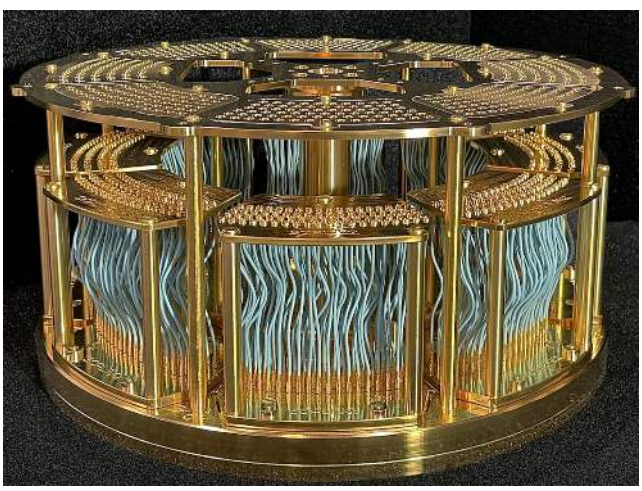


Figure 424: Scalinq LINQER600 processor packaging. Source: [3377].

They announced a partnership with Qblox in September 2023 which makes sense. Indeed, Qblox hardware outputs are connectors for coaxial cables that can land in Scalinq's connectors. The company is also partnering with Atlantic Quantum, another Swedish startup.

In March 2024, Scalinq extended its packaging offering with the LINQER600, which can accommodate controls for hundreds of qubits and up to 600 lines (Figure 424). It was developed in cooperation with IQM which is using it in its forthcoming 150 qubit Radiance QPU.

T0.technology

Canada, 2021

T0.technology develops quantum computing control electronics solutions. It supports over a thousand independent pulses per I/O, arbitrarily sequenced or combined, low-latency feedback, direct digital synthesis at RF-frequencies and real-time pulse generation, using pre-computed or algorithmically determined pulse-profiles. The company also manufactures superconducting sensors.

Wenteq Microwave Corp

USA, 2006

Wenteq Microwave Corp provides low-noise amplifiers, attenuators, circulators and coaxial connectors, in the RF/microwave range.

Yquantum

Switzerland, 2024

YQuantum provides superconducting qubit-control electronics including a sample holder equipped with 20 RF ports. They also sell filters, packaging, IR-filter array, DC-block and Flux BiasT (Figure 425).

Figure 425: Yquantum products.

2.2.8 Thermometers

It is possible to measure **pressure**, **temperature** and gas **flow** at cryogenic temperatures. Cryogenic thermometers are installed at several points on the refrigerator stages and sample assembly. Many established thermometer technologies are shown in Figure 426. NV-center thermometry is an additional research technique for local or nanoscale temperature sensing [3379].

Commercial cryogenic sensors include **Lake Shore Cryotronics** Cernox thermometers, with model-dependent operation down to about 100 mK and relatively low magnetic-field-induced errors, and ultra-low-temperature ruthenium-oxide sensors calibrated to about 10 mK, with some calibrations or extrapolated points extending to 5 mK. These limits are calibration-dependent and are quoted for the sensor alone, excluding self-heating and thermalization in a given mount.

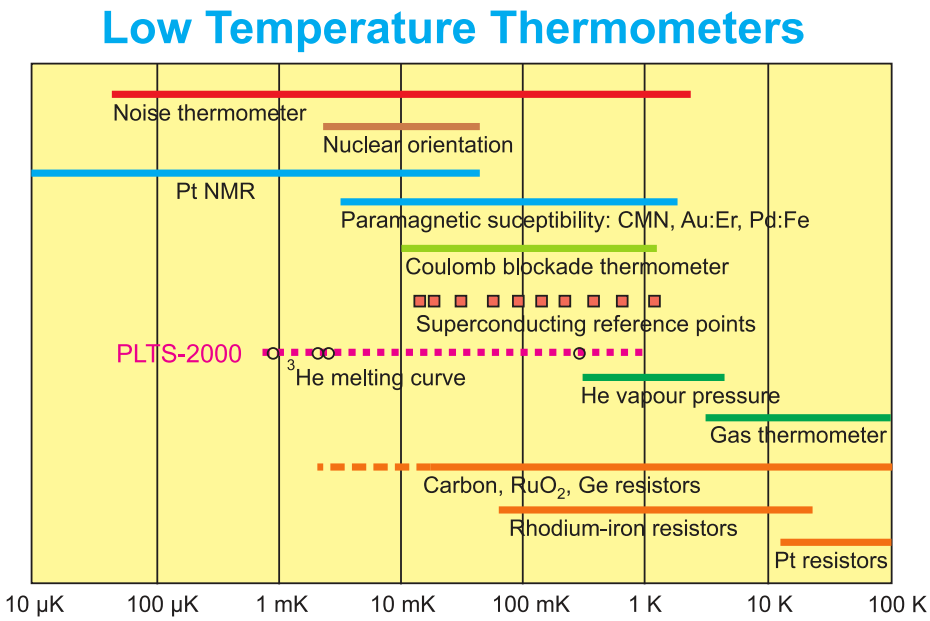


Figure 426: Categories of low-temperature thermometers. Several thermometer technologies operate below 1 K. Coulomb-blockade thermometers use arrays of tunnel junctions and infer temperature from the temperature-dependent differential-conductance curve, notably the width and depth of the conductance dip. Source: [3378].

Below roughly 20 mK there is no single mandatory thermometer technology. Johnson-noise thermometry, Coulomb-blockade thermometry, ruthenium-oxide sensors and other primary or secondary techniques may be used depending on accuracy, magnetic field, self-heating and calibration requirements. At these temperatures, thermalization and sensor response time are also important because the thermometer may not instantaneously track the sample temperature.

Temperature can even be measured within cryo-CMOS chips operating at 20 mK to a couple K, as proposed by Quantum Motion [3380, 3381].

Qprobe

Switzerland, 2024

Qprobe provides a cryogenic temperature probing station that supports measurements at temperatures below 2 K. It contains a 3-axis piezo positioning unit, a sample holder with heater and temperature sensor, an interchangeable probe card, and standardized electrical connectors.

Figure 427: Qprobe temperature prober.

2.2.9 Bibliography and notes

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This **Control electronics** subsection contains 310 bibliographical references and notes containing at least 4,122 pages.

2.3 Photonics

We explore here the broad field of photonics enabling technologies used in quantum technologies. The first are of course the many lasers used to power quantum communications, quantum sensors and quantum computing using light and atoms. Then, you have all the devices modifying the course and properties of photons, their phase, polarisation, and path.

2.3.1 Lasers

Masers and lasers are applications of three successive discoveries and inventions:

- **Fabry-Pérot resonant cavities**, named after Charles Fabry (1867-1945) and Alfred Pérot (1863-1925). Their system, invented in 1898, was originally used to create an interferometer.
- **Stimulated emission**, formalized by Albert Einstein in 1917. It occurs when an incident photon resonant with a transition stimulates an excited emitter to make a transition to a lower energy level while emitting an additional photon into the same optical mode.
- **Optical pumping**, proposed by Alfred Kastler in 1950 at ENS in France. His optical methods for studying Hertzian resonances in atoms earned him the 1966 Nobel Prize in Physics.

Optical pumping can create a population inversion by transferring population to an upper laser level, such as E_2 in Figure 428, faster than it leaves that level. In common three- and four-level schemes, pumping may excite a still higher level, followed by rapid non-radiative relaxation to the upper laser level. A separate relaxation path empties the lower laser level toward the ground state E_0.

A simple resonant two-level system cannot sustain a population inversion under steady pumping because absorption and stimulated emission compete on the same transition. Three- and four-level schemes avoid this limitation. Both schemes can operate in pulsed or continuous-wave mode, although four-level lasers generally reach inversion more easily because the lower laser level is rapidly depopulated.

A laser combines a gain medium with optical feedback, usually from a resonant cavity. The gain medium can be pumped optically, electrically or chemically. Once population inversion is created, spontaneous emission can seed a cavity mode and stimulated emission then amplifies that mode. Stimulated emission adds a photon to the stimulated optical mode, so its frequency, polarization, propagation mode and phase relation are set by that mode. In broadened, multimode or nondegenerate systems the emitted photon is therefore not simply identical to an arbitrary incident photon. The gain medium is placed inside an optical resonator, often a linear cavity formed by two mirrors. One mirror is highly reflective and the output coupler is partially transmissive, allowing a fraction of the amplified intracavity field to leave the laser.

The resonator provides optical feedback and selects spatial and longitudinal modes that satisfy its boundary conditions and experience sufficient net gain. Off-axis or poorly matched modes generally experience larger losses, while resonant modes repeatedly traverse the gain medium and are amplified.

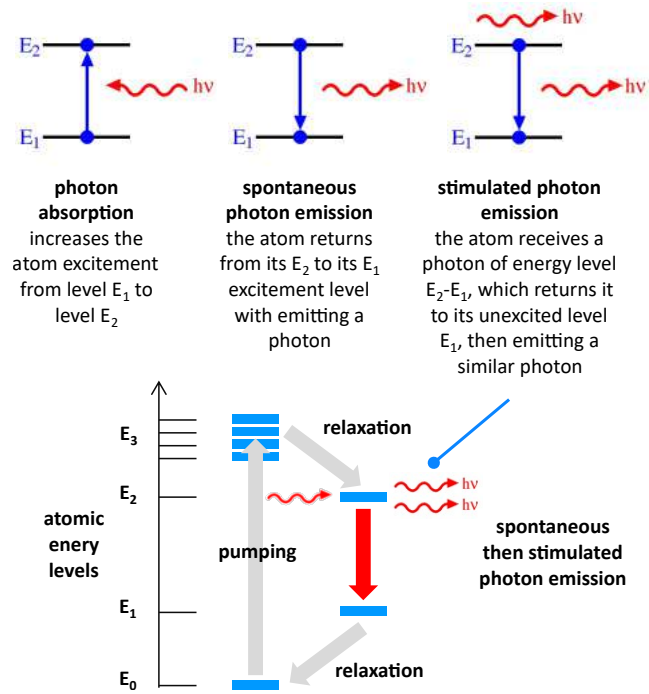

Figure 428: How lasers work. © Olivier Ezratty, 2021-September 2026.

The output is highly **directional**, can have a very narrow **linewidth**, and exhibits high spatial and temporal **coherence**. In a simple linear cavity, longitudinal resonances approximately satisfy $2nL = m\lambda$, where nL is the one-way optical path length and m is an integer. The emitted frequency is selected jointly by the gain spectrum and the cavity resonances. As an order of magnitude, a 1 mW laser at 650 nm emits about 3.3×10^{15} photons per second.

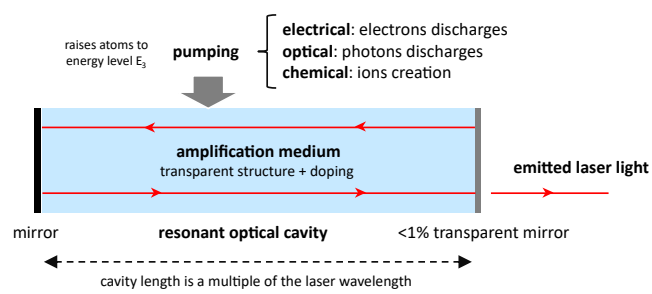

Figure 429: How a laser works in its cavity. © Olivier Ezratty, 2021-September 2026.

The optical-maser concept was formalized by Arthur L. Schawlow and Charles H. Townes in 1958 [3382]. The first working laser was Theodore Maiman's optically pumped ruby solid-state laser in 1960 [3383]. The first helium-neon gas laser was demonstrated by Ali Javan, William R. Bennett Jr. and Donald R. Herriott later in 1960 and reported in 1961 [3384]. **Excimer** gas lasers emit mainly in the ultraviolet.

Laser families include **doped-crystal solid-state lasers**, such as ruby, Al_2O_3:Cr^{3+}, and Nd:YAG, based on $Y_3Al_5O_{12}$ doped with Nd^{3+}. **Chemical lasers** often operate in the infrared. **Semiconductor diode lasers** use several III-V material systems including GaAs and InP. **Fiber lasers** typically use rare-earth dopants such as erbium, ytterbium or neodymium and are widely used in telecommunications, metrology and industry. **Free-electron lasers** were already briefly covered in the relativistic quantum mechanics section (Figure 430).

Lasers can operate continuously or in pulses. Pulsed systems can reach very high peak powers and, with mode locking and nonlinear frequency conversion, can generate femtosecond pulses. High-harmonic generation driven by ultrashort lasers can produce attosecond pulses, usually in the extreme-ultraviolet range. **Anne L'Huillier**, **Pierre Agostini** and **Ferenc Krausz** were awarded the 2023 Nobel Prize in Physics for experimental methods that generate attosecond pulses of light for studying electron dynamics in matter. High-power laser systems often use a low-power seed followed by one or more gain stages. Tunable lasers allow the output wavelength to be adjusted over a finite range.

Laser applications span a few broad categories: materials processing (drilling, cutting, surface stripping, stereolithography 3D printing), data storage and printing (Laserdisc in 1978, audio CDs in 1982, DVDs in 1995, laser printing, barcode readers and scanners), medicine (ophthalmology, dermatology, cosmetic and refractive surgery), metrology and sensing (construction alignment, velocity measurement, LiDAR, depth and focus sensors, confocal microscopy, flow cytometry, DNA chip analysis), telecommunications, defense and inertial-confinement fusion, and astronomy with adaptive optics. Quantum applications add atom cooling and trapping, quantum communications, quantum cryptography and quantum computing. Lasers are therefore pervasive across quantum science and technology [3385].

The frequency ranges covered by lasers range from infrared to ultraviolet (Figure 431). There are even types of lasers with adjustable frequency. Free electron lasers go as far as X-rays. No generally accepted operational gamma-ray laser, or graser, has been demonstrated so far.

Quantum technologies use many platform-specific wavelengths (Figure 432). Around 775 nm is commonly used as a pump wavelength for spontaneous parametric down-conversion that generates photon pairs near the 1,550 nm telecom C band, while 1,550 nm is important for fiber-based quantum communications because standard silica fiber has low loss at this wavelength. Trapped ions, neutral atoms, NV centers and semiconductor emitters instead require wavelengths matched to their atomic or solid-state transitions.

Quantum frequency conversion can interface emitters or processors operating at different optical wavelengths. It is useful, but not mandatory, when a photonic processor already emits in a low-loss telecom band. Microwave-to-optical quantum transduction is a separate challenge relevant to qubits whose native transitions are in the microwave domain, notably superconducting qubits and some spin systems. Solid-state optical emitters such as quantum dots and color centers already have optical transitions. The transferred quantum state may be encoded in polarization, time bins, frequency bins or other photonic degrees of freedom.

Another important class is **femtosecond lasers**, which generate ultrashort coherent pulses with durations on the order of 10^{-15} s. Picosecond lasers, around 10^{-12} s, are usually treated as a neighboring ultrafast class. Such sources are used in micromachining, spectroscopy, frequency-comb generation and quantum sensing [3386].

The **maser**, for "Microwave Amplification by Stimulated Emission of Radiation", preceded the laser. The first experimental ammonia maser was built by James P. Gordon, Herbert J. Zeiger and Charles H. Townes in 1953-1954 and operated near 23.87 GHz [3387]. Nikolay Basov and Alexander Prokhorov independently developed related maser principles. Townes, Basov and Prokhorov shared the 1964 Nobel Prize in Physics. Hydrogen masers followed around 1960.

There are many laser vendors who play a role in the second quantum revolution, both with photon qubits, quantum telecommunications, quantum cryptography and quantum sensing. Lasers are also used to control cold atoms and trapped-ions qubits.

Chromacity

UK, 2013

Chromacity is a manufacturer of lasers targeting various industry and research needs, including quantum communications.

DenseLight Semiconductors

Singapore, 2000

DenseLight Semiconductors manufactures various laser products.

FemTum

Canada, 2016

FemTum creates mid-infrared lasers which can be used in quantum optics and silicon photonics applications and quantum sensing using optical frequency combs. It

gas	doped crystals	chemical	diodes	fibers	free electrons
ionized argon ionized krypton helium-neon copper-neon nitrogen CO_2 excimers	ruby Nd-YAG rare earths titanium chromium OPO	hydrogen-fluoride deuterium-fluoride	GaAs DFB VCSEL	ytterbium erbium Nd^{3+}	

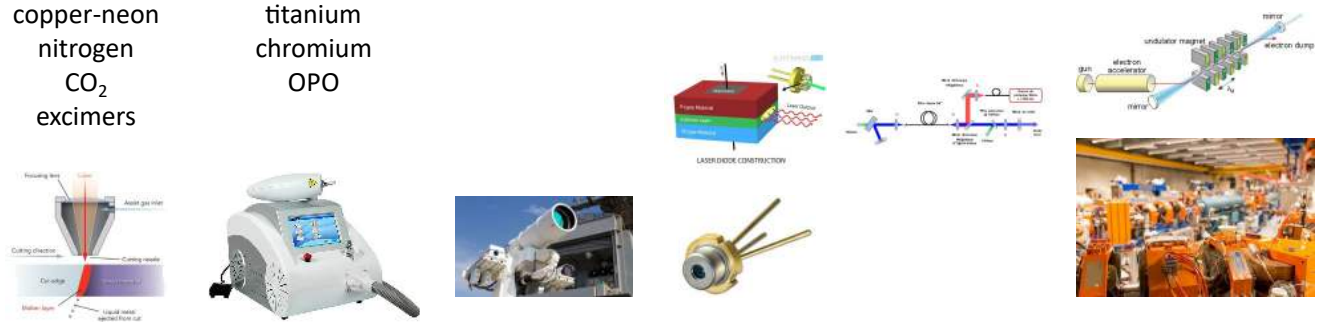

Figure 430: The various types of lasers and their cavity materials. Olivier Ezratty, 2021-September 2026.

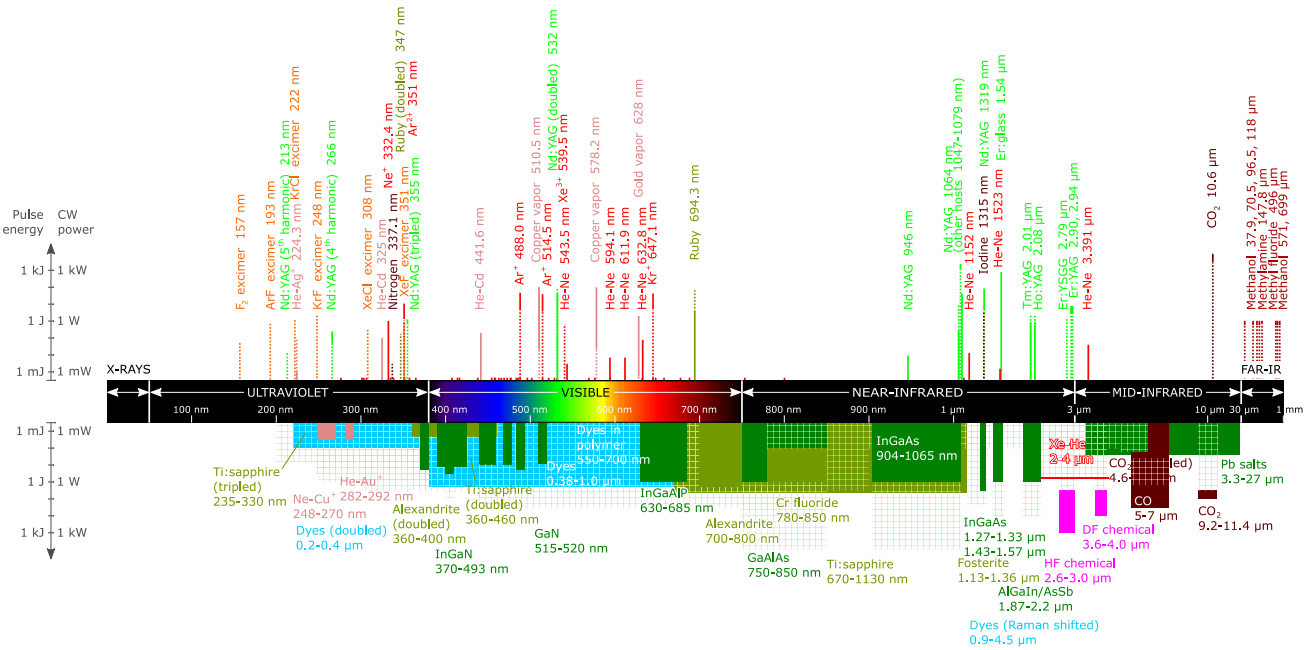

Figure 431: The great variety of lasers covering the electromagnetic spectrum from ultraviolet to mid-infrared waves. Source: Wikipedia.

is a spin-off from the Center of optics, photonics and laser (COPL) in Quebec City.

FocusLight Technologies

China, 2007

FocusLight Technologies produces laser diodes and laser optics components.

Freedom Photonics

USA, 2005-2022

Freedom Photonics develops semiconductor lasers and photonic components, including InP- and GaAs-based devices. It was acquired by **Luminar** in 2022 as part of Luminar Semiconductor. Quantum Computing Inc. acquired Luminar Semiconductor in February 2026, so Freedom Photonics is now part of QCi.

GLOphotonics

France, 2011

GLOphotonics sells hollow-core photonic crystal fiber (HC-PCF) and their functionalized form Photonic Microcells (PMC).

These fiber and gas-photonics products use proprietary hollow-core photonic-crystal-fiber technology. The company works with the CNRS XLIM laboratory in Limoges.

iPronics

Spain, 2019

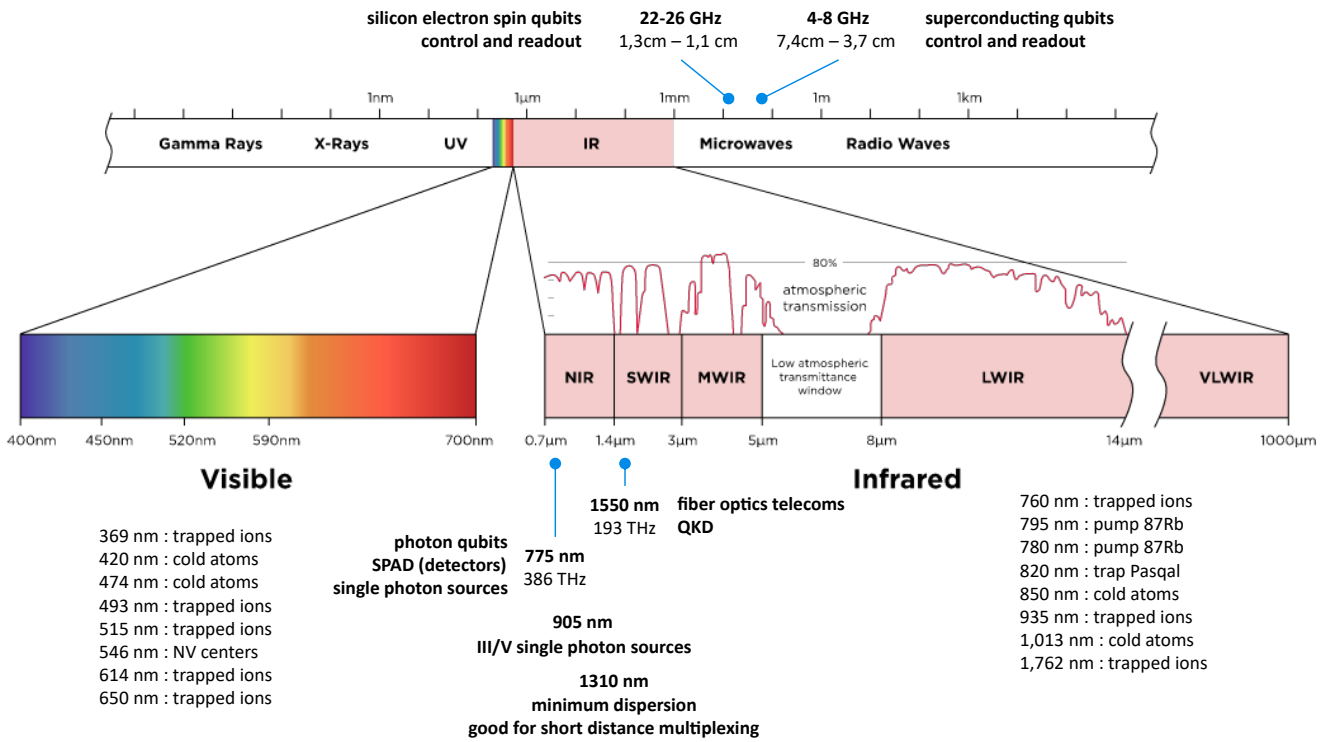

Figure 432: Representative wavelengths used in quantum technologies. Source: Infiniti Optics, multi-sensor technology page.

iPronics develops general-purpose integrated programmable photonic systems, where optical hardware complements software to perform multiple functions.

Lumibird

France, 1997

Lumibird is a supplier of solid-state, diode and fiber lasers. The current group traces its creation to Keopsys in 1997 and incorporated Quantel through a 2017 merger. It reported more than 1,000 employees and revenue of €225.6M for the 2025 financial year, as published by the company.

Q.ANT

Germany, 2018, €68M

Q.ANT has a product line organized in four segments: particle metrology, atomic gyroscope, magnetic sensing and photonic computing.

Q.ANT, a subsidiary of the TRUMPF Group, develops photonic technologies for sensing and computing, including green-laser subsystems for NV-center sensing and thin-film lithium-niobate photonic circuits. Its photonic-computing platform uses waveguides, Mach-Zehnder interferometers, electro-optic modulation and related integrated optical components. High-power laser systems used in semiconductor lithography belong to the broader TRUMPF group rather than to Q.ANT itself.

They lead a related German consortium with €50M in funding, including €42M of public funding from the German government.

Quantum Pulse Ventures

Israel, 2021

Quantum Pulse Ventures (QPV) is a company created by Ofer Shapiro (CEO), Haim Suchowski (Chief Architect), and Yaron Oz (CSO) that develops a composite pulse driven directional coupler, the basic building block used in state preparation, gates, and readout across photonic quantum computing or quantum routing platforms. It reuses composite pulse sequencing from NMR/MRI physics and applies it to segmented waveguide couplers, making them tolerant to fabrication error without changing the underlying silicon photonics, silicon nitride, or lithium niobate process. They reported in 2025 a high-fidelity but still probabilistic CNOT gate implemented with their technology, with the fidelity and success probability holding for the device and operating conditions described in that work [3388].

Silentsys

France, 2021

SilentSys develops optical frequency-discrimination and laser-stabilization systems. Its OFD converts input-laser frequency fluctuations into an electrical error signal that can drive a feedback servo. The discriminator is based on stabilized fiber interferometers, including modified Michelson or Mach-Zehnder configurations, and the company reports frequency-noise reduction exceeding 60 dB

in suitable setups, reaching Hz-level linewidth from MHz-level input linewidth. These are company figures rather than peer-reviewed results, and a stabilization claim should state the input linewidth, the output linewidth, the measurement time and the noise conditions under which it was obtained.

Skylark Lasers

UK, 2013, £4.1M

Skylark Lasers, formerly UniKLasers (until 2022) develops narrow-linewidth, single-frequency diode-pumped solid-state lasers at wavelengths selected for precision spectroscopy, quantum sensing and related applications.

Stable Laser Systems

USA, 2009

Stable Laser Systems offers ultrastable Fabry-Pérot reference cavities and laser-stabilization systems used in precision spectroscopy, atomic clocks and cold-atom experiments. The Boulder-based company was founded by Mark Notcutt, whose earlier JILA work with Long-Sheng Ma, Jun Ye and John L. Hall demonstrated a compact reference-cavity system supporting a 1 Hz laser linewidth [3389]. John L. Hall shared the 2005 Nobel Prize in Physics for contributions to laser-based precision spectroscopy, including the optical frequency-comb technique.

Figure 433: Stable Laser cavities. Source: Stable Laser Systems.

Toptica Photonics

Germany, 1998

Toptica Photonics develops high-end laser systems for scientific and industrial applications, including tunable diode lasers, ultrafast fiber lasers, terahertz systems and frequency combs (Figure 434). Its narrow-linewidth and frequency-stabilized lasers cover many wavelengths used for cooling, trapping and manipulating neutral atoms and trapped ions.

Toptica also supplies frequency-comb and metrology systems, including components used in optical-clock platforms. As of September 2026 the group reports about 600 employees and consolidated revenue of about €140M. I visited the company in October 2024 near Munich, meeting Wilhelm Kaenders, cofounder and member of the executive board.

Vescent Technologies

USA, 2002, $6.5M

Vescent Technologies, formerly Vescent Photonics, created an optical frequency comb, the RUBRIComb, which is used to tune quantum computers, act as a clock oscillator, or for dual-comb spectroscopy, and enable ultra-precise remote sensing. They also master the laser-based technique used for atom cooling, propose a 1,542 nm stabilized laser, many laser controllers and power supplies, and various other laser accessories.

Vexlum

Finland, 2017, €12.4M

Vexlum produces high-power narrow-linewidth vertical external-cavity surface-emitting lasers (VECSELs) including blue and UV lasers, used among other things, to control trapped beryllium ions. It is a spinoff from Tampere University of Technology Optoelectronics Research Centre (ORC).

And also: **Spectra Physics** (1961,USA), **Alpes Lasers** (1994, Switzerland) which sell infrared quantum cascade lasers, **Altitun** (1997, Sweden, $10M), **Ampliconyx** (2016, Finland who manufactures short-pulses lasers), **Amplitude Laser Group** (2001, France) and their femtosecond lasers, **Active Fiber Systems** (2009, Germany) which creates femtoseconds fiber lasers and is a spin-off from Fraunhofer IOF, **Calmar Laser** (1996, USA), **FISBA** (1957, USA) which develops multi-wavelengths lasers, **HUBNER Photonics** which produces solid state tunable lasers, **InnoLume** (2002, Germany, $26.8M, which sells laser diodes), **Intense Photonics** (1994, USA, $51M, which develops single and multi-mode monolithic laser array products, and high power laser diodes and was acquired by Orix Group), **Lytid** (2015, France) which manufactures terahertz cascade lasers, **Spark Lasers** (2015, France) and their picosecond and femtosecond lasers, **mirSense** (2015, France) with its quantum cascade lasers, **MKS Newport** which sells lasers and other photonic components used particularly with trapped ions and cold atoms quantum computing, **Luna Innovations** (1990, USA, $13.1M), **neoLASE** (2007, Germany) a supplier of various laser products including laser amplifiers, **OEwaves** (2000, USA, $15M) which provides ultra-narrow linewidth lasers, oscillators and optical/RF tests and measurement systems. **Prenishq** (2024, India) with diode-laser systems, and **Vector Photonics** (2020, UK, £1.6M) is a spin-off from the University of Glasgow which develops semiconductor lasers based on PCSELs (Photonic Crystal Surface Emitting Lasers).

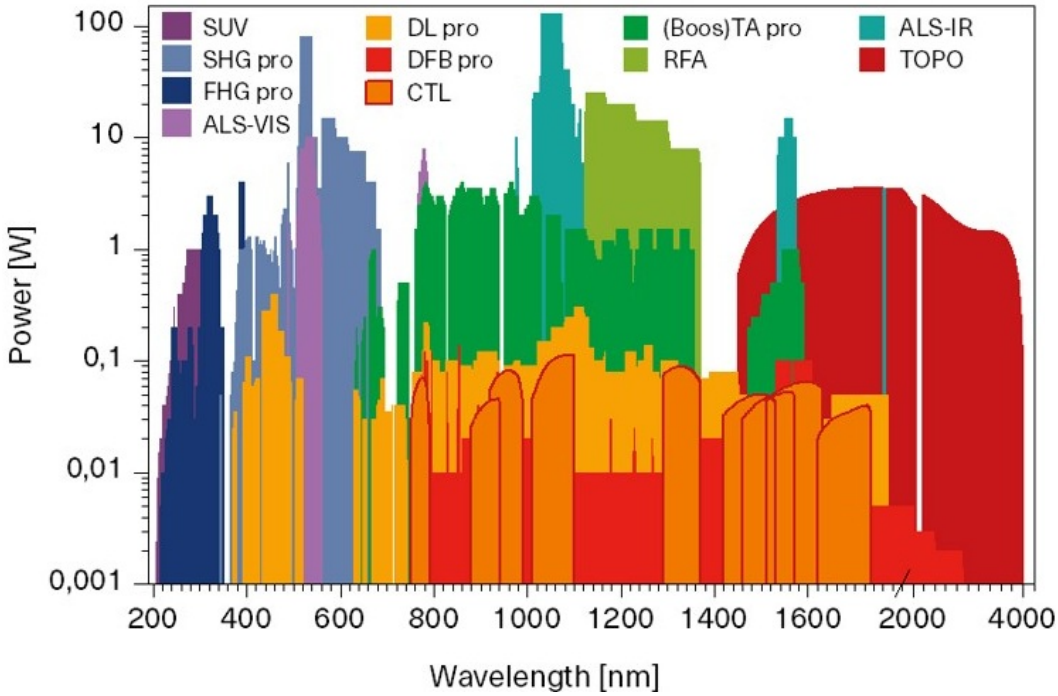

Figure 434: Wavelengths coverage of Toptica lasers, from 190 nm to 4,000 nm, and with power from 1 mW to 10 W, at single frequency, narrow linewidth and high coherence. Source: Toptica.

2.3.2 Single photon sources

Single-photon sources are key components for many quantum-photonic applications, particularly quantum computing and quantum communications.

Comparing single-photon sources is difficult. The metrics below determine whether a source is useful in a quantum-photonic processor. These numbers are not interchangeable percentages. Reported best values must always be read together with the excitation protocol, the collection plane at which efficiency is defined, polarization filtering, background correction, the delay and repetition rate used for indistinguishability, whether the quantity was measured or inferred, and whether the device is a laboratory prototype or a packaged source [3390]. In particular, $g^{(2)}(0)$ and $1-g^{(2)}(0)$ are different quantities and are kept distinct below, as are extraction efficiency into the collection mode, first-lens brightness and overall system efficiency.

- **Single-photon character or multiphoton suppression**, commonly characterized by $g^{(2)}(0)$, which we explain in the Photon quantum numbers subsection in Quantum 101. The quantity $1-g^{(2)}(0)$ is often informally called "single-photon purity". A raw $g^{(2)}(0) = (7.5 \pm 1.6) \times 10^{-5}$ was demonstrated with a GaAs/AlGaAs quantum dot [3391]. Bright cavity sources commonly trade some multiphoton suppression for brightness. The 2025 C2N/Quandela packaged source reported $g^{(2)}(0) = 1.3\%$ [3392].

- **Indistinguishability at short delay**, quantified by a Hong-Ou-Mandel visibility or an inferred mean wavepacket overlap M_s. It strongly affects the fidelity of interference-based photonic operations. C2N reported 0.9956 ± 0.0045 with $g^{(2)}(0) = 0.0028 \pm 0.0012$ in an electrically controlled micropillar, where biasing stabilizes the charge environment and strongly reduces charge-noise-induced dephasing [3393]. Other high-efficiency devices report values around 0.985 [98, 3394].

- **Indistinguishability over long photon trains**, the relevant quantity when using temporal demultiplexing where photons separated by hundreds of nanoseconds must then interfere. Quandela reported about 94% flat out to 1 μs on the Ascella processor in 2024 [50], and 97.5% average visibility has been maintained over trains of thousands of photons in an open microcavity in 2021 by Richard J. Warburton in Basel [2600]. The earlier C2N 2016 benchmark was 88% at 463 ns after 39 emitted photons [3395].

- **Remote-source indistinguishability**, a demanding metric when two independent emitters sit in uncorrelated noise environments. A 2026 C2N/Quandela preprint reports $88 \pm 1\%$ interference visibility between two distant quantum-dot-cavity devices, close to the upper bound set by the intrinsic single-source indistinguishability [2855]. The same teams previously reported 44 to 69% across four source pairs in a peer-reviewed 2025 study [3396].

- **Extraction efficiency into the collection mode**, since photon loss is the dominant error in linear optical quantum computing. The highest value reported as of September 2026 is 80.6% for an InAs dot in a tunable open microcavity [98], against 65 to 80%

for micropillar cavities, obtained in China's Jian-Wei Pan's team.

- **Polarized first-lens brightness**. Half the photons are discarded by cross-polarized laser rejection unless the excitation scheme avoids it. Phonon-assisted excitation of a linear dipole gives 0.50 ± 0.01 with a purity of 0.954 and $M_s = 0.909$ at C2N/Quandela in 2021 [3397], while polarization-selective Purcell cavities give a polarized efficiency of 0.60 with an indistinguishability of 0.975 in China in 2019 [3398].

- **Overall system efficiency** from the emitted source photon to the defined system output is critical because optical loss compounds rapidly with photon number. Ding et al. reported 0.712(18) together with $1 - g^{(2)}(0) = 0.9795(6)$ and indistinguishability 0.9856(13) [98]. This exceeded the 2/3 source-efficiency benchmark, which belongs to a specified photon-loss model and to particular fault-tolerant linear-optical constructions rather than to photonic architectures in general, and which does not transfer unchanged to fusion-based or spin-photon architectures.

- **Fibered brightness in a packaged device**, which separates a physics result from a product. A permanently pigtailed source reaches 20.8% fibered brightness with $g^{(2)}(0) = 1.3\%$ and 97.5% indistinguishability, stable over ten hours in one cooldown and across nine thermal cycles at C2N/Quandela in 2025 [3392].

- **Reproducibility and yield** condition industrialization. A 2020 statistical benchmark covered 15 deterministically fabricated sources averaging $92.2 \pm 2.6\%$ indistinguishability, $95.4 \pm 1.5\%$ single-photon character and $13.6 \pm 4.4\%$ first-lens brightness [2587]. A 2026 C2N/Quandela preprint reports fabrication and characterization across thousands of monolithic devices [2854].

- **Photon-number coherence and single-photon Wigner negativity** provide complementary state information that Hong-Ou-Mandel interference alone does not capture. In particular, a source can have high conditional indistinguishability while still suffering the effect of vacuum or other loss. A 2026 C2N/Quandela preprint reports field-quadrature reconstruction, Wigner negativity and high single-photon-state quality on pilot-line devices [2854].

- **Spin-photon entanglement fidelity and rate** are central to deterministic sequential cluster-state generation. C2N and Quandela reported in 2023 two- and three-particle entanglement fidelities of $80 \pm 4\%$ and $63 \pm 5\%$, with photon indistinguishability of $88 \pm 0.5\%$, at rates substantially above earlier work [2732]. A 2026 preprint reports seven-partite spin-multiphoton entanglement and spin coherence extendable to microsecond timescales at low magnetic field [2854]. A separate 2023 experiment in Israel demonstrated longer photonic strings from a hole-spin emitter, with lower per-photon quality [3399].

- **Multiphoton scaling in practice**, with a reported 40-photon event observed at an event rate of 1.67 mHz under the stated source and detection conditions, together with 1.89(14) dB intensity squeezing [98]. For a Quandela processor, six-photon sampling at 4 Hz was sustained over weeks [50].

- **Telecom-band support** can avoid lossy wavelength conversion in fiber networks. A 2026 preprint reports a deterministic C-band cluster-state source with at least 83% photon indistinguishability and a process fidelity of 0.71 ± 0.01 [3400]. Current telecom-band quantum-dot devices generally lag the best near-930-nm devices in combined brightness and indistinguishability.

- **Operating temperature and clock rate**. High-performance III-V quantum-dot sources commonly operate at a few kelvin in closed-cycle cryostats. Device excitation can run from tens of megahertz into the gigahertz regime depending on the source and protocol [3401]. The 2025 fibre-pigtailed C2N/Quandela device delivered single photons at 16.7(5) MHz at 2.4 K [3392].

No single-photon source simultaneously optimizes all of these metrics. For example, the 2016 near-unity-indistinguishability device had a measured brightness of 0.154 ± 0.015 [3393], the 2025 71.2% system-efficiency result used a tunable open microcavity [98], while the 2026 C2N/Quandela preprint emphasizes reproducibility and scale across many devices rather than a single peak metric [2854].

Quandela

France, 2017, €67.5M

Quandela initially specialized in laser-driven quantum-dot sources of indistinguishable single photons. From 2020 onward, the company expanded into photonic quantum computing.

Quandela's leadership includes Niccolo Somaschi (CEO), Valérian Giesz (COO), an Institut d'Optique engineer with a PhD in photonics [3402], and Pascale Senellart (CSO), a CNRS research director at C2N, Université Paris-Saclay. The company had a staff of more than 140 people as of mid-2026 and international customers, mainly in Europe and Asia. The team also includes Shane Mansfield, Director of Research for theory, algorithms and software, Jean Senellart (CPO), Alberto Peruzzo working on FTQC architecture, and Xavier Pereira (Chief Growth Officer).

Quandela's single-photon sources use self-assembled InGaAs semiconductor quantum dots, often described as artificial atoms because three-dimensional carrier confinement produces discrete optical transitions [3390]. The dot is embedded in a semiconductor microcavity with distributed Bragg reflectors, which enhances

emission into a useful optical mode through the Purcell effect. In the 2025 fibre-pigtailed C2N/Quandela device, the planar cavity used 20 top and 40 bottom $GaAs/Al_{0.95}Ga_{0.05}As$ Bragg-reflector pairs and operated near 930 nm [3392] (Figure 435).

Under resonant excitation, a laser pulse coherently drives a selected quantum-dot transition. Single-photon emission results from the discrete few-particle level structure, saturation and photon antibunching, together with the excitation protocol. The exciton X and biexciton XX transitions are separated by the biexciton binding energy, which is useful for spectrally addressing particular transitions and for exciton-biexciton photon-pair schemes [3390].

Polarization selection rules depend on the total angular momentum of the electron-hole or trion state and on the magnetic-field geometry, so the correspondence is more subtle than "spin-up emits right-circular polarization". In a charged quantum dot, a resident electron spin can serve as a matter qubit. Optical transitions to a trion state then provide spin-selective photon emission, while a transverse magnetic field can produce Larmor precession between successive optical excitations. This spin-photon interface is the basis of sequential spin-multiphoton entanglement schemes which can enable FBQC architectures [2732]. Electrical gating through a diode structure stabilizes the charge state and tunes the optical transition through the DC Stark effect. The resident carrier is deliberately maintained during an experimental sequence, but not literally "trapped forever".

Quantum dots are bright on-demand photon sources and their sequential output can be actively demultiplexed into several spatial or temporal modes for multi-photon experiments. Phonon-assisted excitation can improve robustness and polarized brightness in suitable cavity designs [3403]. The 2025 fiber-pigtailed C2N/Quandela source reported 20.8% brightness at the output fibre, 97.5% indistinguishability and a single-photon emission rate of 16.7(5) MHz [3392].

The next goal is to create large cluster states of entangled photons, because several techniques are being investigated (spin-photon entanglement mechanism [2858, 3404], photon number entanglement [3405], frequency-bin entanglement, etc.). They work on the generation of cluster states as part of the European Union FET Open Qluster project (2019-2023). But the current focus is more on spin-photon entanglement, for the enablement of the SPOQC architecture where the quantum dots are the data qubits and the photons mediate two-qubit gates.

Quandela has also worked on single-photon sources at telecom wavelengths in the ParisRegionQCI project, led by Orange, whose objective includes QKD fiber links between Paris and Université Paris-Saclay.

High-performance InGaAs quantum-dot sources commonly operate at a few kelvins in closed-cycle cryocoolers. The 2025 fibre-pigtailed C2N/Quandela device was integrated in a compact AttoCube two-stage Gifford-McMahon cryocooler operating at 2.4 K [3392]. Research is also pushing quantum-dot operation toward higher temperatures. A 2026 preprint investigates GaAs quantum dots for operation compatible with Stirling coolers around 30 K [3406]. The achievable indistinguishability depends strongly on phonon coupling, cavity enhancement and device design.

Quandela launched a compact integrated single-photon-source system named Prometheus. Permanent fibre pigtailing removes repeated free-space fibre alignment at the user level. The peer-reviewed 2025 C2N/Quandela work demonstrated nanometre-scale source-to-fibre alignment that remained stable through operation and repeated thermal cycles [3392].

The pulse tube of the cryostat is also integrated in the rack, the compressor being outside and water-cooled at first. Eventually, it will be integrated into the rack and cooled by air. The rack was designed by **Pentagram**, the same British designer that IBM used for the Q System One launched in January 2019. It is 1.75 m high and 80 cm wide. The whole system draws about 5 to 6 kW as of the 2026 configuration, the bulk of it coming from the cryostat. Moving the compressor into the rack and switching to air cooling is a plan rather than the present configuration.

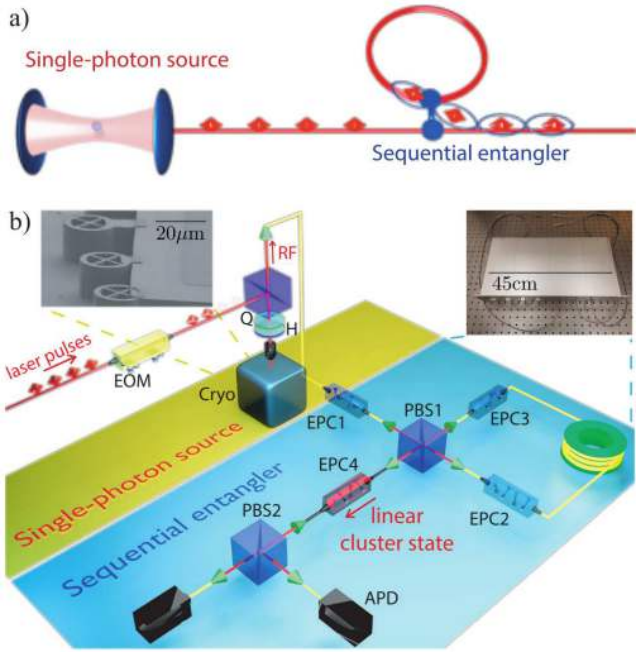

Figure 437: Creation of cluster-state photons with a sequential entangler using a delay line. Source: [3408].

Quandela and C2N collaborate with research laboratories on advanced photonic platforms. In 2020, with the **Hebrew University of Jerusalem**, they demonstrated polarization-encoded linear cluster states of up to four photons from a quantum-dot source using a sequential entangling gate in a fibre loop [3408]. The architecture is relevant to measurement-based quantum

How are Quandela's quantum dots manufactured?

Quandela's quantum dots form randomly during a Stranski-Krastanov epitaxial growth during molecular beam epitaxy (MBE) on a 2 inch III/V GaAs wafer. Their positions are unpredictable, with a typical areal density of roughly 1-100 quantum dots per μm^2. The nucleation sites of these QD islands are determined by atomic-scale surface fluctuations (step edges, defects, local strain variations) that are random and uncontrollable at the wafer scale. The fabrication sequence starts with growing the wafer with randomly positioned QDs. The dots are then located at 4 K using photoluminescence imaging and fine scanning under a focused laser, determining each dot position to 50 nm accuracy [3390]. Then, the wafer is exposed with a cryogenic resist at each QD location. At room temperature, a second lithography step defines the micropillar shape centered on each located QD, with the pillar diameter tuned to bring the cavity mode into resonance with that specific QD. The pillars are etched and metal contacts are deposited.

The devices have a diode structure: the planar cavity heterostructure contains AlGaAs stacked Bragg reflectors with the active region doped to form a p-i-n diode with an undoped intrinsic semiconductor region sitting between a p-type semiconductor and an n-type semiconductor region. The diode stabilizes the charge state through Coulomb blockade, and a bias voltage tunes the optical transition through the DC Stark effect. Quandela's wavelength is about 930 nm [3407]. So, in total, the chip has typically two metal layers, one on each side of the quantum dot structure.

Deterministic fabrication aligns the micropillar cavity to a pre-characterized quantum dot, while later fibre-pigtailing aligns the selected cavity mode to a single-mode fibre with nanometre-scale precision [3392, 3393] (Figure 436).

Growth is therefore random while device fabrication is deterministic: the cavity is aligned to a dot whose position and wavelength were measured beforehand, and only the dots meeting the selection criteria become devices. In 2026, Quandela reported fabrication and characterization across thousands of monolithic devices on a pilot line, including several addressable quantum-dot devices on a single chip. What was demonstrated is device yield and per-device optical quality at that scale, not a multiqubit processor operated on one chip [2854].

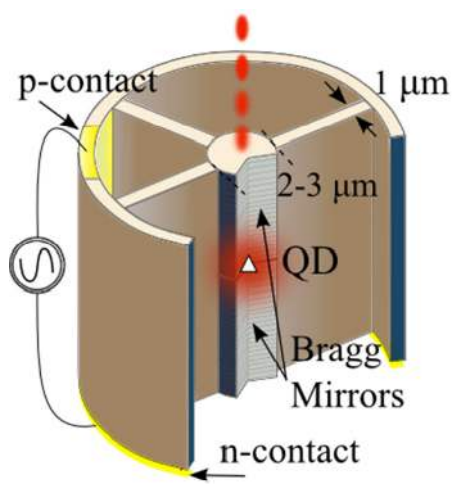

Figure 435: Quandela's quantum-dot single-photon source design with about 20 top and 40 bottom $GaAs/Al_{0.95}Ga_{0.05}As$ Bragg-reflector pairs. Source: [3393].

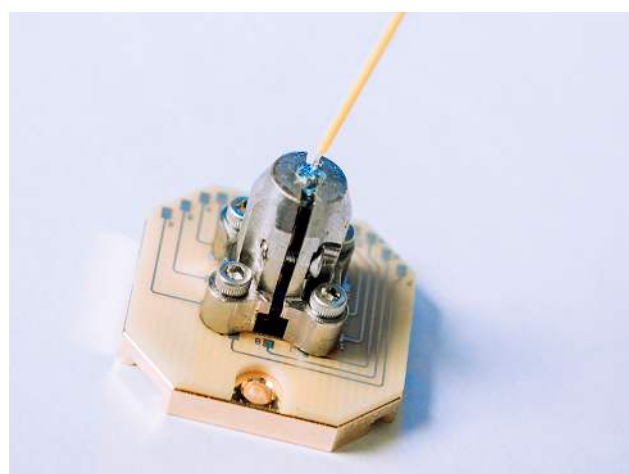

Figure 436: Quandela's pigtail mount attaching an optical fiber to the chip containing a single quantum dot. Source: Quandela.

computing because the same emitter-and-delay principle can in principle generate longer photonic cluster states.

In Europe, they collaborate mainly with **Fabio Sciarrino**'s team in Italy, in Spain with **INL** and other teams in Austria, the United Kingdom, Slovakia and Israel. They are part of the European FET project PHOQUSING for boson sampling led by Fabio Sciarrino's team.

In 2019, a C2N/Quandela source was actively demultiplexed into three synchronized photons and interfaced with a reconfigurable laser-written glass tritter circuit, where high-rate three-photon interference was measured (Figure 438) [3409].

Since 2020, Quandela has started working on creating a photon-based quantum computer using their own pho-

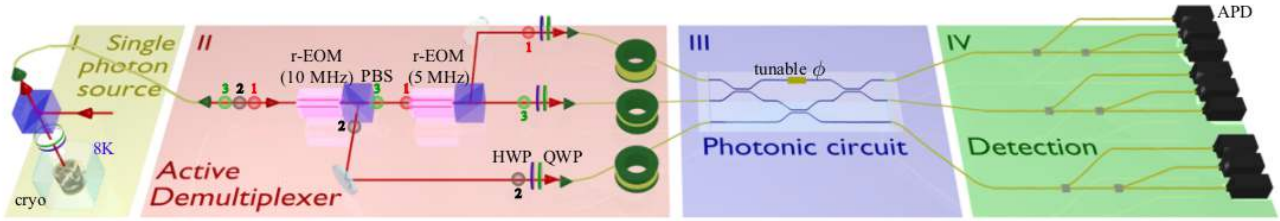

Figure 438: Three-photon interference using an actively demultiplexed quantum-dot source and a reconfigurable glass photonic circuit. Source: [3409].

ton source. We cover this core part of their business in the photonic qubits vendor section.

Sparrow Quantum

Denmark, 2016, $40.1M

Sparrow Quantum is a spin-off from the Niels Bohr photonics research laboratory cofounded by Peter Lodahl. Like Quandela and Qubitekk, they offer single photon sources.

Sparrow Quantum uses InAs quantum dots coupled efficiently to photonic-crystal waveguides. Resonantly excited devices operate in the roughly 920-980 nm range, with reported indistinguishabilities in the mid-to-high 90% range depending on device and conditions. In 2025, the underlying NBI research platform demonstrated a quantum-coherent emitter interface in the telecom O band [3410]. The source can emit sequential single photons at rates of tens of megahertz [3411]. Sparrow sources are integrated into photonic platforms including products from QuiX and ORCA Computing. In 2025, researchers from NBI, the University of Copenhagen and the University of Bristol published a blueprint for low-depth photonic quantum computing with quantum-dot sources [2752]. A September 2026 preprint studied purification protocols for photonic graph states [3412].

2.3.3 Single photon detectors

This part lists only the pure players vendors in this space. Other vendors of single photon detectors are in the other photonic vendors inventory in 2.3.4. Single photon detectors are used in quantum computing and quantum communications.

Photon Spot

USA, 2010

Photon Spot develops nanowire-based single-photon detectors. They have received a DARPA funding of $100K in 2014 and $1.5M in 2015.

Pixel Photonics

Germany, 2020, €1.45M

Pixel Photonics develops single photon detectors (SNSPD) targeting quantum computing, QKD and imaging markets. With HTGF (Germany) and Quantonation (France) as seed investors.

Quantum Opus

USA, 2013

Quantum Opus develops single photon detectors based on superconducting nanowires, the Opus One. The compact version Opus Two is an 8U data center rack-mount package, including cryostat [3413]. The company benefited from US federal funding, including $100K in 2015 and $1.5M in 2015 from DARPA and $125K from NASA in 2018. They are a provider of the Chinese team who did run the Gaussian boson sampling experiment announced in December 2020.

Scontel

Russia, 2004

Scontel offers single photon detectors in the visible and infrared (SSPD, for Superconducting Single Photon Detecting Systems). These detectors are cooled at 2.2 K helium-4 using a Sumitomo SRDK 101 pulse head system with a water-cooled HC-4E compressor.

Single Quantum

the Netherlands, 2012

Single Quantum sells SNSPD systems covering several visible and near-infrared wavelength bands.

Current rack-integrated systems use closed-cycle cryogenic cooling around 2.5 K with an external helium compressor, rather than a liquid-helium bath. Depending on detector configuration and wavelength, the company reports system detection efficiencies around 85–90% or higher and timing jitter in the tens-of-picoseconds range, these two figures not being reached at the same operating point.

An SNSPD consists of an ultrathin superconducting nanowire patterned into a meander. Absorption of a photon can nucleate a resistive hotspot, producing a measurable voltage pulse while the wire is current biased. Modern systems can exceed 90% system detection efficiency at selected wavelengths, typically near 1,550 nm and for an optimized input polarization, with timing jitter down to the order of tens of picoseconds. Such a figure is only meaningful when the system detection

efficiency, the wavelength, the polarization, the count rate, the dark-count rate, the jitter definition and the device-versus-system boundary are reported together, since efficiency, jitter and dark counts trade against each other and against the cryogenic configuration. Single Quantum SNSPD systems are used in quantum sensing, communications and photonic quantum computing.

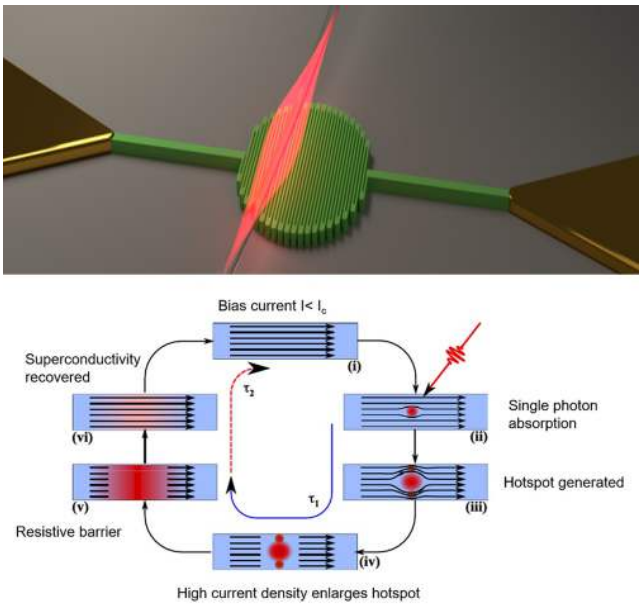

Figure 439: Single Quantum SNSPD photon detector.

g2-zero (2020, Spain) also manufactures single photon detectors.

2.3.4 Other photonics vendors

Let's now look at other photonics equipment manufacturers. They sometimes also manufacture lasers but even more.

Accelink

China, 1976

Accelink sells optoelectronic components, including fiber optics modulation and demodulation systems, lasers and SiO_2/Si material plane optical waveguides. They probably play a role in the deployment of quantum telecommunication networks.

Alcyon Photonics

Spain, 2018, $560K

Alcyon Photonics is a spin-off from IO (Instituto de Óptica) in Spain. Its expertise is in sub-wavelength grating (SWG) technology. They create complex photonic circuits like high-performance Application Specific Photonic Integrated Circuits (APICs). The company was cofounded by the researcher Aitor Villafranca.

AQLS

Germany, 2023

AQLS (*aka* Advanced Quantum Light Sources) is a Berlin-based startup specializing in quantum communication, quantum sensing, and photonic quantum computing, with a focus on high-performance SPDC quantum light sources. The company was created by Janik Wolters, from TU Berlin and DLR. Their main product is PPS-DG, a room temperature photon pair source that generates narrow-band photons at the rubidium D1 line (795 nm). Pairs are produced by cavity-enhanced spontaneous parametric down-conversion (SPDC) in monolithic periodically poled potassium titanyl phosphate (ppKTP) resonators. Their applications range from mobile quantum memory systems to single-photon storage experiments.

Aresis

Slovenia, 2004

Aresis is a manufacturer of high-end laser tweezer systems. These are used in soft matter physics, biophysics, biology and in the field of Bose-Einstein condensates and cold atom physics. Their founders are involved in the creation of Atom QL (Slovenia), which builds a cold atoms based QPU.

Artilux Tech

Taiwan, 2014

Artilux Tech develops GeSi short-wave-infrared sensors. The 2024 Nature paper on its CMOS-compatible room-temperature GeSi SPAD reported a single-photon detection probability of 12% at 1,310 nm, a dark-count-rate density of 19 kHz μm^{-2}, timing jitter of 188 ps and afterpulsing below 1% [3414]. The previously stated 95% efficiency is not reported by that paper.

Aurea Technology

France, 2010

Aurea Technology is a photonics equipment manufacturer targeting various markets including quantum communications (QKD) and quantum sensing.

It sells twin photon sources (TPS), time correlated single photon detectors (Picoxea), ultra-low-noise NIR single-photon counting detection modules (SPD_A and SPD_OEM_NIR), time correlators (Chronoxea) and high-resolution fiber sensors (q-OTDR) and picosecond pulse lasers (Pixea).

The SPD_OEM_NIR is using an InGaAs single photon avalanche diode (SPAD) in the 900 to 1,700 nm wavelength range with very low dark count rate noise (DCR<700 Hz). It is cooled with the Peltier effect. The supported wavelengths make it suitable for photon counting in telecom-wavelength QKD systems (1,550 nm). It also fits into a standard datacenter rack in a 2U package.

They also developed Fluoxea, a fluorescence lifetime imaging mapping system using time-correlated single photon counting that can be used to characterize semiconductors, qualify quantum dots or measure local magnetic fields (with the help of NV centers). The company has its own assembly plant in Besancon, France. It is a spin-off company from the optics department of FEMTO-ST, a public research lab based as well in Besancon.

Azurlight Systems

France, 2010-2023

Azurlight Systems developed high-power laser amplification systems in the visible and near-infrared spectra (from 488 nm to 1,065 nm) using ytterbium-based fibers with low thermal dissipation. These can be used for atom cooling and trapping. The company was acquired by **Toptica** (Germany) in 2023.

Cailabs

France, 2013, $46.2M

Cailabs is a company based in Rennes, France, which is a spin-off from the LKB of ENS Paris and markets photonics equipment and in particular spatial multimode multiplexing systems for optical fibers supporting up to 45 nodes. This is what makes it possible to multiply the speed of the optical fibers of the telecom operators' networks. In particular, they have KDDI (Japan) as a customer. They also develop adaptive optics for satellite communications, including satellite QKD. The startup is managed by Jean-François Morizur (CEO) and Guillaume Labroille (CTO) with Nicolas Treps from LKB being their scientific advisor.

Ephos

Italy, 2022, $8.5M

Ephos is a producer of glass-based photonic chips based in Milano and San Francisco. Its benefit compared to silicon based chips is low losses [3415]. Quandela is one of their customers.

Excelitas

USA, 2010

Excelitas sells various photonics devices including Single-Photon Counting Modules (SPCMs).

Hamamatsu Photonics

Japan, 1953

Hamamatsu Photonics provides silicon photodiodes, electron multipliers for detecting electrons, ions, and charged particles, photon counters, LCoS based spatial Light Modulators (SLM) used for cold atoms controls, laser cooling systems, quantum imaging and image sensors for the detection of neutral atoms, trapped ions and NV centers fluorescence. Hamamatsu acquired NKT Photonics (Denmark) in 2024.

MenloSystems

Germany, 2001

MenloSystems was cofounded by Theodor Hänsch, laureate of the Nobel prize in physics in 2005 as a spin-off of the Max-Planck Institute for Quantum Optics (MPQ) in Garching, near Munich. It was the first company to build optical frequency combs. They also provide terahertz systems and femtosecond lasers, as well as provide optical clocks that are used by companies such as Pasqal or Atom Computing.

Micron-Photons-Devices

Italy, 2004

Micron-Photons-Devices, aka MPD, creates Single Photon Counting Avalanche Diodes, "SPAD", fabricated using custom silicon, standard CMOS and InGaAs/InP technologies. It also sells photon counting based QRNGs.

Miraex

Switzerland, 2019, $6.9M

Miraex has several quantum technologies in its portfolio: photonic based quantum sensors for vibration, acceleration, acoustic, pressure, electrical field and temperature measurement, a microwave to optical photon convertors, and quantum repeaters. It is a spin-off from EPFL.

Mirega

France, 2023

The company was created by Vincent Hardy in the Grenoble region and is using technology coming from the ENS LKB in Paris. They created a fiber-based Fabry-Perot microcavity with extremely high finesse ($F > 100{,}000$) which is used in a tunable fiber Fabry-Perot tunable filter for photonics and telecommunications applications to selectively filter and manipulate specific light wavelengths. Mirega is also developing a compact high sensitivity miniaturized gas analyzer.

Photon Queue

USA, 2024, $4.5M

Photon Queue is a spin-out of Paul Kwiat's lab from the University of Illinois Urbana-Champaign. It was cofounded by Nathan Arnold (CEO), Colin Lualdi, Kelsey Ortiz, Kai Shinbrough, and Paul (scientific advisor). Their product is a room-temperature free-space all-optical photonic quantum memory that stores single photons by circulating them in low-loss free-space optical loops built from proprietary high-reflectivity mirror systems and fast optical switches. It was first deployed at Sandia National Laboratories and the University of Maryland. The caveat is with the photon loss during their roundtrip in the loops [3416]. It could be used

in QKD repeaters, quantum computing photonics and quantum processor interconnect.

PINC Technologies

USA, 2023, $6.8M

PINC Technologies is a Caltech spin-out developing integrated nonlinear photonic devices and circuits. Its NanoPPLN platform provides an extensive library of nonlinear photonic circuits on periodically poled thin-film lithium niobate. Their circuits enable a wide range of up- and down-conversion processes across the UV (350 nm [3417]) to mid-infrared (5 μm [3418]) spectra. They are used with OPO (optical parametric oscillator), SPDC (spontaneous parametric down-conversion) and OPA (optical parametric amplification, [3419]).

Qlibri

Germany, 2022

Qlibri is a spin-out from the group of Nobel prize laureate Theodor W. Hänsch at LMU Munich and the Max-Planck-Institute of Quantum Optics, cofounded by Michael Fög, Thomas Hümmer, Jonathan Noé, and Manuel Nutz. It develops optical micro-cavities (Figure 440) and high-reflectivity fiber-based microcavity mirrors with laser-machined concave profiles and dielectric coatings. These are used in absorption microscopy and quantum technologies.

Figure 440: Qlibri optical micro-cavity. Source: Qlibri, 2025.

Qlibri also developed a raster-scanning absorption microscope for the detection and quantitative characterization of nanoscale particles, low-dimensional materials, thin films, and defects in vacuum, air, and liquid environments. Their components are used in quantum computation and single-photon sources. It can be used to sample inhomogeneous nanosystems like quantum dots, NV-centers, or 2D-Materials. They also developed a Helmholtz coil upgrade which generates hundred-millitesla magnetic fields perpendicular to the resonator axis.

Quan2D Technologies

India, 2022

Quan2D Technologies develops SNSPDs used in quantum communications. They also produce 2D nanosheets.

Quanastra Technologies

India, 2025

Quanastra also develops SNSPD, as well as Low Noise Amplifiers (LNA).

Qontrol Systems

UK, 2016

Qontrol Systems develops photonics components including photonics device status readout modules and backplanes (boards) on which several of these modules can be installed. These modules drive photonics devices via a 12V voltage and read signals with 18-bit accuracy. This is control electronics.

Scintil Photonics

France, 2018

Scintil Photonics develops mixed silicon and III/V photonic components, using their BackSide-on-BOX process, that mixes active and passive optical components. Their technique bonds InP/III-V dies on the backside of processed Silicon-On-Insulators (SOI) wafers, only where it is needed. Their fabrication process is classical CMOS. Their components integrate lasers (WDM laser arrays and tunable lasers), modulators, waveguides, wavelength filters, surface fiber couplers, semiconductor optical amplifiers (SOA), and photodetectors.

Teem photonics

France, 1998

Teem photonics creates lasers and integrated photonics components including erbium doped waveguide amplifiers and arrayed-waveguide gratings. Not the same AWGs as the arbitrary waveform generators used to control solid-state qubits, although these can be used for signal multiplexing/demultiplexing.

VLC Photonics

Spain, 2011-2020

VLC Photonics produces photonics equipment and fabless design of photonic integrated circuits. The company is involved in European Flagship projects. It is a spin-off of the University of Valencia. The company was founded by Iñigo Artundo, Pascual Muñoz, José Capmany and José David Domenech. They also market technical reports at prices ranging from €4K to €5.4K per piece.

The company was acquired by Hitachi High Tech in 2020.

And...

Andor (1989-2014, UK) is a branch of Oxford Instruments which manufactures CCD and CMOS imagers used for example for qubit readout with cold atoms QPUs.

BluGlass (2006, Australia) which manufactures gallium nitride (GaN) blue laser diodes.

Covesion (2009, UK) develops laser frequency conversions devices that are used in many quantum optics applications. It is a spin-off from the University of Southampton [3420].

Exosens (2023, France, the Netherlands) owns the Photonis brand and supplies photocathode- and microchannel-plate-based photon detectors. Photonis advertises more than 95% *microchannel-plate collection efficiency* for some detector architectures.

ICON Photonics (2018, France) offers optical coupling and packaging solutions for high-speed optical communications using 3D wafer-level polymer optical beam shaping. It can be used for the development of quantum communications and quantum computing solutions.

Liquid Instruments (2014, Australia) is a photonic equipment manufacturer. Their offering contains a 4-channel time and frequency analyzer that can detect individual photon events, generate time interval statistics, and determine correlation functions between channels, with zero dead time. It can be used in many fields like quantum metrology [3421].

M Squared (2006-2025, UK) developed lasers and systems for cold-atom interferometry and quantum technologies. The company ceased trading and entered administration in August 2025. Its assets and intellectual property were subsequently sold to Novacene Photonics in November 2025.

Monarch Quantum (2026, USA) is a startup developing advanced photonics-based control systems for cold atom control. Their first partner is Oratomic.

Meadowlark optics (1989, USA) is a provider of a wealth of optical elements, including SLMs like the ODPDM512.

Micro Align (2019, the Netherlands, €1M) is a provider of fiber arrays that are used in quantum photonic computing like in Quandela's QPUs to align photon sources and fibers. It is a spin-off from Eindhoven University of Technology.

Nüvü Cameras (2010, Canada) sells EMCCD high sensitivity cameras with spatial resolution up to 512×512 pixels. They can be used for the detection of cold atoms. Infleqtion is one of their customers.

Munich Quantum Instruments (2021, Germany) creates single photon detectors.

Muquans/Exail (France) is also a provider of laser and intelligent frequency tunable lasers, laser frequency doublers and narrow-linewidth lasers used in various quantum technologies. Particularly with its subsidiary Leukos.

Photon Force (2015, UK) creates single-photon cameras of 32×32 pixels. It can be used in various photonic based quantum sensing applications. It enables time-tagging of incoming photons with a time resolution of 55 picoseconds.

Photonscore (2017, Germany) provides the LINCam, a 1000×1000-pixel CCD camera with single photon counting feature, with a 100% fill-factor and minimal noise.

Photec (2023, Italy) provides SNSPDs with an efficiency reaching 98% and low dark count.

Quantum Composers (1993, USA) provides GaAs laser systems and precision pulse generator instrument lines.

Quintessent (2019, USA, $11.5M) is a developer of heterogeneous silicon photonics and quantum dot laser technology.

Q-Block Computing (2020, Canada) is a quantum hardware startup who created an ultrastable laser, a photon detector, an optical modulator, some form of quantum memory, and a quantum clock.

Redback Systems (2019, Australia) is a spin-out from Macquarie University created by Matt van Breugel (CEO), Tobias Feger (CTO) and Lachlan Rogers (CSO), that sells high-resolution optical spectrometers using cooled CMOS sensors. They are used by Quandela and QuiX.

UQDevices (Canada) develops time correlation measurement devices for photons covering the field of time-correlated single photon counting (TCSPC).

We also have **Amsterdam Scientific Instruments** (2011, the Netherlands) and their various photon and electron sensors, **Ibsen Photonics** (1991, Denmark) which provides spectrometers and various photonic equipment, **Lumiphase** (2020, Switzerland) which develops optical modulators, **Bay Photonics** (2007, UK) which provides photonic circuits assembly and packaging, **Qubig** (2008, Germany) which develops light modulators (amplitude and phase modulators, phase shifters, Pockels cells) that can be used in quantum computing or communications, **Menhir Photonics** (2018, Switzerland) which create femtolasers, **Oxxius** (2002, France) which develops visible and near diode based UV lasers, and **Photek** (1991, UK) with its photon and imaging detectors.

2.3.5 Bibliography and notes

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2.4 Fabs and manufacturing tools

Many quantum technologies components are nanofabrication based and must be manufactured somewhere. It is the case with superconducting qubits, superconducting electronics, quantum-dots based electron spin qubit circuits, quantum nanophotonic circuits, NV center based qubits and sensors, single-photon generating quantum dots, photon detectors, trapped ions supporting circuits, traveling wave parametric amplifiers and the like. You could wonder how these circuits are manufactured and where. Like your regular smartphone chip processor, is it coming from a giant $20 billion TSMC 5 nm fab in Taiwan? Well, most of the time, no!

2.4.1 Foundries

We are in a very different technology and market realm. Quantum related components have some distinct characteristics compared to mass market semiconductors that you'll find in your TV, smartphone, laptop or tablet. They are very specialized and use sometimes special manufacturing processes and/or materials like III/V semiconductors or niobium/aluminum deposition for superconducting qubits and electronics. They are experimental most of the time with many try/error cycles. They are sometimes manufactured with specialized tools. And finally, they are produced in rather small quantities. Surprisingly, given the experimental nature of many components, the related fabs are usually less impressive in size and cost.

Fabs contain cleanrooms, where the concentration of airborne particles is controlled on top of temperature, humidity and sometimes, other parameters like ambient magnetism and vibrations. Cleanrooms are classified according to the number and size of particles suspended in the atmosphere. Cleanroom ISO classes range from 1 to 9, with an (exponential) increased number of particles per volume unit above fixed size thresholds, 1 being the "cleanest". Most specialized quantum technologies fabs have a less stringent cleanroom class requirement than the most expensive and modern semiconductor fabs, since they are not creating high-density chips at volume. Research fabs may prioritize rapid process iteration over high-volume yield, although yield remains important and is increasingly tracked as devices scale. They are typically class 100 to class 1000 cleanrooms in the older FED-STD-209E scale, namely ISO 5 to ISO 6, although the class varies by facility and by process step. The pre-industry fabs and the largest research fabs remain an exception and run class 10 (ISO 4) areas for their most critical lithography steps.

We can segment quantum technologies fabs in a couple categories as shown in Figure 441:

Research fabs. These are most of the time fabs from national research organization labs and universities. These fabs have cleanrooms with sizes ranging from 100 m^2 to 4,000 m^2. Their teams and the associated researchers are creating the "recipe" of new semiconductor technologies. These fabs usually produce 200 mm or smaller wafers.

North-America with the MIT Lincoln Labs (superconducting electronics and qubits, trapped ions chips, with about 1,680 m^2 of class 10 and class 100 clean rooms in a 90 nm-class 200 mm facility, plus a new 160,000 sq ft Compound Semiconductor Laboratory–Microsystem Integration Facility costing $277M and adding 3,250 m^2 of ISO 4 cleanroom), Princeton (1,350 m^2 cleanroom, silicon and III/V, up to 100 mm wafers), HRLabs in California (all sort of things in a 900 m^2 clean room), UCSB Nanofab (1,170 m^2, superconducting qubits, MEMS, photonics, imaging sensors), Harvard CNS (966 m^2), Yale University (108 m^2, superconducting qubits), Stanford (180 m^2, various quantum techs), NIST NanoFab (1,800 m^2 cleanroom), DoE Argonne Quantum Foundry (500 m^2) and Fermilab SQMS Center, the Fermilab Quantum Computing Lab Two, University of Chicago (890 m^2, Pritzker Nanofabrication facility), the National Quantum Nanofab (NQN) at the University of Colorado (focused on photonics, with a $20M funding by NSF in 2024) and the University of Waterloo Quantum Nano Fabrication and Characterization Facility (600 m^2).

Europe with VTT in Finland (2,600 m^2 cleanroom for 150 and 200 mm wafers, superconducting qubits and electronics, photonics), DTU Nanofab in Denmark (1,350 m^2), the superconducting Royal Holloway cleanroom in the UK (350 m^2), CNRS C2N (2,900 m^2 clean room near Paris, photon quantum dots sources in GaAs, polaritons circuits, TWPAs, etc), CNRS Institut Néel (220 m^2, near Grenoble, superconducting electronics and qubits, graphene, diamonds growth [3422]), Van Leeuwenhoek Lab at TU Delft (3,500 m^2 cleanroom used by QuTech and TNO in The Netherlands), MyFab (Sweden), Fraunhofer IPM (400 m^2 clean room in Freiburg, various optical quantum sensors), Fraunhofer IPMS near Dresden (200 mm wafers, 1,500 m^2 cleanroom) and also PTB, Leibniz IPHT and Jülich in Germany, PoliFAB from Politecnico di Milano which created an interferometer used by Pascale Senellart's team to demonstrate the indistinguishability of photon clusters [3423], ISTA Nanofabrication Facility in Austria (450 m^2), EPFL and ETH Zurich in Switzerland and the UK National Epitaxy Facility.

Asia-Pacific with RIKEN and AIST (superconducting electronics, but also a strong CMOS 300 mm manufacturing capacity) in Japan, UNSW in Australia and the Shanghai Institute of Microsystem And Information Technology (SIMIT) has also its own fab.

Pre-industry research fabs. These are the likes of IMEC (Belgium) and CEA-Leti (France) who create new semiconductor components and design new manufacturing processes before they are volume-produced in commercial fabs. These are larger fabs than the aforementioned research fabs. CEA-Leti operates 11,000 m^2 of cleanrooms in Grenoble. IMEC cleanrooms totals 12,000 m^2 in Leuven, Belgium. CEA-Leti produces sili-

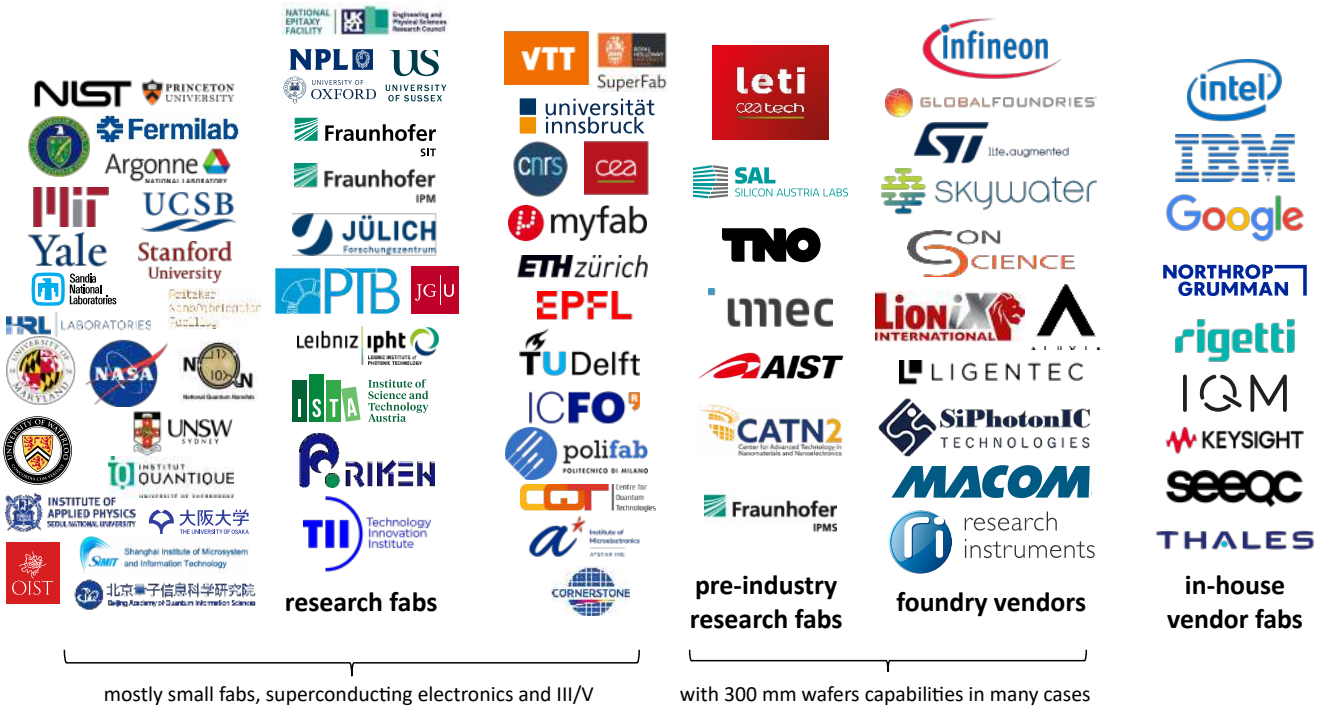


Figure 441: Research and industry cleanrooms fabricating semiconductors for quantum use cases. Olivier Ezratty, 2022-2026.

con qubits wafers for its own usage as well as for vendors like Quantum Motion (UK). These fabs produce wafers up to 300 mm.

Likewise, the Center for Advanced Technology in Nanomaterials and Nanoelectronics (CATN2) from SUNY Polytechnic Institute in New York State has a cleanroom of 12,000 m^2 producing 200 mm and 300 mm wafers for AI, photonics, CMOS spin qubits, superconducting qubits and digital electronics.

Foundry vendors. These are independent foundries manufacturing semiconductors for third parties. GlobalFoundries manufactures nanophotonic chips for PsiQuantum and Xanadu in Malta, New-York State in their 41,400 m^2 clean room on top of classical CMOS chips like the IBM Power processors. Infineon's Villach fab in Austria manufactures trapped ions chips in its 23,000 m^2 cleanroom for Oxford Ionics [3424, 3425]. In Germany, Infineon is an industry partner of many other projects with superconducting qubits, silicon qubits, ion traps, qubit control electronics and NV centers qubits and sensing [3426]. In the USA, SkyWater is the largest foundry for superconducting electronics, working among others for D-Wave, on top of working on various space applications and with DARPA. IonQ closed its acquisition of SkyWater in July 2026, which is operating as a wholly owned subsidiary under its own name. Formerly from Cypress Semiconductor, Control Data and VTC, SkyWater consolidates a 7,360 m^2 clean room in Minnesota, another one of 3,300 m^2 in Florida and a 200 mm fab in Austin, Texas acquired from Infineon in 2021, and support 90 nm features geometries on 200 mm wafers.

Lionix in The Netherlands manufactures nanophotonic circuits for its subsidiary QuiX. Aluvia Photonics (2022, the Netherlands) is a spin-off from the University of Twente that manufactures low-loss photonic integrated circuits based on aluminum oxide (AlO_x). SiPhotonIC (2018, Denmark) is a spin-out of the silicon photonics technology developed by DTU Electro. Larger foundries are usually needed for high-density chips, particularly with silicon qubits where patterns are relatively small, down to about 10 nm. MACOM (formerly OMMIC, 2000, France) is a small foundry specialized in manufacturing III-V MMIC (monolithic microwave integrated circuit) which could comprise cryogenic amplifiers used in quantum computing. It was acquired in 2023 for €38.5M by MACOM Technology Solutions (USA), a company specialized in radio, microwave and millimeter wave semiconductors. At last, let's mention Research Instruments Gmbh which manufactures special components for research and industry applications, including some superconducting components used in quantum computing and ConScience AB (Sweden), a clean room fab service with various capabilities including the manufacturing of superconducting chipsets. It proudly announced in September 2023 to have *"delivered its first quantum technology components to a US based quantum computing company"* without any details. In January 2024, it announced the QiB0 device containing 4 qubits and 2 coplanar waveguide (CPW) resonators for testing purposes.

In-house vendor fabs. These are the fabs from quantum technology vendors who are self-sufficient for this respect. Intel manufactures its own quantum dots spin qubits chips in one of its clean rooms at its Hillsboro

facility in Oregon. IBM also has its own manufacturing capacity for superconducting qubits (on 200 mm silicon wafers) and high-density silicon chips with a cleanroom of 3,600 m^2 in Yorktown, New York State.

IBM is also a partner of the Albany NanoTech Complex, which is owned and operated by the non-profit NY CREATES and can manufacture 300 mm wafers in its 16,000 m^2 cleanroom. NY CREATES announced in December 2023 a $10B public/private High-NA EUV Lithography Center, the first publicly owned one in North America, with $9B from industry partners including IBM, Micron, Applied Materials and Tokyo Electron and $1B from Empire State Development. Installation of the ASML High-NA tool, itself owned by NY CREATES, started in 2026 in the new NanoFab Reflection building. It is partnering with Rapidus (2022, Japan) for the development of 2 nm node technology, using nanosheet gate-all-around FET (GAA FET) devices. Rigetti in the USA and IQM in Finland have their own small fabs for their superconducting qubit chips, each reported in the $20 million range. Google has also an in-house fab in Santa Barbara, California. SEEQC has a small 150 mm wafers 200 m^2 cleanroom dedicated to manufacturing superconducting electronics. Keysight also has its own III/V 1,200 m^2 cleanroom, the High Frequency Technology Center (HFTC) in Santa Rosa, California [3427]. Northrop Grumman's fab in Maryland creates 150 mm silicon, SiGe, GaAs, GaN-on-SiC, GaN-on-Si, indium-based nitrides and SiC wafers. Qilimanjaro relies on a fab that was put in place in 2021 at TII in Abu Dhabi. Finally, Thales has an in-house 4,000 m^2 III/V fab with CEA-Leti as a partner.

Having your own fab makes sense when you need to have a fast turnaround and test repetitively many generations of qubit chips. It is relatively affordable for producing superconducting qubits on small wafers.

The USA, European Union and China all want to increase their share, self-reliance and supply security with semiconductor manufacturing. In February 2022, the European Union launched the European Chips Act to "*foster development of capacities in advanced manufacturing, design and system integration as well as cutting-edge industrial production*", with public and private funding of €43 billion until 2030. It includes international partnerships like when Intel is installing a new fab in Germany. The plan contains a provision for quantum technologies, to "*set up advanced technology and engineering capacities for quantum chips in the form of design libraries for quantum chips, pilot lines, and testing and experimentation facilities*". This may provide some additional funding for the extension of the many quantum-related fabs mentioned before.

After the Senate's USICA bill of June 2021 and the House's America COMPETES Act of February 2022, the reconciled CHIPS and Science Act was passed in July 2022 with $52.7B of semiconductor funding and signed by POTUS on August 9th, 2022. It contains an additional Federal budget of $152M per year for quantum technologies for the 2023-2027 period, although seemingly not specific to components manufacturing. Chips USA manufacturing market share is in the 12% mark, above EU's that sits around 9%. The rest is in Asia, mostly Taiwan, South Korea, China and Japan [3428].

2.4.2 Generic processes

We'll describe here the generic processes used to produce chips regardless of their use case, the most commonplace being bipolar, CMOS and BiCMOS chips. Bipolar transistors have a very high speed and are used in analog devices. CMOS transistors are slower and do not handle such high power as bipolar transistors but are aggressively scaled down in density and require far less power to operate. BiCMOS used both bipolar and CMOS logic that are co-integrated within the same chip, which requires additional process steps and incur higher costs.

The story always begins with a wafer, as shown in Figure 442.

Wafers are usually made of monocrystalline silicon sliced with wired diamond saws out of ingots manufactured with the Czochralski crystal growth method.

They are sometimes completed with a thin buried layer of SiO_2 (aka SOI, for silicon on insulator) and another thin layer of regular Si, using the Smart Cut process invented by Michel Bruel at CEA-Leti in 1991 [3429] and implemented by SOITEC and its licensing partners [3430]. It is not using a wire diamond saw like the ones used to slice wafers out of silicon ingots. It first creates a layer of SiO_2 on a Si wafer using thermal oxidation in a wet atmosphere, PECVD or CVD. A second Si wafer is then implanted with H or He ions, which does not act as an adhesive but creates a weakened plane at a controlled depth. The oxidized face of the first wafer is bonded to the implanted wafer, and thermal annealing splits the implanted wafer along that plane, transferring a thin monocrystalline Si film onto the SiO_2. The transferred layer is then finished by annealing and polishing. This is a bonding and exfoliation sequence, not a silicon deposition. The remainder of the second wafer can be reclaimed and reused for another transfer cycle. Both the SiO_2 and the overlay Si layers can be as thin as 10 nm. A variant of the Smart Cut process is also used to transfer a thin Si layer onto sapphire wafers and thermal annealing is created with laser beams in a so-called "LLO" process, for laser lift-off.

SOI wafers have many interesting characteristics like reduced parasitic capacitances and low leakage currents. They are frequently used for nanophotonic circuits (like those from PsiQuantum manufactured by GlobalFoundries) or for silicon qubits chips (CEA-Leti, QuTech, ...). In other cases, wafers are made of III/V semiconducting materials (like GaAs or GaN, for manufacturing some nanophotonic circuits) or even sapphire (aluminum-oxide, Al_2O_3, for some superconduct-

ing qubits and trapped ion circuits). A wafer has a thickness ranging from 40 μm to 775 μm, the SEMI standard for 300 mm wafers, and its diameter ranges from a couple inches (for III/V and other small volume processes) to 300 mm for volume CMOS processes. A 450 mm transition was planned in the 2010s but the G450C consortium was wound down in 2016 and no 450 mm production line was ever built.

The most generic chips production processes then involve several cycles with the following successive steps with a repeat cycle ranging from resist coating to planarization including patterning, removing and adding matter.

When this cycle is over will all chip layers added on top of the other, the process ends with various finishing steps up to a packaged chip ready for integration.

Patterning

These are the process steps that define the places in the wafer where matter has to be removed with etching or added afterwards. It involves several steps that are defined during the design stages exploiting automated electronic design automation (EDA) software tools like those from Synopsys, ANSYS (acquired by Synopsys for $35B in 2025), Cadence, Keysight Technologies and Mentor Graphics (in Siemens group).

Resist coating is applied on the wafer with a photoresist liquid that will be later exposed during the lithography process and selectively removed during development. The coating is mechanically added with a dispenser nozzle positioned above the center of the rotating wafer attached to a chuck and spindle with vacuum pumping [3431] (Figure 443).

EBR (edge bead removal) removes excess coating at the wafer edge with a solvent. Then a N_2 based soft bake evaporates most of the solvent.

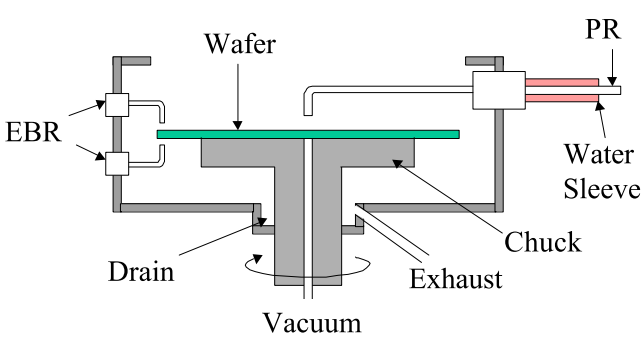


Figure 443: Resist spin coating. Source: [3431].

Photolithography is used to expose a special coating on selected areas (Figure 446). The photolithography technique makes use of a photomask and ultra-violet rays exposing a photoresist film or coating. It's being used to produce silicon qubits and nanophotonic chips. The usual photolithography process involves a stepper which moves the wafer under the projection optics to expose the wafer for each and every chip to produce, with a stage placement and overlay accuracy well below the nanometer, 0.7 nm on ASML's latest High-NA systems. This overlay budget should not be confused with the printed resolution, which is one order of magnitude larger depending on the level of High-NA photolithography used.

It replaces mask aligners that are used when the photolithography process exposes the whole wafer in a single step. The size of the chip is limited by the size of the photolithography reticle, which conditions the mask maximum size. Across time and density improvements, various ranges of ultraviolet wavelengths have been used.

It started with UV, to DUV or deep ultraviolet at 248 nm (KrF) and 193 nm (ArF), then to EUV (extreme ultra-violet) at 13.5 nm. A further step to BEUV (beyond EUV) at about 6.x nm, border line to soft XRays, is investigated on synchrotron and free-electron laser sources but has no announced tool roadmap. Starting with EUV, there is only one provider of photolithography system, ASML (Figure 444).

Figure 444: A typical ASML EUV photolithography system, without its doors. Probably a TWINSCAN EXE:5200B. Low-NA (0.33) EUV systems resolve down to 13 nm while this High-NA machine reaches 8 nm single-exposure resolution with 0.7 nm overlay, thanks to its 0.55 NA (numerical aperture) anamorphic projection optics, both at the same 13.5 nm wavelength. Source: ASML.

Electron beam lithography (EBL) is another lithography technique, which focuses a beam of electrons onto an electron-sensitive resist film, without requiring a mask. The beam exposes the resist rather than removing matter directly: development then reveals the pattern, which is used in the later etching or deposition steps. EBL beams can be focused down to about 1 nm, and routinely pattern 5 to 10 nm features, better than photolithography, with sub-5 nm demonstrated on HSQ resists. It is used to create precision nanostructures like with photon-generating quantum dots and superconducting qubit chips. It is a very slow process compared with photolithography, so adapted to low volume and custom productions. An EBL looks like an electron microscope. Existing electron microscopes can be converted to run EBL tasks.

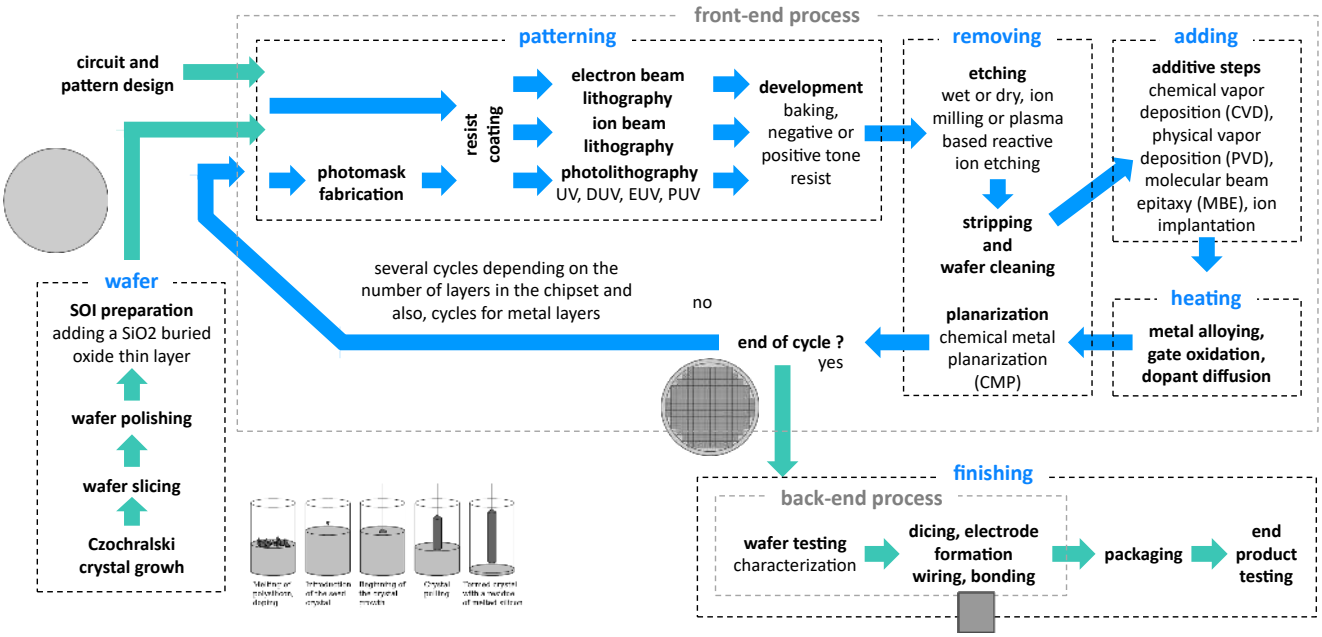


Figure 442: Generic layout of a chip manufacturing process. ⓒ Olivier Ezratty, 2022.

Other less used varieties of lithography are ion-beam (using helium), laser lithography, the latter being used for resolutions down to about 200 nm on current direct-write tools, and STM (Scanning Tunnelling Microscopy) that can reach sub-nm resolutions.

Development which removes the photoresist coating where it was or wasn't exposed during the photolithography or electron beam lithography step. It depends on the photoresist material used which is either a negative (insoluble after exposure) or positive resist material (soluble after exposure).

Positive photoresist enables better lithography resolution but is more expensive than negative photoresist. It uses so-called hard baking above 100°C to polymerize and stabilize the photoresist coating.

Figure 445: Kurt Lesker OCTOS Automated Thin Film Deposition Cluster Tool (source)

There are many resist coatings depending on the process (photolithography or electron beam lithography) and whether we are using a negative or positive resist. With positive resist, coating can be made of long polymer chains with weak chain bonds. Exposure creates chain scission in the exposed areas. These are dissolved during the chemical development process while the longer chains do not dissolve. Another process uses resist creating hydrophilic product when exposed, which are then dissolved by water. Negative coating can be made of monomers that polymerize when exposed to light and become non dissoluble by the solvent used in the development process.

Figure 447: Applied Materials Endura Clover MRAM PVD System (source).

The photolithography process contains in total about 10 stages (coating, soft-baking, exposure, cleaning, hard-baking, ...). In volume production, these are handled in cluster tool systems, using one or several robotized systems to move the wafer from one tool to the next in a

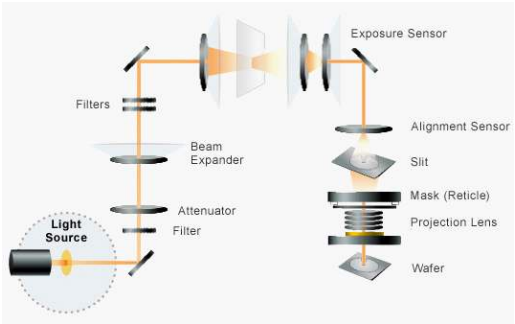
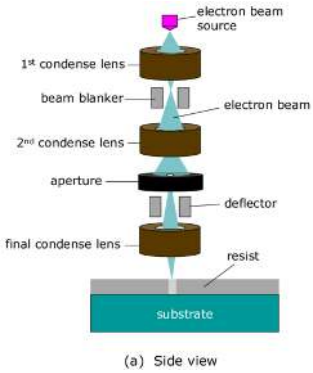
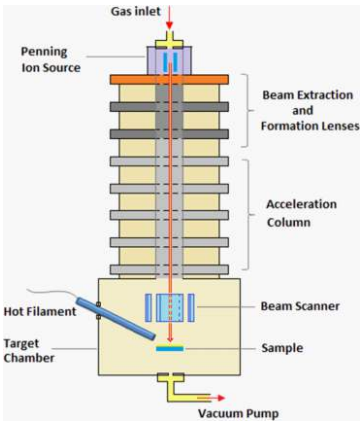
	photolithography	electron beam lithography (EBL)	ion beam lithography
how it works	use of a photomask and ultra-violet rays exposing a photoresist film or coating	focusing a beam of electrons on an electron-sensitive resist film to remove matter in specified areas	focusing a beam of ions on an ions-sensitive resist film to remove matter in specified areas
			
variations	DUV, EUV, PUV	electrostatic or magnetic lenses, scanning tunneling microscope	
use cases	CMOS chipsets, superconducting circuits, high volume throughput	superconducting qubits Josephson junctions, sub 10 nm resolution but low throughput	III/V photonics and quantum dots, very high resolution structures

Figure 446: The three main lithography techniques used for semiconductors manufacturing. Compilation 🅭 Olivier Ezratty, 2022-2023.

controlled environment. This ensures both productivity and production quality (Figure 445 and Figure 447).

Photolithography clusters vendors include Dainippon Screen, which partners with ASML. Cluster tools are also in place for other parts of manufacturing seen later, like etching and additive steps. Multi-axis robots and roof conveyors like those from Kuka and Muratec move wafer cassettes (handling 25 wafers) from one cluster to the other.

Removing matter

These steps correspond to the removal of matter on the wafer based on the zones defined by the lithography process (Figure 448).

Etching removes matter in the uncovered areas, using wet chemical or dry physical methods, the dry methods being the most commonplace for high-density (VLSI) circuits. Various dry etching techniques include ion milling or sputter etching, and plasma based reactive ion etching. The first uses the projection of inert ionized noble gas. Reactive ion etching combines both mechanisms: reactive species generated in the plasma attack the surface chemically, while directional bombardment by the ions accelerated toward the wafer supplies the physical component and the anisotropy. In general, plasma is an ionized gas with the same proportion of positive and negative charges. There are also variants with isotropic etching (direction independent, which undercuts the mask) or anisotropic etching (direction dependent, which produces vertical sidewalls). Dry plasma methods owe their anisotropy to the directional ion bombardment normal to the wafer, wet chemical etching being usually isotropic except on crystal-plane selective chemistries.

Stripping and cleaning remove the remainder of the photoresist material. In volume production clean rooms, etching and stripping are handled by cluster tools with robotized handlers moving wafers from the etcher to the stripper tool, with a loading and unloading station extracting wafers from its carrier box (usually, containing 25 wafers in volume production environments).

Planarization of the wafer combines chemical and physical polishing. It is based on CMP (Chemical Mechanical Planarization), which uses an abrasive and corrosive slurry on a rotating pad, and applies to dielectrics as well as metals. It is generally implemented after additive steps.

Adding matter

Additive steps consist in adding some materials in the visible areas, like silicon or doped silicon in classical CMOS transistors, using boron or indium (for p-doping) and arsenic (As), phosphorus (P), antimony (Sb) or aluminum (Al) (for n-doping). Some of these processes are implementing an epitaxy, creating a perfect crystalline structure with the added material, in the feature layers (doped silicon, gates). Other processes like PVD and sputtering are not epitaxial and are used for the production of superconducting qubits.

Additive steps can use various techniques like ion implantation, CVD (chemical vapor deposition, where the target surface is exposed to one or more volatile precursors, which chemically react and/or decompose on the target surface to leave a thin film deposit on the target, e.g. using silane SiH_4 to deposit Si on the wafer, gen-

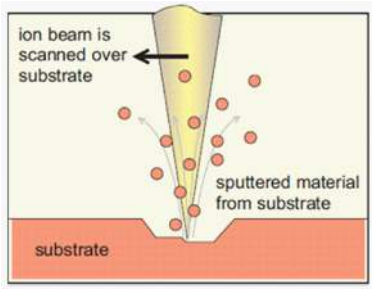
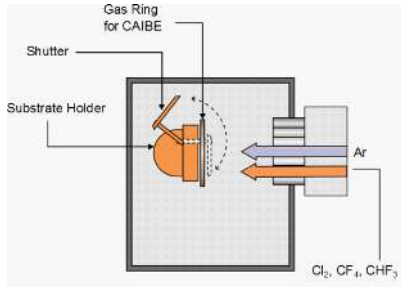
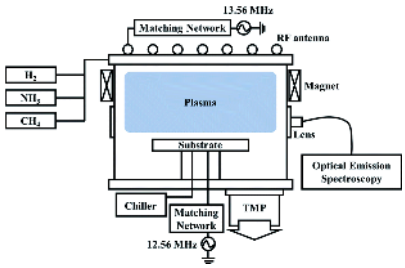
	ion milling or sputter etching	ion beam etching (IBE)	plasma based reactive ion etching (RIE)
how it works	the ions of an inert noble gas like argon are accelerated from a wide beam ion source on the target in vacuum to mechanically remove material on the target.	the ions of active molecules like CF_4, Cl_2 or CHF_3 are accelerated from a wide beam ion source on the target in vacuum to mechanically remove material on the target.	energetic and neutrally charged free radicals reacting at the surface of the wafer, attacking the wafer from all angles, aka, being anisotropic.
			
variations	reactive ion etching deep reactive ion etching	ion polishing, ion cutting, reactive ion beam etching (RIBE, RIE), chemically assisted ion beam etching (CAIBE).	MEMS, nanophotonics, niobium resonators in superconducting qubits
use cases	superconducting qubits	III/V chipsets, single photon quantum dots shapes, MEMS	

Figure 448: Various ways to remove matter in semiconductor manufacturing. Compilation © Olivier Ezratty, 2022-2023. Illustration sources: Wikipedia and others.

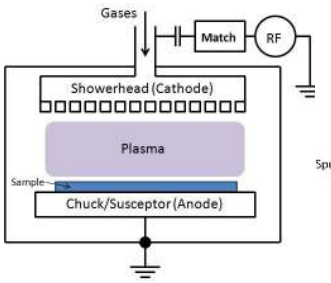
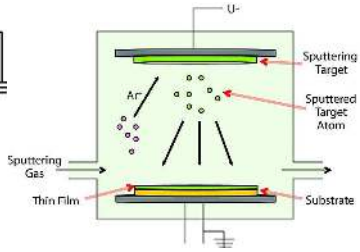
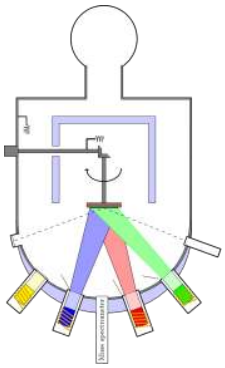
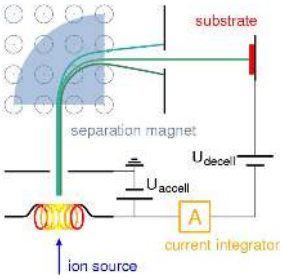
	CVD chemical vapor deposition	PVD physical vapor deposition	MBE molecular beam epitaxy	ion implantation
how it works	target surface is exposed to volatile precursors, which chemically react and/or decompose on the target surface to leave a thin film deposit on the target	the material to deposit is first turned into vapor and then condenses on the target surface	thin-film highly controlled deposition of single crystal structures, in ultra-high-vacuum	ions are separated in a magnet, accelerated in an electric field , deflected to obtain homogeneous doping, then implanted into the wafer
				
variations	plasma assisted CVD (PECVD) low-pressure CVD (LP-CVD), MOCVD, HTCVD, LPCVD, ALD	sputter deposition electron beam PVD pulsed laser deposition (PLD) molecular beam epitaxy (MBE)		
use cases	synthetic diamonds, graphene, SiO_2 with SiH_4 (silane), aluminum, polysilicon deposition	superconducting qubits (Al, Al/AlO_x/Al)	III/V layers depositions	silicon doping

Figure 449: Various ways to add matter in semiconductor manufacturing. Compilation © Olivier Ezratty, 2022-2023.

erating 2 H_2 molecules), ALD (atomic layer deposition, a variation of CVD using self-limiting surface reactions in repeat cycles to create highly conformal films with sub-nm thickness control, generally amorphous or polycrystalline rather than epitaxial, the epitaxial variant being ALE, atomic layer epitaxy), PVD (physical vapor deposition under low pressure, where the material to deposit is turned into a vapor by evaporation, sputtering or plasma and then condenses on the target surface), sputtering being one type of PVD (using ion projection to pull material from a source and deposit it on the target wafer or ionized gas like argon that, thanks to a high-voltage applied to the target, is projected on the target and creates a plasma with the target atoms that then condenses on the surface of the chip), e-beam deposition (another variety of PVD using electron beams to evaporate the matter to deposit on the wafer), PLD (pulsed laser deposition, using nanosecond excimer laser pulses, usually KrF at 248 nm, to ablate matter from a target that is then deposited on the substrate, femtosecond PLD remaining a research variant), and MBE which is a variety of PVD (molecular beam epitaxy, for thin-film deposition of single orderly crystal structures). CVD can be plasma based (Figure 449).

In the last process cycles, these steps are related to the creation of several superposed metal layers connecting the various semiconducting circuits created in the earlier steps. With superconducting qubits, aluminum, and aluminum oxide (or niobium) sputtering is implemented in this step.

Metal layers. When all cycles related to the functional parts of the circuits are finished, some electrodeposition of metal is made to connect the chip to the outside world, usually copper or aluminum (in the case of superconducting qubits and electronics) and copper-aluminum alloys.

Metal layers are created with a mix of lithography-etching and PVD/CVD.

As metal layers are added, their density decreases. Then, some wiring may be added and bonding or bumps plus packaging.

In CMOS designs, the "front-end-of-line" (FEOL) contains the individual active elements (transistors, capacitors, etc.) while the "back end of line" (BEOL) contains the metal layers (Figure 450).

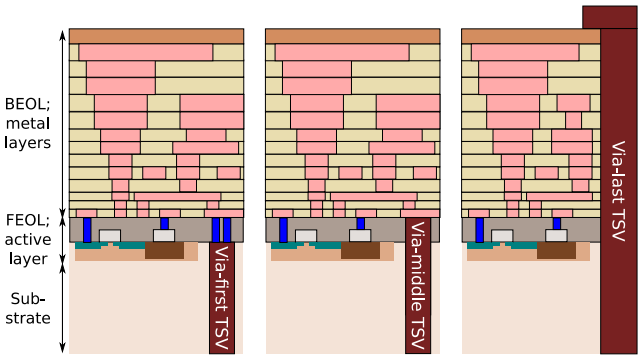


Figure 450: Typical metal layers of a semiconductor.

So-called 3D chips like the superconducting qubits chips from IBM, OQC and others result from the assembly and perfect alignment of stacked chips. CEA-Leti (France) is collaborating with Intel in the design of such innovative 3D packaging technologies. 3D stacking makes use of TSV (through silicon vias), which establishes a metal connection from top to bottom of a chip or from the active layer to the front plane through the wafer. A TSV hole is created with reactive ion etching, copper electrochemical deposition for creating a seed layer and electroplating to fill the hole [3432]. Creating TSVs in chips can add 30 to 200 steps in manufacturing.

Heating

Thermal processes are implemented for various purposes like dopant activation and diffusion, gate oxidation (dry, $Si + O_2 \rightarrow SiO_2$, or wet, $Si + 2\ H_2O \rightarrow SiO_2 + 2\ H_2$), metal reflow which smooths its surface usually in an atmosphere of N_2 or H_2O, metal alloying and chemical vapor deposition. One used technique involves rapid thermal annealing, using a vertical or horizontal furnace.

Finishing

These are the product finishing tasks undertaken when the patterning-removing-adding-heating cycle is completed (the front-end process). The aim here is to turn the chip on its wafer into a functional component with its connectivity. It is also called the back-end process (Figure 451).

Wafer testing. Then, testing and characterization are done to make sure the manufactured components meet the required quality. One inspection tool used is electron microscopes, which can also be used to analyze the patterning quality between each patterning cycle. Wafers containing chips operating at cryotemperatures can be tested by a cryo-prober like the one provided by Bluefors/Afore and being used by Intel in Oregon and CEA-Leti in Grenoble.

Electrode formation, wiring and bonding. These are more traditional steps to add macro-elements to the circuit that will connect them to the outside world. This is done after the chips are extracted from the wafer with dicing.

Packaging. It is mostly about putting plastic and sometimes metal shielding for specific applications (space, military, quantum) around the chip and its bonds/wires. The component can be then integrated in a system with its surrounding electronics.

End-product testing. The electronic circuit is fully functionally tested here before being used.

The manufacturing yield is the percentage of functional chips at the end of manufacturing. Each intermediate manufacturing step has its own yield, and the end yield is the result of the multiplication of each step yield.

2.4.3 Quantum process specifics

Each and every chip is manufactured with a specific recipe with many steps involving different tooling and dozens of parameters (tool, chemical compounds, temperature, pressure, angles, ...). Putting in place such processes is tedious and requires very specialized skills. The whole manufacturing process for a chip can last from a few hours to a few months, depending on the process flow, the number of lithography levels and the facility, a research fab with short queues behaving very differently from a volume line. All in all, a new chip design, manufacturing and testing can last between a couple weeks to 2.5 years depending on the product and process.

Superconducting qubits

Manufacturing a superconducting qubit chip is both rather specific and simple, at least, compared to classical silicon CMOS chips and their epitaxy processes, creating pure crystalline semiconducting structures. It explains why so many labs in the world have their own cleanroom able to prototype such chips. A supercon-

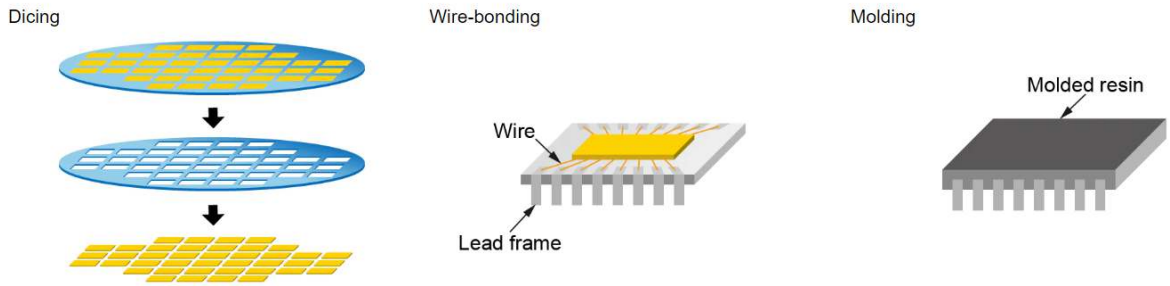


Figure 451: Finishing steps of semiconductor manufacturing with dicing, wire bonding and molding. Compilation Olivier Ezratty, 2022 and The semiconductor manufacturing process (back-end process), Matsusada, February 2022.

ducting chip wafer can usually be produced in less than a week when it can last months if not over a year for CMOS chips on 300 mm wafers [1101, 3433, 3434]. There are of course many variations and as the superconducting chips become more complicated, assembling up to three stack chiplets, and with more lithography steps, the production cycle gets longer.

We will describe here one of the methods to create a superconducting qubit chip which is derived from the Niemeyer-Dolan bridge technique [3435, 3436] (Figure 452). There are other Josephson junction techniques like the Manhattan bridge [3437]. The superconducting qubit core feature is its Josephson junction made of three layers: a conducting metal like aluminum and its oxide insulator variant in between. It is surrounded by metal structures for creating capacitances and a resonator.

- The wafer substrate is made of either **sapphire** (aluminum oxide) or **intrinsic silicon**, meaning monocrystalline and undoped. Silicon is commonplace but has its shortcomings: the native oxide is usually removed before deposition, because amorphous SiO_2 and the substrate-metal interface host two-level-system defects that contribute dielectric loss. The issue is interface and dielectric loss rather than silicon dioxide being intrinsically damaging. Sapphire does not form such a native oxide but is less commonplace [3438]. The wafer may be gold plated on its unpolished side to ensure good electric and thermal contacts between the chip and the chip-carrier.

- Resist deposition is done using the spin-coating technique and with two layers of resist one on top of each other. The bottom one is more sensitive to the e-beam than the one above.

- Electron beam lithography (EBL) usually exposes some of the resist to an electron beam. This is a rather slow process. It uses a double exposure at different doses to attack the two resist layers. This can be replaced by photolithography [3439].

- Development where the resist is removed from the hole exposed by the e-beam and etching which creates an undercut carved in the resist.

- First metal evaporation where a first layer of aluminum is deposited with an angle $+\theta$. It creates the first layer of the Josephson junction. This is called angle evaporation.

- An aluminum oxide layer is grown during a controlled static oxidation step. This tunnel barrier, not a gate, is 1 to 2 nm thick and its thickness sets the junction critical current, hence the qubit frequency.

- Second angled metal evaporation to create a new layer above the oxidized aluminum from the Josephson junction gate. It is done in the opposite angle -θ to cover a different area in the hole.

- The residual resist may in some situations be removed with a CMP process or more classically dissolved in solvent during the liftoff step. For these, no additional layer or isolation layer is added on the Josephson junction. The liftoff process can create defects that reside at amorphous interfaces between the various superposed layers. These defects are generating qubit decoherence.

All this process was just about creating a single Josephson junction that is usually 200 nm wide. A classical superconducting qubit contains at least two other circuits: capacitances (about 100 μm to 600 μm wide), a resonator (*aka* superconducting coplanar waveguide) and a microwave network.

The network and resonator can be created using 193 nm UV lithography or laser lithography and negative resist etching, meaning the metal is first deposited everywhere (except on the Josephson junction) and then, the resist coating is removed where it was not exposed. RIE (reactive ion etching) can also be used, particularly for creating resonators. This process can make use of aluminum, niobium, TiN (titanium nitride), first shown as a low-loss resonator material by Vissers et al. at NIST in 2010 [3440] and systematically characterized by the Martinis group at UCSB [3441], and even indium.

Titanium nitride is valued as a potentially low-loss material when properly deposited and patterned, its surface oxidizing far less readily than niobium. It can also be used as a dielectric layer on a sapphire substrate to limit losses between the various qubit components [3442].

Superconducting qubits circuits are usually rather simple and only 2D with no additional metal layers. Still, superconducting metals like tantalum are tested over the parts of the chip outside the $Al/AlO_x/Al$ Josephson junction, like on the various niobium circuits (resonators, ...), the native Ta_2O_5 being significantly less lossy than the Nb_2O_5 that forms on niobium. Tantalum transmons pushed relaxation times (T_1) past 0.3 ms at Princeton in 2021 [3443] and niobium surface encapsulation gives comparable gains [826, 3444].

There's an empty space of a minimum height of 2 mm above and below the chip in its (copper) packaging. On the other hand, superconducting electronics dies can superpose up over 10 alternating layers of niobium and dielectric, usually SiO_2. The surrounding connections are themselves superconducting and the chip edge is connected to gold or aluminum wires and bonds. Some elements on the chip may be connected with 'airbridges' which use wired connections between two distant elements 'flying' over a qubit component, with a small layer of air/vacuum between the circuit and the wire [3445]. These airbridges are usually made in aluminum or niobium [3446–3448].

Andreas Fuhrer Janett from IBM Zurich labs developed a process and apparatus to put the chip in ultra-high vacuum (UHV) during assembly [877]. According to IBM, the UHV can contribute to creating less noisy qubits.

The connectivity constraints explain for example the limitations of the chimera structure in D-Wave superconducting qubits layout. The trend is to create 3D structures, assembling several chips, with one being dedicated to electronic signals controlling the qubits, like with Google, IBM and OQC.

The chips are assembled using wafer bonding, connecting metal layers using indium thanks to its ductility, which it retains at cryogenic temperatures, and to its low 156°C melting point. Chips also use TSV (through-silicon vias) to facilitate signals routing between the connectivity chip and the qubit chip [420]. As of 2024, fabs are looking for a way to etch superconducting TSV to enable low-losses interconnect.

The chip density is not very high compared with classical CMOS chips. The quality and fidelity of superconducting qubits depend on several factors including materials purity [3449]. The manufacturing yield of superconducting chips is rarely published. It falls exponentially with the qubit count at a given per-junction yield, which is why frequency targeting and post-fabrication trimming matter so much, and the only systematically measured figures come from the 300 mm CMOS pilot lines [3450]. One avenue to potentially improve the manufacturing quality of superconducting qubits would be to produce them with 300 mm CMOS fab technologies. That's what IMEC experimented in 2022 until 2024 with the production of superconducting qubits of rather good quality (but not stellar), using argon milling [3451] and subtractive processes [3450, 3452].

We have mentioned aluminum frequently so far. It is not the only superconducting metal used with Josephson junctions, but it is favored partly because the aluminum oxide forms a stable thin junction. Niobium, niobium-titanium nitride, and tantalum [768] can be used for large structures like resonators. Niobium is also used in superconducting electronics (SFQs, already covered) and SQUIDs sensors with the advantage of a critical temperature of about 9.2 K against about 1.2 K for aluminum. Niobium is easy to etch but oxidizes quickly.

Some other techniques are also inspired by classical CMOS manufacturing with EUV lithography, particularly at IMEC [3453, 3454]. While the dominant aluminum and aluminum oxide deposition is using sputtering, alternative techniques are using ALD (atomic layer deposition) [3455].

Superconducting nanowire single photon detectors

Superconducting nanowire single photon detectors (SNSPDs) are made of a few nm of a disordered superconductor sputtered on an oxidized silicon or SiN substrate, then patterned into a meander by EBL. NbTiN [3456], NbN and amorphous WSi or MoSi are the main material systems, the amorphous ones giving the highest system detection efficiencies [3457].

Trapped ions circuits

These circuits implementing Paul or Penning traps are manufactured using a mix of techniques with e-beam metal evaporation-based deposition of titanium and gold, etching process, and femtosecond-laser machining for 3D surfaces shaping using tools like those from **FEMTOprint** [1851].

Infineon

Germany, 1999

Infineon formally opened its quantum lab near Munich in October 2023, to develop and test ion trap circuits with a team of about 38 people as of mid-2025, who are located in their Villach plant in Austria and Munich in Germany. They are using very traditional CMOS manufacturing techniques for building ion traps. They became the defacto manufacturer for many trapped-ion QPU vendors, like Oxford Ionics, AQT and Quantinuum. They can produce Si, GaN, SiC and glass wafers of 6, 8, and 12 inches. They have an in-house ion-trap testing bed supporting $^{40}Ca^+$ ions. They even publish new ion-trap chip design papers from time to time [3458, 3459].

Photon-generating quantum dots

The quantum dots from CNRS C2N and Quandela are manufactured by growing about 100 alternating

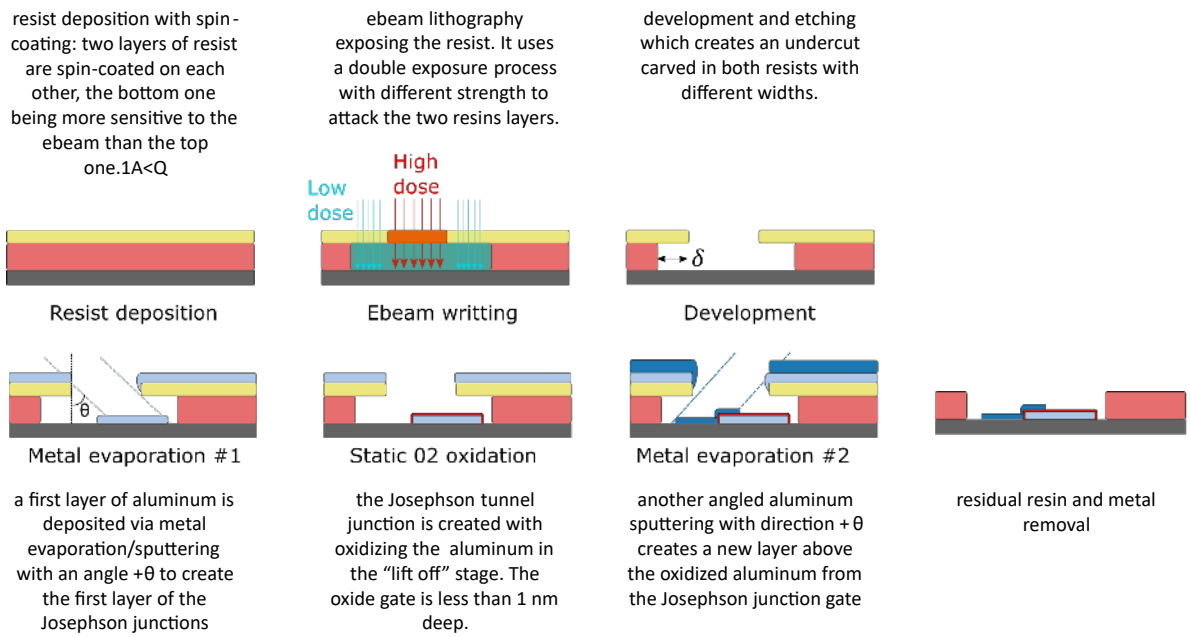


Figure 452: Process for manufacturing a superconducting qubit or superconducting component like a TWPA. Source: [3292]. Comments added by Olivier Ezratty in 2022.

GaAs and AlGaAs layers by molecular beam epitaxy, which form the distributed Bragg reflectors of the cavity. Adding these many layers can be achieved in a couple of hours. In the middle of the road, the planar λ cavity contains the active layer in which self-assembled InGaAs quantum dots nucleate, a few nanometers in size and randomly positioned. The cylinder cut for the quantum dot enclosing is implemented with ion milling [3460].

Silicon qubits

Their manufacturing is very close to traditional CMOS manufacturing techniques (Figure 453) [3186]. It requires UV/EUV photolithography due to the relatively high features density in the chips (which can go as low as 10 nm). The etching processes are also rather similar. The materials purity is an important figure of merit to ensure the quality of the manufactured qubits as it is with superconducting qubits.

The silicon wafers used to create spin qubits are covered by a layer of about 100 nm of ^{28}Si using a wafer scale CVD process fed with isotopically enriched silane (SiH_4), a scarce and costly precursor. Only this active layer needs enrichment, the point being to remove the 4.7% of spin-carrying ^{29}Si from the qubit environment. Gate polysilicon, gate oxides and passivation layers keep natural isotopic abundance. There are many variants with Si/SiGe heterostructures, Al/AlO_x structures, etc. Indeed, superconducting features must be integrated in these chipsets on top of more regular CMOS ones [3461]. The chip vertical structure is relatively simple, with only a few metal layers, and some control electronics are usually placed in a separate chip that is bonded to the qubits in a 3D.

In its various research papers published at APS March meeting in 2022, **Intel** did showcase how manufacturing quality had an impact on the quality of quantum-dot spin qubits. In October 2022, they added some information on the quality and yield of their silicon qubits wafers, later published as full cross-wafer statistics on 300 mm [3462, 3463].

3D printing

3D printing or additive manufacturing is now becoming commonplace to produce various elements in quantum technologies [3464]. They can be used to create various plastic or metal elements in labs or for commercial products. 3D printing is often used to create custom optical package elements in photonic experiments, like for fiber holders. It can even be used to create complex titanium surface structures that can be used to manipulate gases in ultra-high vacuum (UHV) chambers [3465]. A team at UC Berkeley proposed using 3D printing for the integration of 3D structured micro Radio-Frequency (RF) electrodes above a surface-electrode trap in QCCD ion traps [3466]. Some superconducting qubit elements like resonators could also be deposited through 3D printing using liquid metal (eutectic gallium-indium, EGaIn) [3467].

2.4.4 Tools

We'll cover here some specific manufacturing tools that are used for producing quantum technologies semiconductor components. The breadth of tools in semiconductor fabs is much broader with tools from vendors like **ASML** (UV and EUV photolithography) and **Applied Materials** (PVD, CVD, etching and stripping, ...). Their tools are used in high-volume large fabs while

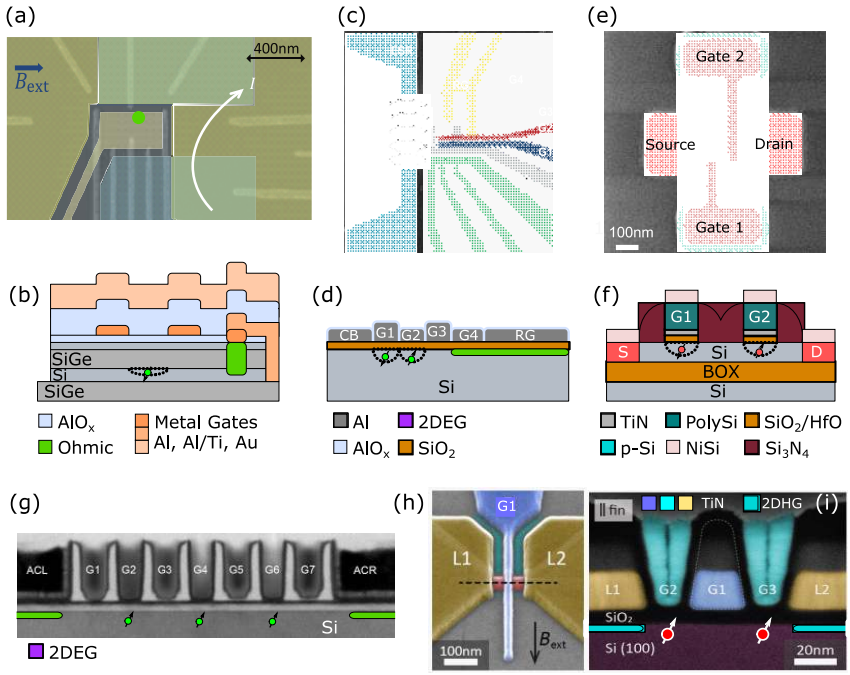


Figure 453: Various implementations of silicon spin qubits. Source: [115].

many of the quantum-specific production tools are used more for research purposes and for small scale industrial production.

ADNANOTEK

Taiwan, 1999

ADNANOTEK is a provider of MBE, PLD (pulsed laser deposition which is a variation of PVD) and Laser MBE PLD, various sputtering systems, EBE (electron beam evaporators), Ion Beam Sputter Deposition (IBSD), ALD (atomic layer deposition), Plasma Enhanced Atomic Layer Deposition (PEALD) and various ultra-high vacuum equipment.

Angstrom Engineering

Canada, 1992

Angstrom Engineering is a manufacturing tool vendor. Their Quantum Series line of physical vapor deposition (PVD) systems is adapted to the creation of Josephson Junctions, from using an electron beam source to deposit aluminum, magnetron sputtering for niobium and ion beam cleaning.

Arkeon Technologies

Sweden, 2024, €600K

Arkeon Technologies is a spin-out from Chalmers University of Technology and the Wallenberg Centre for Quantum Technology (WACQT), created by Peter Hörstedt and Andreas Nylander. Their core product is a post-fabrication trimming process for Josephson junctions. It allows precise adjustment of Josephson junction resistances directly on completed chips, enabling controlled tuning of qubit frequencies without multiple cooldowns or redesign cycles [3468].

ATLANT-3D

Denmark, 2018

ATLANT-3D created an on-demand atomic layer deposition advanced manufacturing technology based on hybrid Microreactor Direct Atomic Processing.

Beamfox

Sweden, 2016

Beamfox is a company created by Leonardo Midolo (CEO), Anders Lynge Esbensen (CTO) and Søren Stobbe (CSO) that created Proximity, a software for correcting errors for electron-beam lithography.

Besi

the Netherlands, 1995

Besi, or BE Semiconductor Industries, is the worldwide leader in semiconducting assembly machines (die attach, packaging, plating). One key use case is 3D chiplets assemblies. The company participates in the EU project MATQu to create a manufacturing capacity of superconducting chips on 300 mm silicon wafers.

CDimension

USA, 2025

CDimension is a MIT spin-out that is developing wafer-scale single-crystalline 2D insulators that may contribute to reducing noise in quantum devices like superconducting qubit chips. It replaces amorphous or polycrystalline

oxides with single-crystalline, ultra-thin 2D insulators that can increase coherence times and reduces two-level-system (TLS) noise. It could also lead to the creation of low-dissipation cryo-CMOS circuits.

Chiral Nano

Switzerland, 2023, $15.8M

Chiral is spin-out from ETH Zurich and Empa, created by Seoho Jung (CEO), Natanael Lanz (CTO/COO), and André Butzerin (CPO), all former PhD students from a joint ETH/EPFL/Empa national research project. The company builds robotic and AI-enabled systems for the wafer-scale integration of nanomaterials like carbon nanotubes, graphene and TMDs into semiconductor and quantum devices. Its first prototype was 100 times faster than existing systems. Empa demonstrated ultra-clean carbon nanotube quantum dot devices at 300 mK using their technology and the first commercial systems are being installed at customer sites in 2026. The $12M seed round was led by Crane Venture Partners with Quantonation, HCVC, Founderful and Innosuisse.

CVD Equipment Corporation

USA

CVD Equipment Corporation is specialized in CVD and dry etching systems that can be used for various semiconductor production, including III/V and nanophotonic chips.

Encapsulix

France, 2011

Encapsulix develops ultra-short cycle time ALD systems. It is mostly used in the production of OLED in encapsulated quantum dots.

Evatec

Switzerland

Evatec provides a family of evaporation, sputtering and PECVD products covering various needs including in MEMS and photonics applications. They also develop and sell wafer cassette-to-cassette processing tools in their Clusterline family.

Izovac Photonics

Lithuania

Izovac Photonics provides the IZOVAC range of products vacuum coating equipment using vacuum sputtering (magnetron sputtering, Ion Beam Assisted Deposition, Ion beam sputtering, DLC (Diamond-Like Carbon) coating by PECVD (Plasma Enhanced Chemical Vapor Deposition). Their main market is the manufacturing of displays and touch screens. They also develop customized vacuum deposition equipment.

Kelvin Nanotechnology

UK, 2020

Kelvin Nanotechnology is an electron beam lithography and nanofabrication tooling company. It manufactures various miniaturized MEMS and photonic components used in quantum technologies. These include 3D ion traps, various photonic devices, MEMS gravimeters and lasers built on 200 mm wafers in features going as low as 20 nm. They are based at the James Watt Nanofabrication Centre (JWNC) in Glasgow, Scotland.

Mind Foundry

UK, 2024

Mind Foundry is a spin-out from Oxford University that does contract research for the defense industry. They are using AI to run wafer-scale superconducting qubits characterization. They partnered with NPL, SEEQC and Riverlane.

NoPo Nanotechnologies

India, 2011

NoPo Nanotechnologies manufactures small diameter (0.8-1 nm) single-walled carbon nanotubes (SWCNT).

Onnes Technologies

the Netherlands, 2018

Onnes Technologies is a startup created by Max Kouwenhoven (CEO) that develops the arQtika Linear Cryo-Walker for Quantum Scanning Probe Microscopy (qSPM). It is a low-dissipation cryogenic nanopositioner, that can be used to study the structure of protein complexes, such as ferritin, a protein in the human brain linked to Alzheimer's disease, with excellent precision and accuracy. It was developed in collaboration with Leiden Cryogenics. Their solution can also be used to characterize various aspects of transmon qubits.

OrangeQS

the Netherlands, 2019, €28.5M

OrangeQS, *aka* Orange Quantum Systems, is a provider of superconducting chip testing hardware, the OrangeQS MAX, which contains a cryostat and all control and characterization electronics. It also developed the OrangeQS FLEX product line, a set of modular software building blocks to complement existing chip test equipment, OrangeQS Box Lab PC, a PC with optional pre-installed OrangeQS Linux-based Juice, and Quantum Diagnostics Libraries.

Figure 454: OrangeQS MAX is a testing system for superconducting chips with a cryostat and control electronics.

Orsay Physics

France, 1989

Orsay Physics is a subsidiary of Tescan Orsay Holdings (Czech Republic - France). It provides manufacturing tools for focused ion and electron beam processes. Out of these, their nitrogen-FIB (i-FIB, for focused ion beam) is being used to create NV centers in nano- and microstructures with high precision, like in NV center arrays with 2 μm separations between the centers [3469].

Picosun Group

Finland, 2003-2022, €17.4M

Picosun Group is a manufacturer of atomic layer deposition (ALD) tooling used in the production of various electronic components (imaging sensors, LEDs and OLEDs, MEMS, etc). It was acquired by **Applied Materials** in June 2022 and now operates within its ICAPS group, still from Espoo, Finland. Their technology can be used to create graphene structures among other things. They are one of the Finish industry partners of **QuTI**, a €10M collaborative research project on quantum related components manufacturing and testing. They partner with VTT, Bluefors, Afore, IQM, Quantastica, Saab, Vexlum and the Finish offices from Rockley Photonics (USA) and CSC (USA).

Plasma-Therm

USA

Plasma-Therm has a broad range of plasma and ion beam etching and deposition used among other things in GaAs components manufacturing. The company made several acquisitions: Advanced Vacuum Europe of Lomma (1993, Sweden) in 2011, Nanoplas France in 2015, Nano Etch Systems (2009, USA) in 2016, Kobus and Corial (France) in 2018, JLS Designs Ltd (UK) in 2020. The company opened in 2018 its European Head Office in Grenoble, France, and in 2020, one process and technical support office in Singapore.

Plassys Bestek

France, 1987

Plassys Bestek develops and manufactures vacuum and ultra-high-vacuum thin film deposition systems with a turnover of about €7M. Most of their tools are based on physical vapor deposition (PVD) processes (vaporization of metal or compounds for deposition on a substrate, all under vacuum).

Positioned at the end of the 1990s as a key supplier of equipment for the fabrication of superconducting qubits, they have developed a wide range of electron beam deposition systems dedicated to controlled angle evaporation under the name "MEB". It makes Plassys the leader for this technology (Yale University, Rigetti Computing, QCI, NTT, Oxford, CEA Saclay, Qilimanjaro, TU Delft, VTT…rely on their tools). The "MEB" tools use an electron beam to melt and to evaporate materials that allows the deposition of aluminum films for forming the Josephson junctions or for resonators as well as of niobium as underlayer or as resonators. They also provide sputtering tools for depositing various kind of superconducting films (Al, Ti, Nb, Ta, MoSi, MoGe, nitrides…) and other elemental materials or complex compounds. Sputtering tools integrate cathodes on which a bias voltage is applied under a controlled atmosphere of gas mixture including argon for generating a plasma around 10^{-3} – 10^{-2} mbar. Positive ions from the plasma are attracted by the cathodes on which a "target" is made from the material source you want to deposit. The high energy of the ions sputters the target inducing then the generation of a vapor that condenses onto the substrate.

Figure 455: Plassys-Bestek evaporation production tool.

They also supply the SSDR150 chemical vapor deposition (CVD) reactor for the growth of ultra-pure diamonds which is the raw material for the development of NV center based technologies. This CVD process is using hydrogen and methane (CH_4) at a pressure around 100 millibars [3470] with the assistance of a microwave source generating a high density plasma. They also handle diamond doping with nitrogen, boron, phosphorus….

Their R&D and production machines dedicated to quantum technologies are now grouped under the Qutek Series brand (Figure 455). In addition to the MEB systems, Qutek series includes MP systems (sputtering deposition for superconducting or photonic devices) and thermal evaporation system for indium bumps (used for connecting superconducting qubits).

Polyteknik

Denmark, 2005

Polyteknik provides PVD and coating systems, including their Flextura e-beam PVD system.

Prevac

Poland

Prevac has a breadth of semiconductors manufacturing tools including a UHV Magnetron Sputtering System working with 3-inches wafers and PLD systems. They also sell an UHV multichamber cluster tool to automate a process with a thin film layer growth deposition chamber, load-lock chambers and a transferring tunnel.

Quantamap

the Netherlands, 2024

Quantamap was created by Johannes Jobst (CEO), Kaveh Lahabi (CTO) and Milan P Allan. It is developing a characterization tool for quantum chips (superconducting, silicon spin and ion traps), providing an image of what is happening on it. It uses a SQUID-on-tip quantum sensor to detect defects on the chip and operates at cryogenic temperatures on prototype chips with a size of 30x30 mm.

Quantum Foundry Copenhagen

Denmark

Raith

Germany, 1980

Raith provides nanofabrication and electron beam lithography instruments. These tools are involved in the manufacturing of all sorts of qubits, trapped ions, superconducting, electron spin, topological qubits, NV centers and nanophotonics.

Riber

France, 1987

Riber is a manufacturer of MBE reactors, used mostly in III/V and II/VI multi-layers epitaxy processes. They handle various MBE processes: solid sources MBE, Plasma-Assisted MBE (PAMBE), Metal-Organic MBE (MOMBE), Gas Source MBE (GSMBE) and full gaseous Chemical Beam epitaxy (CBE). A Riber MBE reactor is being used to manufacture the 100+ layers quantum dots based photon sources from Quandela.

Samco Inc

Japan

Samco Inc is a provider of thin film deposition, microfabrication and surface cleaning, CVD and other treatment machines. Their tooling includes PECVD systems (plasma-enhanced CVD), SiC CVD systems, ALD (atomic layer deposition) systems, reactive-ion etching (RIE) systems, Inductively Coupled Plasma (ICP) etching systems, Silicon Deep Reactive Ion Etching (DRIE) systems for MEMS device fabrication and TSV (through-silicon-vias) via-hole etching and plasma cleaners. These systems are used to produce various sorts of quantum components like niobium and tantalum based superconducting circuits, from qubits to surface acoustic waves filters [767, 3471]and GaAs photonic components.

Seki Diamond Systems

Japan

Seki Diamond Systems (Japan) is a subsidiary of **Cornes Technologies** (USA) that sells CVD diamond reactors producing synthetic diamonds and supporting Microwave Plasma CVD, Hot-Filament CVD and Low Temperature CVD. It covers broad industry use cases.

SOITEC

France, 1992

SOITEC is a company producing SOI wafers which contain an isolation layer of SiO_2. These wafers are commonplace in many quantum technologies semiconductor components.

SOITEC acquired EpiGaN (2010, Belgium, €4M) in 2019. It adds GaN wafers production to their portfolio.

Some other vendors can be mentioned like **RECIF Technologies** (France) with its wafers handling and sorters, **Heidelberg** (Germany) and its mask writer, **Süss MicroTec** (Germany) and its photomask handling and mask aligners, Keysight Technologies (and its NX5402A silicon photonics hybrid wafer testing system), **Oxford Instruments** (UK) and its RIE plasma etchers from the Plasmalab family and ALD systems, **Vistec Electron Beam** (Germany, Jena) and **Elionix** (Japan) and their e-beam writers, **Transene Company** (USA) and their etching systems, **Pureon** with its diamond based Chemical Mechanical Planarization tools (CMP, in 2020, Microdiamant (Switzerland) acquired Eminess Technologies from Saint Gobain and was rebranded as Pureon), **Polygon Physics** (2013, France) which provides ion, electron, plasma and atom sources based on ultracompact and ultralow power electron cyclotron resonance plasma technology (ECR) and Multi Beam Sputtering tools (MBS), **JEOL** (Japan) and **Multibeam** (USA) and their e-beam lithography systems, **Thermo Fisher** (USA) and its focused ion beam and electron microscopy systems, **Veeco Instruments** (USA) and its lithography, MBE, CVD, PVD,

ion beams, ALD and dicing systems, **Aixtron** (1983, Germany) and its CVD systems, **NuFlare** (Japan) and its mask writers and epitaxial growth reactors, **AJA International** (1989, USA) and its thin film deposition systems including magnetron sputtering, e-beam evaporation, thermal evaporation, and ion milling systems and **Denton Vacuum** (1964, USA) and its evaporation, sputtering, PE-CVD and ion beam deposition tools.

2.4.5 PDK

Chips design and manufacturing are specified using a **Process Design Kit** (PDK), which is a set of files and software tools used to specify, develop, simulate and then manufacture integrated circuits using a specific manufacturing technology such as FDSOI (Fully Depleted Silicon on Insulator) or for manufacturing superconducting qubit chips.

A PDK typically includes the following items:

- Design Rule Manuals (DRM) documenting the general geometric and physical rules of the circuit and indicating how to arrange components and their interconnections on the chip, to ensure that the layout meets the constraints of manufacturability, reliability, and process performance.
- Geometric description files of the basic components of the circuit such as transistors, resistors and capacitors (size, shape, spacing).
- Electrical models SPICE (Simulation Program with Integrated Circuit Emphasis) representing precise mathematical models of transistors and other components behavior in the chip.
- Design Rules Check (DRC) and Layout Versus Schematic (LVS) verification tools that are used to validate that the circuit layout meets the manufacturing specifications in terms of spacing and dimensionality from the DRM, while the LVS ensures that the electrical schematic matches the logic diagram of the circuit.
- Standardized cell libraries (or Standard Cells) supporting basic logic functions.
- Elements to generate realistic numerical performance simulations.
- Elements related to the Design of Experiment (DOE), which specifies methods for characterizing and optimizing manufacturing processes. It defines the optimal manufacturing parameters that achieve the expected performance. This makes it possible, among other things, to adjust the content of the SPICE models, design rules, and electrical models included in the PDK by defining realistic boundary conditions for process tolerances.

2.4.6 EDA

Electronic design automation (EDA) software tools running on classical computers are unsung heroes of semiconductor advances [3472]. They kept pace with the growth of chips complexity and come from Cadence, Synopsys and Siemens (formerly from Mentor Graphics) to name a few vendors, in a market that is being consolidated.

One famous tool to design and even test your own superconducting chip is Quantum Metal (formerly IBM Qiskit Metal), that was announced in 2021 [3473]. In February 2023, Amazon AWS introduced Palace (PArallel, LArge-scale Computational Electromagnetics), a finite element open-source code for full-wave electromagnetics simulations capable of simulating a single transmon qubit with its readout resonator coupling and a terminated coplanar waveguide (CPW) transmission line for input/output [3474]. A similar tool, QuantumPro, was launched by Keysight in August 2023. Synopsys QuantumATK runs atomic-level modeling and simulations using machine learning techniques. It can help simulate the characteristics of interfaces between superconductors and insulators in superconducting materials.

Cadence tools are used to design spin qubits and control electronics chips like with IQM [3475]. Qubit designers usually assemble their own suite of multiscale EDA tools ranging from the physics of the qubits at low level to the whole behavior of chip circuits and, in between, for designing specific parts of these circuits like Josephson junctions, resonators [3476] or couplers [3477] in the case of superconducting qubits, or, for example, of readout lines for quantum-dot spin qubits [3478].

Tools frequently mentioned include Sonnet ABS (Adaptive Band Synthesis), Ansys HFSS 3D High Frequency Structure Simulation Software Multipurpose that helps the design and simulation of high-frequency electronics and Ansys RaptorQu which is used for electromagnetic simulations of superconducting qubit circuits, and Dassault Systèmes CST which also simulates electromagnetic fields in circuits. Drawpy is a Python framework based on HFSS that creates circuits drawings. SPICE is an open-source software used to digitally simulate analog circuits. Qplacer is a superconducting qubit placement software framework from Duke University, with MIT and Arizona State [3479]. At a higher level, Synopsis Technology Computer-Aided Design (TCAD) helps design a whole circuit. Machine learning can also be used to define the parameters of superconducting circuits, leveraging then Quantum Metal for simulation [3480], and even LLMs [3481]. Quantum computing could even be used to simulate parts of the manufacturing process like EUV-based photolithography [3482].

One challenge here is to create software suites able to implement digital twins of qubit chips in a full-stack manner, from the lower quantum physics level at the atomic scale, up to all the circuitry, including time domain effects [3483] and various material defects and

noise models [3484]. This is labeled "Quantum Design Automation" [3485], or Q-EDA, a concept well framed by Cai et al. in 2026 [3486–3488]. At the atomic scale level, we are using quantum physics digital simulations using DFTs and other classical methods, and, in the future, quantum algorithms. At the circuit level, simulations use various methods: Method of Moments (MoM) for planar and stacked planar structures [3489], Finite Element Method (FEM) for 3D structures and Finite Difference Time Domain (FDTD) for handling large problems [3490].

A team at Stanford University implemented a machine learning gradient-based optimization of superconducting circuit design using SQcircuit software package [3491]. Another team, at Oxford University, is using machine learning to optimize the design of SiGe qubits [3492].

At the highest abstraction level, circuit designers are using MBSE (Model-Based System Engineering) and ESL (Electronic System Design) methods as well as the SysML (System Modeling Language) for the creation of product specifications. Also, Automatic Test Pattern Generation (ATPG) tools are used to model circuit defects. Then, you can build optimizers to find the best parameters for your superconducting qubits, like what a team in China did with its SuperGrad Python toolkit, first posted in 2024 and updated in 2025 [3493].

Conductor Quantum

UK, 2024, $500K

The company was created by Brandon Severin who got a PhD from Oxford University specializing in AI for quantum computing in silicon, and Joel Pendleton who worked previously at Quantum Motion, C12 and QuantrolOx. It builds AI-based software for the automated tuning and calibration of silicon spin qubits, aiming to replace the days or weeks of manual bring-up per device. It went through Y Combinator in 2024 and relocated to San Francisco, and partnered in November 2025 with SemiQon, the VTT spin-out, which supplies the silicon chips.

NanoAcademic Technologies

Canada, 2008

NanoAcademic Technologies is a company created by Hong Guo from McGill University and Yu Zhu and Leil Liu (all coming from China) which sells quantum materials software simulation tools like NanoDCAL. It is used to simulate the physics of quantum chips like superconducting qubits. In 2023, it introduced QTCAD, its spin-qubit modeling tool.

QuantCAD

USA, 2021

QuantCAD is a company created by Michael Flatté and based in Iowa that develops and sells CADtronics and qNoise, a suite of simulation software that models noise and current in quantum devices. It is used to design various quantum components, including quantum sensors and optoelectronic devices.

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This **Fab and manufacturing tools** subsection contains 82 bibliographical references and notes containing at least 2,584 pages.

2.5 Other enabling technologies vendors

These companies are developing physical components and enabling technologies that can play a role in building quantum computers.

More often, as this market remains limited to research, these startups are more generalist and target broader markets than quantum computing, covering physics research in general and even various industrial applications.

Advanced Quantum

Germany, 2022

Advanced Quantum is a spin-out from the 3rd Institute of Physics at the University of Stuttgart.

It provides consulting services on NV-center technology, sells confocal characterization microscopes and magnetic-field scanners. It also created several classroom kits for studying NV-center sensing, covering optics, microwave electronics, fluorescence detection, single-photon and lattice interactions, Zeeman splitting and EPR pulse sequences, with a software interface. They are also involved in the StarQ DLR project in Germany, on developing surface processing of diamonds at atomic resolution. Its goal is to improve the quality of diamond qubit systems for QPUs [3494].

Aeponyx

Canada, 2011, $11.4M

Aeponyx is a fabless micro-optical switch semiconductor chips designer and manufacturer, specialized in Micro-Electro-Mechanical-Systems (MEMS) and silicon-nitride based silicon photonics.

Alter Technology

Spain-Germany, 2006

Alter Technology is a subsidiary of the German group TÜV NORD specialized in micro and optoelectronics engineering for space and harsh environment applications. It has labs in UK, France, Spain and Italy. They develop several quantum enabling technologies like frequency-stabilized lasers used to control cold atoms, an ion-trap chip carrier, entangled sources of photons for space based QKD, a squeezed light quantum MEMS gravimeter.

AuroraQ

Canada, 2017

AuroraQ creates communication systems based on superconducting qubits, including quantum communication repeaters. It is complemented by the QSPICE Design software which allows the design of superconducting quantum circuits. In other words, this is an ultra-niche market [3495]. QSPICE is a derivative from the SPICE open-source project ("Simulation Program with Integrated Circuit Emphasis") used to digitally simulate analog circuits.

Elemental Instruments

Australia, 2020

Elemental Instruments is a provider of high-precision magnetic field sources used for example in quantum spin technologies like diamond microscopes.

Hummink

France, 2020

Hummink developed a patented technology combining a nanometric "pen" with an oscillating macro-resonator to perform a capillary deposition of various liquids. It can print conducting materials with an existing choice of 10 different materials. It can be used to add precision items on devices in 3D.

Labber Quantum

USA, 2016

Labber Quantum developed software solutions for controlling the qubits of experimental quantum computers with Python scripting handling electronics hardware control (AWGs, DACs, ADCs), data storage and visualization. They are used to calibrate qubits. The startup was acquired by **Keysight Technologies** in March 2020.

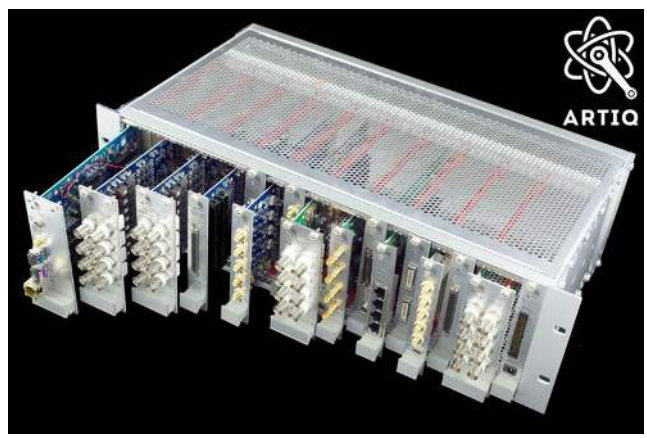

Figure 456: M-Labs ARTIQ system

M-Labs

Hong Kong, 2007

M-Labs, formerly known as Milkymist, was founded by the French engineer Sébastien Bourdeauducq.

It developed ARTIQ (Advanced Real-Time Infrastructure for Quantum physics), a system that combines hardware and a real-time operating system to control quantum computer hardware based on trapped ions. It is a bit like the trapped ions counterpart of Quantum Machines. They developed their own FPGA circuit for ARTIQ, all programmed in Python. ARTIQ was developed with the Ion Storage Group at NIST (USA), which

works on trapped-ion qubits. In 2026, US scientists from Duke University and the University of Maryland developed a multi-agent LLM system that created the code for ARTIQ while enforcing experiment boundaries, to build out the calibration routines controlling a mixed-species trapped-ion crystal containing $^{40}Ca^{+}$ ions together with $^{40}CaOH^{+}$ molecular ions, the latter forming through reactions with background gas [3496].

Meca Magnetic

France, 1963

Meca Magnetic produces magnetic shielding targeting various markets, focused on scientific markets and including quantum technologies. It creates nickel–iron soft ferromagnetic alloy Mu-metal shields.

Nano-Meta Technologies

USA, 2010

Nano-Meta Technologies is a spin-off from the University of Perdue that aims to create a quantum information storage system. It is in fact a private contract research laboratory. It commercializes intellectual property on technologies associating photonics and nanomaterials that could be used in quantum cryptography systems.

ParTec

Germany, 2001

ParTec is a supercomputer and quantum technologies integrator also involved in software tools development, including the creation of a digital twin for superconducting qubits [3497]. It participates in the European HPCQS project. It provides solutions to connect classical hardware to QPUs as part of the German project QSolid. It also developed with Quantum Machines QBRIDGE, to integrate HPC workflows and QPUs which was deployed at the Israeli Quantum Computing Center (IQCC) in 2024, along with a chip from QuantWare. The company is also investing €5 M in the buildup of a production facility for the assembly and testing of cryogenic and non-cryogenic systems.

This kind of player opens a book of questions on the future QPU players business models and supply chains. Will they become "chip" vendors, leaving the field of integration to players like ParTec, or will they remain full-stack R&D and integration players like what most QPU vendors do today? My view is that it will depend on the market size and diversity of technologies to integrate. Also, QPU vendors will be better off capturing as large a share of the QPU build-up value as they can, by acting as prime contractor for end-user customers.

QBee.eu

Belgium, 2020

QBee.eu is a sort of quantum accelerator or incubator created by Koen Bertels, who also leads the Quantum Computer Architectures Lab in TU Delft and also works at QuTech. They run various research projects like defining a quantum micro-architecture for quantum accelerators using the OpenQL language from TU Delft, a quantum computing emulator, quantum genomics, quantum chemistry [3498], and quantum finance plus some services in education and consulting.

QFX

UK, 2024, €2.2M

QFX is a quantum hardware startup spun out of the University of Oxford which is developing modular atomic sources for trapped-ion and neutral-atom quantum computing. It was created by Timothy Ballance (CEO), Joseph Goodwin (CTO), Laurent Stephenson (CSO) and Peter Drmota (Chief Innovation Officer). Joseph Goodwin had collaborated with the team of Oxford Ionics [1841]. Their flagship product is the Miniature Atom Source (MAS) [1891]. It is an oven with a 6 mm diameter by 6 mm long UV fused silica body with encapsulated source metal, conductive and radiative thermal isolation, and an integrated beam collimator, heated by a low-power continuous-wave laser rather than by resistive current. It also develops sensing and communications platforms.

Q-Lion

Spain, 2019

Q-Lion develops an error correction code solution for trapped ion qubits. The startup is a spin-off from the Bank of Santander's Explorer incubation program. It was created by Andrea Rodriguez Blanco, who was still working on a thesis in 2020.

QuantTera (2005, USA) is a contract R&D company created by Matt Kim that develops nano-engineered photonic devices targeting photonic telecommunications and wireless applications. It is mainly using silicon-germanium based photonics. It says it targets quantum applications, with no details.

TreQ

UK, 2023, $5M

TreQ is a manufacturing company that builds and operates quantum computing clusters. They appear to operate as a system integrator, in the same category as ParTec. They say that they collaborate with small and medium enterprises (SMEs) which provide unspecified components.

In 2025, TreQ opened its UK headquarters and production facility at Milton Park Innovation Centre in Oxfordshire, in order to deploy its first QPU in 2025. It launched Compass SG25B (Figure 457), a system made of a Bluefors Ultra Compact LD cryostat, plus control electronics from Qblox, calibration tools from

QuantrolOx and unspecified technology from Rigetti (maybe their 9-qubit Novera chip). They then got £1.65M from Innovate UK to develop an Open Architecture Quantum (OAQ) Testbed along with Rigetti, Oxford Ionics, Q-CTRL, and Qruise.

Figure 457: TreQ Compass SG25G is built around a Bluefors Ultra LD cryostat.

S-Fifteen Instruments

Singapore, 2017

S-Fifteen Instruments is a spin-off from CQT that develops qubit control systems, entangled photon sources, single-photon detectors and quantum cryptography solutions covering QKD and QRNGs.

Spectrum Instrumentation

Germany, 1989

Spectrum Instrumentation is selling AWG and digitizers that are used in quantum research, particularly for controlling cold atom quantum computers AODs and AOMs used for shuffling and sorting atoms as well as trapped ions systems. In that latter case, EleQtron (Germany) is one of their customers, using their AWG PCIe cards.

Star Cryoelectronics

USA, 1999

Star Cryoelectronics, *aka* STARCryo, creates SQUIDs sensors used mostly in quantum sensing and other cryoelectronics products (cables, connectors, ...). It also produces transition edge sensor (TES) and superconducting tunnel junction (STJ) X-ray detectors.

Vapor Cell Technologies

USA, 2020

Vapor Cell Technologies provides alkaline atom capsules, mainly rubidium, for use in various miniaturized solutions using cold atoms [3499]. The company was founded by Doug Bopp, a former NIST researcher from Boulder, Colorado.

Zyvex Labs

USA, 1997

Zyvex Labs develops atomically precise manufacturing (APM) solutions based on STM (Scanning Tunneling Microscopy) that can be used to produce components for use in quantum computing (such as the deposition of dopants for superconducting qubits and silicon) and quantum metrology.

They were funded by NIST, DARPA and the Department of Energy SBIR research programs. The company was founded by Jim von Ehr. Zyvex announced in September 2022 a sub-nm version of its STM solution, the ZyvexLitho1.

2.5.1 Bibliography and notes

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2.6 Raw materials

For any new hardware technology, it is now common practice to wonder about its environmental friendliness. We've already been dealing with the energetic dimensions of quantum computing. Another key aspect to investigate is the raw materials that are used. What are their sources of supply, their global reserves, their economic and environmental extraction cost, consumable raw materials if any, and finally, the recycling processes of these materials? I propose here a first broad inventory of the raw materials used in and around quantum technologies of all types, particularly in quantum computers. This is a screening-level materials inventory, not a life-cycle assessment and not a complete supply-chain analysis. It covers the elements and isotopes that end up in the hardware, and it omits process gases, solvents, photoresists, process water, packaging, the surrounding classical electronics and end-of-life treatment. Any environmental conclusion drawn from it is incomplete. All these elements are positioned in an in-house annotated Mendeleev periodic table of elements, Figure 458 [3500].

We mainly have two types of materials to study: those used in qubits and the supplemental materials, particularly for cables and other supporting structures as well as the gases used in cryostats, mostly ^{3}He and ^{4}He. The materials used in qubits are sometimes quite rare (strontium, ytterbium, beryllium). Their selection is based on their energy transitions which correspond to laser or microwave wavelengths that can be used practically with market sources.

Other constraints explain their choice such as the stability of some of these energy levels. Some materials are very rare but their needs in quantum technologies remain marginal in proportion to their production and world consumption. This is at least the case unless millions of quantum computers using them are manufactured. We are not yet at the stage where the consumption of certain elements would come mostly from quantum technologies, as may be the case for smartphones concerning certain rare earths and minerals such as the famous coltan. Coltan is the contraction of columbite-tantalite. It is used to recover tantalum and niobium. If it is an important source for tantalum, it is in fact secondary for niobium compared to other minerals [3501].

How about rare earth elements? Out of the 17 elements in that category who mainly sit in the lanthanum row in Mendeleev's elements table, about 6 of them are used in quantum technologies: yttrium, praseodymium, dysprosium, europium, erbium and ytterbium, the latter two being commonplace in trapped ions computing.

In July 2022, Türkiye announced the discovery of large reserves of rare earths minerals potentially exceeding China's reserves. But the announcement was probably overstated, preprocessed minerals getting out of mines and rare earth oxides being produced after separation [3502, 3503].

One differentiating aspect of quantum technologies relates to the isotopes used which are sometimes the rarest of their elements. This is the case for helium (^{3}He) used in cryogenics below 4 K or for cesium (^{133}Cs) for atomic clocks or rubidium (^{87}Rb) in cold atoms. Silicon (^{28}Si) is used in silicon qubits and, although it is the most abundant isotope, requires costly refining. Carbon (^{12}C) is also used in nanotubes like with the startup C12 Quantum Electronics, while ^{13}C (^{13}C) is used in some NV center structures. Some of these isotopes are purified with centrifugal separation, a technique well known in nuclear physics, both civil and military.

As noted above, this inventory does not cover the consumables used in semiconductor production, such as fluorine compounds, process gases, photoresists and solvents, of which there are many, nor the water and energy used in the fabs.

We will also not deal with the recycling of quantum computers, an issue that has not yet arisen due to their current very limited number. However, it can be reduced to the more generic issue of recycling various electronic devices.

This part deals mainly with technical considerations. Specialized academic work addresses the geopolitical aspects [3504, 3505].

2.6.1 Helium

Helium is a great paradox in the table of elements. It is the second most abundant element in the Universe after hydrogen. Nuclear fusion does the rest to create all the other elements in first- and second-generation stars. Yet, this element is quite rare on Earth and its reserves are dwindling. It is a noble, inert gas that does not interact chemically with any other element because its electron layer is complete with two electrons. Lighter than air, it tends to leave the atmosphere.

Helium applications. Helium exists in two isotopes: ^{4}He and ^{3}He, the less abundant being the latter. ^{4}He is used in cryogenic systems needing temperatures from 1.8 K to 5 K. It is used to cool superconducting magnets in MRI systems and at the CERN LGC at around 4.5 K. One experiment uses 9 T magnets that are cooled to 1.8 K with 18 kW cryostats that handle 120 tons of ^{4}He. ^{3}He is needed, in combination with ^{4}He, in the dilution refrigerators reaching temperatures in the 10 mK to 1 K that are needed for cooling superconducting and electron spins qubits chips. Helium is used besides cryogenics in many other industry applications like for semiconductor manufacturing. It is also used in inflated balloons. A typical dilution-based cryostat requires 15 to 18 liters of ^{3}He gas for a little over 100 liters of ^{4}He gas! As of 2026, ^{4}He is priced at around €20 per liter of gas while a liter of ^{3}He gas sits between €2,000 and €3,000. Both prices are volatile and contract-dependent. The gases are purchased separately and mixed at the right dosage by the manufacturer of the dry cryostat. At

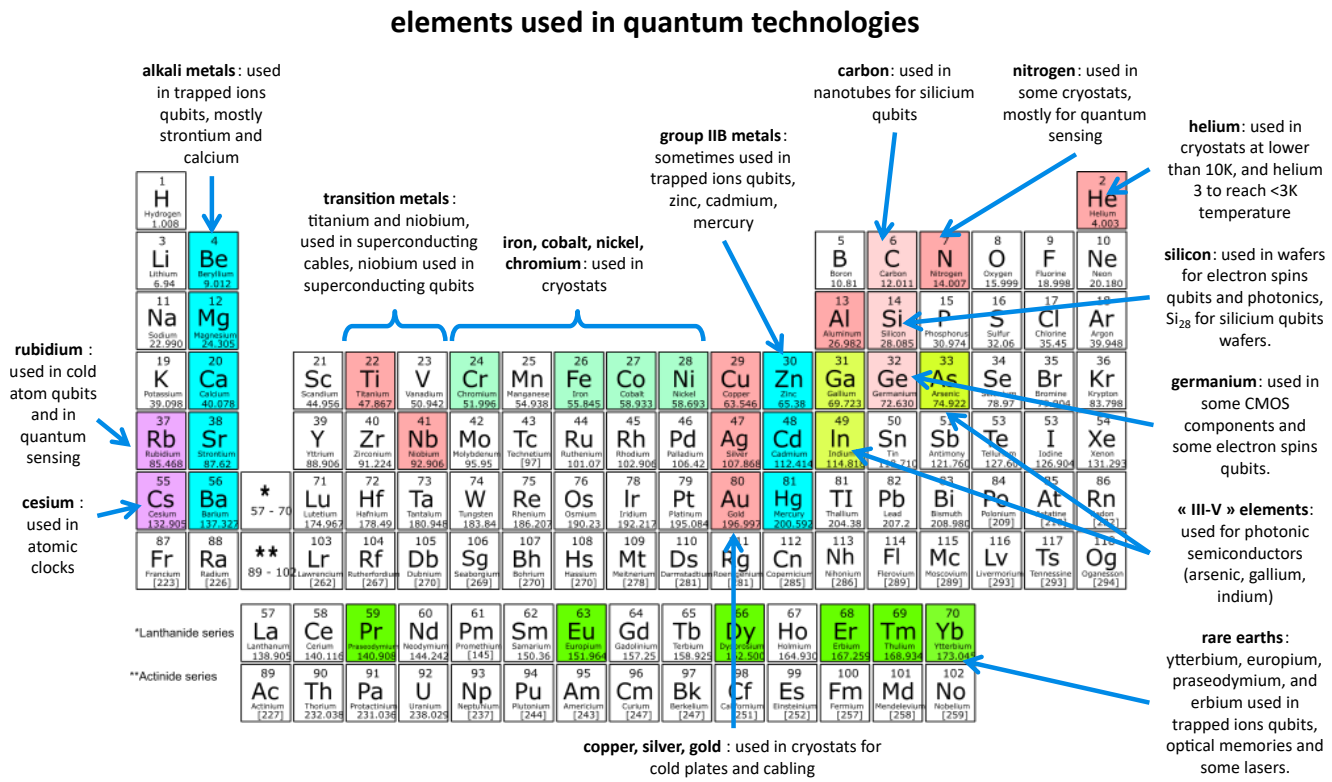

Figure 458: Table of elements and those which are used in quantum technologies. Olivier Ezratty, 2021-September 2026.

the end, it is therefore necessary to pay at least €30,000 to €40,000 of ^{3}He and ^{4}He per dry cryostat, and just for a NISQ system. ^{3}He is also exploited in various specialized applications: in neutron detectors used in security systems, in oil exploration, in medical imaging and in nuclear fusion research.

Helium reserves. The worldwide reserve of ^{4}He is estimated at about 35.2 billion cubic meters, held in natural gas reserves located in Qatar, Algeria, Russia, the USA, Canada, Tanzania and China. Worldwide helium consumption sits around 160 million cubic meters per year, above 25,000 tons [3506, 3507]. Dividing one by the other provides a static reserve-to-production ratio of about 220 years [3508]. The ratio has been updated repeatedly over the past two decades and depends on multiple factors, including demand predictions.

^{4}He production. Helium is generated deep underground via the alpha decay of heavy radioactive elements, primarily uranium and thorium. Due to its low atomic mass, most helium escapes through the Earth's crust into the atmosphere and is lost to space [3507]. It can be trapped in some impermeable rock formations, accumulating with natural gas, primarily methane (CH_4). Helium extraction requires a natural gas field with a helium concentration of at least 0.3% by volume [3509]. The extraction process uses cryogenic fractional distillation with the natural gas stream being pressurized and cooled to condense the heavier hydrocarbons. The output known as crude helium is made of 50% to 80% helium, with the remainder impurities mixing nitrogen, argon, neon, oxygen, and traces of hydrogen.

Purifying helium is done in two stages. One named Pressure Swing Adsorption (PSA) where crude helium gas is passed through beds of activated carbon or synthetic zeolite at high pressure. Impurities like nitrogen and oxygen selectively adhere to the adsorptive materials, allowing the purified helium gas to pass through. Then, some additional steps are used to remove hydrogen, based on chemisorption or catalytic converters [3508]. Traces of hydrogen interfere with dilution-refrigerator operation. When the ^{3}He–^{4}He mixture is expanded through the capillary tubes of the dilution circuit, the temperature falls below the hydrogen freezing point, solid hydrogen accumulates and can block the serpentine micro-tubes, requiring the system to be warmed to clear the blockage.

Helium Grade A (4.7) is the standard commercial threshold for high-tech manufacturing, offering a minimum purity of 99.997% in helium, both isotopes combined.

Air Liquide is one of the major players in this global market, operating a large ^{4}He extraction and production unit in Qatar, linked to their gas operations.

^{3}He production. Whatever the production method, ^{3}He is a very scarce resource. Its supply is highly constrained, inherently inelastic, and closely regulated by national energy and defense departments [3510]. ^{3}He production can be done using three main methods, with two additional potential ones, with different practical and economical trade-offs [3511]:

- **Isotopic purification** using ^{3}He that is present in natural gas reserves at a very low natural ratio

of $\approx 10^{-7}$ to 10^{-8} relative to ^{4}He. When liquid ^{4}He is cooled below its lambda point ($T_\lambda \approx 2.17$ K), it undergoes a phase transition into a superfluid state, characterized by zero viscosity. ^{3}He, however, remains a normal fluid at these temperatures, its own superfluid transition occurring at a much lower temperature, in the millikelvin regime. In the laboratory, passing the isotopic mixture through a porous medium with microscopic channels, such as tightly packed jeweler's rouge powder or porous Vycor glass, known as a superleak, lets superfluid ^{4}He flow through without friction while the normal ^{3}He fluid is held back by its own viscosity. This is a laboratory enrichment and separation principle, not an industrial extraction route: no superleak is used to pull ^{3}He out of a natural gas stream at scale. Industrial isotopic separation instead relies on ultra-low-temperature fractional distillation. Because ^{3}He possesses a higher vapor pressure than ^{4}He at a given temperature, boiling a liquid mixture results in a vapor phase highly enriched in ^{3}He. This process is performed repeatedly in specialized packed distillation columns operating near 1.5 K to achieve high isotopic purity before final bottling. Because extracting ^{3}He directly from natural gas is economically prohibitive for bulk supply, world ^{3}He supply comes almost entirely from nuclear-derived recovery, mainly tritium decay, with cryogenic distillation and final polishing applied downstream. A supplier claiming a ^{3}He product should be asked for its actual process chain, since the feedstock origin, the enrichment steps and the final purification are distinct stages.

- **Tritium radioactive decay**. Historically, the largest reserves of ^{3}He were harvested as a byproduct of maintaining nuclear weapons stockpiles, where tritium is continually replaced as it decays over time. Tritium is a heavy isotope of hydrogen with a half-life of 12.32 years with gradually disintegrates to produce ^{3}He as shown in Figure 459. The captured decay gas is chemically scrubbed of remaining hydrogen (tritium) using heated palladium beds, leaving pure ^{3}He behind.

- **Harvesting from heavy-water power reactors**, through tritium generation with irradiating lithium or with tritium-controlled decay in specialized nuclear facilities, such as those controlled by the US Department of Energy. Tritium is an isotope of hydrogen with one proton and two neutrons. ^{3}He is produced at the U.S. Department of Energy's Savannah site in South Carolina [3512] (Figure 460) and at a Canadian CANDU power plant [3513].

- **Nuclear fusion reactors byproduct**. ^{3}He would be a byproduct of some deuterium-deuterium or deuterium-^{3}He fusion schemes. This is prospective: no fusion plant produces net power today, and the recovery rate, purification chain and cost of extracting ^{3}He from a fusion exhaust stream are unestablished.

- **Lunar regolith mining** is also prospective. Lunar ^{3}He concentrations are of the order of a few parts per billion by mass, so very large volumes of regolith must be excavated and heated per liter of gas recovered. The binding constraints are the energy required for thermal extraction, the recovery rate achieved in practice, the mass and maintenance of the surface hardware, and the cost of return transport to Earth. Two US startups, Intelune and LH3M, are exploring this route and are detailed below.

Intelune

USA, 2020, $25M

Intelune is developing technologies to harvest ^{3}He both from lunar regolith and Earth-based helium sources, supported by funding from the U.S. Department of Energy, NASA, and the NSF. The company was created by former executives from Blue Origin. The first mission to the Moon was planned for 2027 and production supposed to start by 2029.

Meanwhile, they will use more traditional production methods or procurement. In 2026, Intelune disclosed that it demonstrated its "Cold Capture" technology in 2025 which can produce 99% pure ^{3}He from Grade A helium using cryogenic separation methods. Grade A helium corresponds to a commercial classification for highly purified industrial helium that has a guaranteed minimum purity of 99.997%, the most common contaminant of helium being hydrogen. It contains traces of ^{3}He. It is equivalent to a generic gas purity of grade 4.7, meaning four nines and a seven. Cold Capture is an addition to existing helium liquefaction plants and recovers ^{3}He from ^{4}He liquefiers using cryogenic distillation.

In September 2025, Intelune announced a partnership with Bluefors, which makes a lot of sense even though Bluefors will have to be patient.

LH3M

USA, 2025

LH3M (Lunar Helium-3 Mining) is a company created by Chris Salvino (CEO and Chief Engineer) which competes with Intelune. It wants to detect and harvest ^{3}He on the Moon for two main markets: nuclear fusion and quantum computing. They provide some information on the engineering of harvesting and how to send back ^{3}He on Earth. They would establish a human base on the Moon to operate it. A rocket is supposed to send ^{3}He back to earth. Given the heavy price tag of ^{3}He, they might have to create some low-Earth orbit space force to fight against any potential space pirates who would steal their ^{3}He as their vessels would reenter the atmosphere.

Their market projections are very large, with $119B for helium alone and $17T for a ^{3}He fusion market, neither being dated or reconciled with projected FTQC revenue. They also appear to discount the mainstream fusion ap-

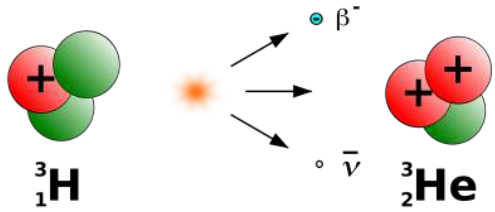

Figure 459: ^{3}He is a by-product of tritium, an isotope of hydrogen with two neutrons.

Figure 460: Savanah River Site is one of the few places where helium 3 is produced in the world.

proach, which uses deuterium and tritium, with tritium bred by exposing lithium to fusion neutrons, as planned at ITER. The company is therefore dependent on two technology programs whose timelines are themselves unsettled, in addition to its own. Meanwhile, they have validated 5 patents which may be a good starter.

2.6.2 Silicon

Silicon is the key element in many semiconductor components used in or around quantum processors. While being the second most abundant element in the Earth's crust after oxygen, the silicon used in semiconductors comes from a few quartz mines. This is because quartz is composed of at least 97% silicon, which is easier to refine. After chemical-based refinement, silicon is turned into large cylindrical ingots which are then sliced into thin wafers. Wafers are then processed in semiconductor fabs with transistors that combine silicon oxide and different doping materials such as hafnium.

Silicon qubits require using ^{28}Si, because the null spin of its nucleus does not interfere with the spin of the trapped electrons used as the qubit observable. The silicon wafers on which the qubits are covered with a thin layer of ^{28}Si. ^{28}Si is the most abundant isotope, at about 92.2%, while the spin-carrying ^{29}Si represents about 4.7%, which is the fraction that enrichment aims to remove.

^{28}Si made headlines in 2010 when some German researchers created a perfect crystal ball made of ^{28}Si to accurately determine the Avogadro number, which determines the number of elements, here atoms, in a mole [3514]. ^{28}Si was obtained by centrifuging silicon fluoride (SiF4) gas, then transformed into SiH4 which was then used to create the crystal by vacuum deposition of purified silicon. All this was carried out in different laboratories in Russia, in Nizhny-Novgorod and Saint Petersburg. The researchers involved also came from Italy, Australia, Japan, Switzerland and BIPM in France, from their respective weights and measures offices. The tests were carried out on a 5 kg sample at a cost of €1M. In 2014, an American team improved the purity of ^{28}Si to 99.9998% with pumping silicon ions in a magnetic field, allowing it to be separated by mass [3515].

This continued in 2017 with 99.999% [3516] ^{28}Si produced by a team of Russian and German researchers. The interest of ^{28}Si was to allow a precise counting of the number of silicon atoms in the mass considered, because of its perfect crystal structure, dimensioned by X-ray interferometry. The Avogadro number determined by the 2010 experiment was $N_A = 6.022\,140\,84(18) \times 10^{23}$. The ambition of these two projects was to create a new material standard of the kilogram, the 1889 material standard preserved in France being degraded by oxidation.

Finally, in 2018, the Avogadro number was redefined in the international measurement system as a fixed constant of $6.022\,140\,76 \times 10^{23}$ mol^{-1}. Indirectly, however, these two experiments did advance the know-how of ^{28}Si purification, at a time when its interest in creating silicon qubits was barely in the radar. What a good illustration of serendipity in science!

Silicon purification process involves the production of silicon tetrafluoride (SiF4) of all isotopes. Enrichment in ^{28}Si is carried out in a centrifuge, originally at the Central Design Bureau of Machine Building in St. Petersburg, in fact, a former plutonium enrichment plant reassigned for this use in 2004.

The gas was transformed into silane (^{28}Si H_4) at the Institute of Chemistry of High-Purity Substances of the Russian Academy of Sciences in Nizhny-Novgorod. It was then be deposited by vapor deposition (CVD) on silicon, releasing hydrogen. The resulting ingot could then be stretched to create a perfect crystalline silicon ready to be sliced into wafers. CEA-Leti researchers were working with Russian teams at Nizhny-Novgorod on the process for vacuum deposition of ^{28}Si on 300 mm wafers [3518].

In October 2021, **Orano** announced its plan to produce ^{28}Si in France, in the form of SiF_4 (tetrafluorosilane), which started in 2023.

Likewise, **Silex Systems** (Australia) got an AUS $5.1M funding from the Australian government in 2023 to also produce ^{28}Si (in the form of silane) using a laser enrich-

Figure 461: ^{28}Si was initially produced to create a replacement for the reference kilogram used in the international metric system, as a way to determine the Avogadro number. Source: PTB, 2010 in [3517].

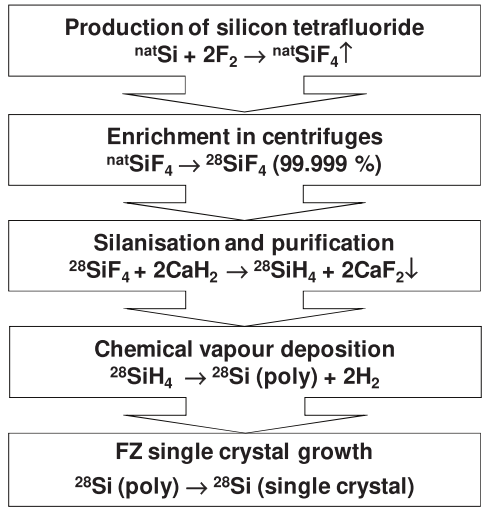

Figure 462: Description of the silicon 28 isotope chemical and mechanical purification process. Source: [3516].

ment technique targeting 99.998% purity, this being a target rather than a qualified production figure. **Urenco** (The Netherlands) is also producing rare isotopes including ^{28}Si, like **Lawrence Semiconductor** (USA) which also produces ^{28}Si, quoted at 99.95% purity as of 2026.

Air Liquide was partnering with the Nizhny-Novgorod laboratory for this process of CVD (chemical vapor deposition) of ^{28}Si on a 30 to 60 nm thin film that is 99.992% pure [3519] above a conventional silicon wafer. Nowadays, these partnerships with Russia are gone.

Air Liquide now transforms SiF_4 (tetrafluorosilane) into $SiH4_4$ (silane) ready for silicon epitaxy process in a US production plant.

ASP Isotopes

South Africa-USA

ASP Isotopes is a company historically in the uranium purification business. This holding owns Quantum Leap Energy (USA/UK, which produces nuclear like HALEU, Lithium 6 and 7, Chlorine 37) and PET Labs (Afrique du Sud). They produce various isotopes of ytterbium, carbon, silicon, germanium and other elements. They use Aerodynamic Separation Process (ASP) which separates gas species and isotopes in a volatile state via an approximate flow pattern as shown below. They then use quantum enrichment which uses lasers to selectively ionize and separate isotopes with high precision, a method adapted to the enrichment of elements that are in a solid form or are not easy to transform into gases.

2.6.3 Germanium

Germanium is a group IV semiconductor metalloid, like silicon, and can be used alongside III-V materials. It is used in many fields: in photonics, in SiGe heterojunction bipolar transistors which are used for the amplification of weak microwave signals as well as in electron spin qubits chips.

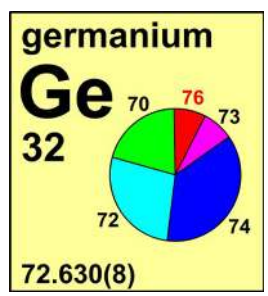

Figure 463: Germanium natural isotopes distribution.

With spin qubits, the point of isotopic purification is the opposite: ^{73}Ge, at about 7.7% natural abundance, is the only stable germanium isotope with a nonzero nuclear spin, so it is the one that must be removed. Enrichment targets the spin-zero isotopes, typically ^{70}Ge, ^{72}Ge or ^{74}Ge, to give the electron spin a magnetically quiet host. Germanium is generally extracted from zinc ores and also from zinc-copper ores. In 2019, 130 tons of germanium were produced, with China the main supplier at 85 tons [3520]. These are 2019 figures and Chinese export controls have applied since 2023. Reserve estimates vary widely and sit at approximately 9,000 tons, mainly located in China, Canada and the USA. Along with gallium and indium, which are also III-V materials, germanium is considered a critical resource. Isotopic purification of germanium is carried out by the same

Figure 464: Rubidium in the molten state. Source: Wikipedia.

Figure 465: Niobium is a relatively cheap metal at $82 per kilogram as of September 2025.

Russian teams at Nizhnii Novgorod as those producing ^{28}Si, ^{74}Ge being of particular interest (Figure 463).

It uses centrifugation of germanium tetrafluoride, along the same lines as the silicon tetrafluoride route shown in Figure 462 [3521].

2.6.4 Rubidium

Rubidium is an alkali metal used to create cold atom qubits that are excited into highly energetic Rydberg states.

It is also used in quantum sensing, notably to create atomic clocks and micro-gravimeters. It is an alkaline, soft, silvery metal with a melting temperature of only 39.3°C (Figure 464). In a neutral atom computer, the metal is used very sparingly. It is supplied in ampoules of a few solid grams.

It is heated in a small box to be sublimated into gas which then feeds the vacuum chamber where the lasers will trap individual atoms. As of 2026 the metal costs about $85 per gram and about $1,600 per 100 g, depending on grade and supplier. It is readily available from chemical companies. Only about 5 tons are produced annually worldwide, in China, Canada, Namibia and Zimbabwe. It is a by-product of the extraction of cesium and lithium. The isotope ^{87}Rb is the most used and represents 27.8% of natural rubidium. It is radioactive but with a half-life longer than the age of the Universe, so it is very stable. World reserves are estimated at 100,000 tons, which at the current production rate gives a large static reserve-to-production ratio.

2.6.5 Niobium

Niobium is a transition metal used in superconducting qubits as well as in microwave cables driving superconducting and electron spin qubits. **CoaxCo** (Japan) is the leading supplier of these NbTi coaxial cables, though not the only one, KEYCOM also supplying NbTi assemblies. They are expensive, of the order of $3,000 per half-meter segment as of 2026, and the number needed per qubit depends on the architecture, typically a drive line, a flux line and a shared multiplexed readout line between the 4 K and 15 mK cold plates.

In industry, it is used in the production of high-strength special steels, in superconducting magnets, in particle accelerators, in arc welding, in bone prostheses associated with titanium, in optics, as a catalyst for rubber synthesis, in aircraft engines and in gas turbines.

World production was estimated at 68,000 tons per year in 2018, with Brazil accounting for 88%, followed by Canada for just over 9%, generated by a single mine. It comes from the exploitation of pyrochlore, an ore combining calcium, sodium, oxygen and niobium (Figure 465).

It is not very expensive and is priced at $82 per kilogram, but in its ferro-niobium form. Reserves are estimated at 9 million tons, a static reserve-to-production ratio of about 130 years at the 2018 production rate. But in practice, niobium is considered a “risky” resource because its demand is growing rapidly even though it comes from relatively safe geopolitical places.

2.6.6 Ytterbium

Ytterbium is a rare earth of the lanthanide series, which is used in trapped ions qubits, quantum memories, atomic clocks, doping of certain lasers and, more rarely, in cold atom qubits (Figure 466). Otherwise, it is used to reinforce certain specialized steels.

The metal is extracted from monazite, a rare-earth phosphate mineral, which contains only about 0.03%

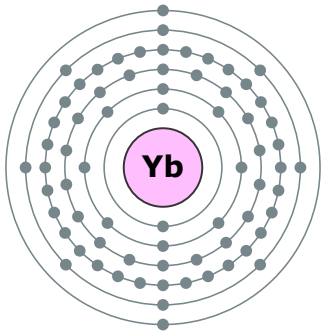

Figure 466: Ytterbium atomic structure.

Figure 467: Erbium. Its price was €229 per kilogram in September 2025.

ytterbium. Production follows a complex cycle using sulfuric acid and ion exchange. Quantum applications use isotope 171, one of the 7 non-radioactive isotopes of the element. It represents 14% of its proportion in the rocks from which it is extracted. Isotopically enriched ^{171}Yb costs considerably more than the natural-abundance metal, itself sold between $500 and $1,000 per kilogram as of 2026. Natural element supply, isotope-enrichment capacity and device-grade purification are three separate markets and should not be quoted interchangeably.

Approximately 50 tons are produced annually, mainly in China, the USA, Brazil, India and Australia, with reserves estimated at one million tons. A trapped-ion processor uses of the order of one gram.

2.6.7 Erbium

This rare earth of the lanthanide family is used in quantum memories, in some fancy cold atom qubits and in certain lasers (Er:YLF for yttrium lithium fluoride or Er:YAG for yttrium aluminum garnet). It is found in some optical fibers used in optical amplifiers (Figure 467).

Erbium intermetallics such as ErNi and Er_3Ni are also used as magnetic regenerator materials in cryocoolers, where what matters is their large heat capacity below 20 K. China is the main producer, followed by the USA. It comes from extracting xenotime (phosphate ore) and euxenite (an ore also containing niobium, titanium and yttrium). The ore is processed with hydrochloric or sulfuric acid and then neutralized with soda ash. After a bunch of chemical treatments, erbium ions are extracted by ion exchange on polymer resins.

Erbium is then obtained by heating its oxide with calcium at 1,450°C in a neutral argon atmosphere. The whole chemical route is long and expensive, and likely polluting, though carried out on small volumes. Erbium is produced at a rate of about 500 tons per year. Its price per gram is about $20 as of 2026, which is affordable to integrate it in memories or cold atoms qubits.

2.6.8 Strontium

Strontium is an alkaline earth metal, not an alkali metal, and is widely used for trapped-ion qubits. Ion qubits generally use $^{88}Sr^+$, the dominant isotope at about 83%, while ^{87}Sr, at about 7%, carries nuclear spin and is the isotope of choice for optical lattice clocks. It is used as a red dye in fireworks.

Mexico and Germany are the main producers, with an estimated world production of 220,000 tons per year and reserves of over one billion tons. It is notably used in bone anti-cancer radioactive chemotherapies.

Strontium metal oxidizes rapidly in air, as do the other reactive metals in this list, and reacts vigorously with water to release hydrogen, so it is handled under oil or inert atmosphere.

2.6.9 Gold

In quantum technologies, gold is mainly used as a thin layer covering the copper plates of the cold plates in cryostats. It prevents copper oxidation and adds good thermal conductivity. The volume used is quite small in relation to gold production and global reserves. About 3,000 t of gold are produced every year worldwide.

2.6.10 Titanium

Titanium is mainly used in association with niobium in superconducting microwave cables.

In industry, it is used for its resistance to corrosion, particularly in the aerospace industry. Some submarines have an all-titanium hull. Titanium oxide is used as a painting white pigment. It is abundant on Earth, ranking fourth among structural metals in crustal abundance after aluminum, iron and magnesium. But only a few ores contain a high enough concentration of it to make its production profitable. The main producing countries are Australia, South Africa, Canada and Norway at a rate of about 4.2 million tons per year of titanium mineral concentrates. Reserves are in excess of 600 million tons.

2.6.11 Nitrogen

Liquid nitrogen is used in cryostats to clean the gaseous helium that feeds them. It is also found in small quantities in NV Centers crystals. It is not a rare commodity. But its production in liquid form is quite energy consuming.

2.6.12 Diamond

We cover here the vendors manufacturing diamonds with defects, like NV centers.

Adamas Nano

USA, 2010

Adamas Nano sells nanodiamond particles for various use cases including NV centers-based sensors. **Bikanta** (2013, USA, $1.7M), **Cymaris Labs** (2004, USA) and **FND Biotech** (2016, Taiwan) sell fluorescent nanodiamond targeting medical imaging applications. **Diamond Materials** (2017, Germany) is a manufacturer of various variations of diamonds including NV centers. **Quantum Diamant** (Germany) also produces NV centers diamonds, for quantum sensing. It is a spin-off from TUM (the Technical University of Munich). **Photonanometa** (2011, Russia) is another producer of diamond with NV-center defects.

DiamFab

France, 2019

DiamFab is a spin-off of Institut Néel in Grenoble specialized in the growth of doped diamond layers on a diamond wafer substrate. Among other markets, they also target NV center use cases in quantum technologies. Diamond is also used as a high-performance semiconductor for power applications for diodes and field-effect transistors.

Diamond Quanta

USA, 2024

Diamond Quanta was created by Adam Khan (CEO) and Tae Sung Kim. It develops lab-grown diamond fabrication through its Unified Diamond Framework, which it says enables true substitutional doping. It creates high-performance semiconductors capable of supporting both negative (n-type) and positive (p-type) charge carriers. It is mainly focused on the development of power electronics and classical electronics but is seemingly also targeting quantum applications.

Diatope

Germany, 2021

Diatope creates diamonds with NV centers for quantum sensing and quantum computing applications. It is a spinoff from the Institute for Quantum Optics at Ulm University by Johannes Lang, Christoph Findler and Christian Osterkamp. They produce NV centers using isotopically purified ^{12}C and do provide NV centers benchmarking services.

Elementsix

Luxembourg, 1946

Elementsix is a subsidiary of De Beers Group, the world's leading diamond producer, which, among other things, manufactures synthetic diamonds for use in NV centers based systems, mostly used in quantum sensing. They hold many patents in the related processes. In September 2021, they launched DNV-B14, a chemical vapor deposition (CVD) grown quantum-grade diamond with a uniform NV spin-center density reported as ten times higher than its previous grade.

HiQuTe Diamond

France, 2022, €7.5M

HiQuTe Diamond is a company created by Riadh Issaoui, Ovidiu Brinza, Fabien Bénédic, Alexandre Tallaire and Jocelyn Achard, who are researchers from LSPM in Paris, France (Laboratoire des sciences des procédés et des matériaux). They produce high quality diamond crystals used in quantum technologies.

LakeDiamond

Switzerland, 2015, €2M

LakeDiamond produced synthetic diamonds used to create NV centers qubits in diamonds or with quantum sensing. They use vacuum deposition with the CVD method (Chemical Vapor Deposition). The company closed in February 2020 after getting funding from an ICO in 2018 (Initial Coin Offering, using some crypto currency).

Lucigem

Australia, 2016

Lucigem manufactures fluorescent nano-diamonds that can be used in various quantum applications, particularly for medical imaging. The company is the result of work carried out at Macquarie University in Sydney.

Qzabre

Switzerland, 2018

Qzabre creates NV center-based tips and probes to be used in scanning microscopes. They also sell a NV center microscope, the QSM. The startup was created by Christian Degen from ETH Zurich.

2.6.13 Sapphire

Crystal Systems

USA

Crystal Systems manufactures sapphire that is the wafers material for some superconducting qubits.

Pristine Diamonds (2024, India) produces diamond based materials for quantum sensing.

2.6.14 Other materials

Many other relatively common materials are used in quantum technologies.

Copper is found in cryostat cold plates and with some of the various electrical connectors. It is purified at 99.99% to become free of impurities and oxygen (OFHC for oxygen-free high conductivity), in order to improve its thermal conductivity and electrical conductance.

It is also widely used in trapped ions chambers. As far as its depletion is concerned, its consumption in quantum technologies is minor.

Carbon is exploited in a variety of places, including carbon nanotubes from C12 Quantum Electronics. This carbon must be purified to keep only its isotope 12. ^{12}C is acquired as isotopically enriched methane, in bottles sourced in the USA for the order of $10,000 as of 2026, at 99.997% purity. The isotopic separation is a chemical exchange process applied to CO_2. Carbon is also used in NV centers.

Aluminum is used in some superconducting qubits as well as for part of the connector technology in cryostats. It is abundant. The spelling is aluminum in American and Canadian English and aluminium elsewhere. This document is mostly in American English.

Manganese is used in very small quantities as a dopant in some superconducting qubits and can be used with trapped ions qubits.

Silver is mainly used in powder form in some heat exchangers in dilution refrigeration systems.

Iron is a commodity used in the form of steel in the structure of quantum computers.

Rhenium and **tantalum** are used in some superconducting qubits.

Cesium is mainly used in atomic clocks, in its isotope 133. Reserves are sufficiently abundant in relation to identified needs. They are mainly located in Canada.

In addition to germanium, **gallium** and **indium** play a key role in III-V components used mainly in photonics and **neodymium** is used in lasers. This is one of the few areas of quantum technologies where there is a strong dependence on China as a source of supply. **Bismuth** and **tungsten** are also use sparely, in donor spin qubits and nucleus spin qubits.

Finally, **beryllium**, **calcium**, **zinc**, **cadmium** and **mercury** can be used in trapped ion qubits, but the most commonly used are ytterbium, barium and calcium.

Table 15 and Table 16 contain a summary of this part with a list of materials, their main usage in quantum technologies, their main countries of production, rarity, and environmental footprint.

2.6.15 Materials science

In September 2026, a 71-page review created by US scientists argued that materials science is now a primary bottleneck for scaling quantum hardware, as progress is increasingly limited by microscopic defects, surfaces, buried interfaces, contamination, and fabrication variability. It looks at superconducting qubits, solid-state vacancies, quantum photonics, and 2D materials, showing that all face a common "structure-coherence problem". They show the need to quantitatively connect a specific atomic-scale defect or interface structure to measured degradation of qubit coherence. They ask for the creation of a transversal science on how to develop an atomic-level understanding of decoherence mechanisms, finding material metrics that predict device performance, and developing characterization techniques capable of probing light elements and buried interfaces [3522]. You can have a look at the manufacturing part of this section in 2.4 as well as a specific part on superconducting qubits in 1.3.5.

Table 15: Raw materials and isotopes used in quantum computing hardware, with production concentration, high-purity processing chokepoints and environmental burden. Production shares are 2025 estimates from [3523] unless stated otherwise, and are mine or refinery output shares by mass, worldwide, with an uncertainty of a few percentage points. Production concentration, high-purity processing concentration, qualified-supplier availability and geopolitical exposure are distinct dimensions and are not aggregated into a single score here. Environmental color code: green, low burden; orange, moderate; red, high; gray, not assessed. The code is an ordinal judgment derived from the qualitative mechanism named in each cell, comparable within this table only, and it is not a per-kilogram life-cycle result. 🅭 Olivier Ezratty, September 2026.

Material	Role in quantum computing	World output and leading producers	High-purity chokepoint and substitutes	Environmental burden
^{4}He	Cryostat precooling, 4 K stages, pulse-tube and wet cryostats	≈190 Mm^3 (2025e). USA 42.6%, Qatar 33.2%, Russia 9.5%, Algeria ≈6%, China 1.6%	Byproduct of natural gas extraction.	Extraction impact allocated to natural gas.
^{3}He	Dilution refrigerator	≈40,000 L/yr worldwide, from tritium decay at Savannah River (USA), CANDU (Canada) and Rosatom (Russia).	Continuous adiabatic demagnetization refrigeration is one alternative for continuous sub-kelvin cooling; other methods exist depending on temperature, heat lift, duty cycle and application. ≈20 L per dilution unit [86].	No mining footprint.
^{28}Si	Spin qubit substrates and epilayers	Centrifuge enrichment of SiF_4. Urenco Stable Isotopes (Netherlands), Orano (France, >99.92%), Rosatom ECP Zelenogorsk (Russia), ASP Isotopes (South Africa, since 2025)	Natural silicon abundant [3524]. Cost rises with enrichment level	Isotope separation is energy intensive.
Si (metal)	Substrates, SiGe, cryo-CMOS and control ASICs, photonic ICs	China ≈85% of world silicon metal [3525]	Polysilicon, wafer and fab chain concentrated in China, Taiwan, Japan and Germany. No substitute	Carbothermic smelting, electricity-intensive, and coal-powered in China.
Nb	Superconducting films, resonators, qubits, wiring, SNSPD (NbN, NbTiN)	Brazil ≈93%, Canada ≈5%	Single-company dominance (CBMM). First US high-purity Nb oxide plant created in 2024 [3526]	Pyrochlore in carbonatite, ferroniobium smelting is energy intensive
Ta	High-coherence transmons (Ta on sapphire), capacitors, SNSPD and TES stacks	Congo, Rwanda, Brazil, Nigeria and China.	Nb substitutes with a coherence penalty. Conflict-mineral due diligence applies to the whole chain	Social rather than climatic burden due to artisanal mining and child labor.
Al (5N–6N)	Josephson junctions ($Al/AlO_x/Al$), wiring, shields, ion trap electrodes	China ≈59% of primary aluminum. Bauxite from Australia, Guinea and China	Ultra-high-purity aluminum for junction growth is a specialty product. No substitute for the Al/AlO_x junction itself.	Bauxite red mud plus coal-fired smelting.
Mo	MoSi SNSPD films [3527], MoRe resonators [3528], cryogenic fasteners and thermal links	≈260 kt (2023). China ≈110 kt, top five producers ≈93% [3529]	Chinese export licensing since February 2025.	Byproduct of porphyry copper with acid rock drainage.
W	WSi SNSPD films, X-ray and thermal shielding	China ≈83% of mined tungsten [3525]	Ammonium paratungstate intermediate chain is even more Chinese than the mine itself. MoSi substitutes	Concentrated downstream processing chemistry, moderate footprint.
Au	Wire bonds, cryostat cold plates, ion trap electrodes, mirror coatings.	China, Russia, Australia, Canada and the USA lead, none above roughly 10%	No supply risk. Substitutable by Ag or Cu in cryostat roles [3530].	Artisanal gold mining is largest anthropogenic mercury source, and refining is the dominant step [3530].

Continued on next page.

Table 15 continued from previous page.

Material	Role in quantum computing	World output and leading producers	High-purity chokepoint and substitutes	Environmental burden
Cu (OFHC)	Cold plates, thermal links, coaxial lines, magnetic shields.	Chile, Peru, Congo, China and the USA. Refining in China.	OFHC and cryogenic-grade copper is routine procurement.	Porphyry mining, tailings volume and water use.
Ti	Cryostat structure, cabling, UHV pumps	Sands from Australia, South Africa, China and Canada. Sponge metal China ≈69% [3525]	Sponge is rare. Stainless steel and aluminum substitute in most structural roles.	Kroll process is energy-intensive, and China sponge production is coal-heavy.
Ag	Heat exchangers in dilution units, RF plating, cold-finger contacts	Mexico, China, Peru, Chile and Poland	Byproduct of Pb-Zn-Cu.	Low impact. Mercury legacy in some historic places.
In	Bump bonds and flip-chip interconnect, cryogenic vacuum seals, InP and InGaAs	China 760 t (≈69%), Korea 180 t, Japan 65 t, Canada 40 t, France 21 t	Byproduct of zinc. Under Chinese export control since February 2025. No good substitute for cold-weld indium seals.	Footprint allocated to zinc smelting.
Ga	GaAs and GaN electronics, laser diodes, III-V photonics, quantum dots.	Primary low-purity ≈760 t, China 98–99%. High-purity refined ≈320 t/yr from Canada, China, Japan, Slovakia and the USA.	Export licensing since 2023. US import went from \$277/kg (2021) to \$580/kg (2025e) [3531]	Byproduct of the Bayer alumina process, small share of the bauxite and smelting burden.
Ge	Ge and SiGe spin qubits, IR optics, fiber dopant, detectors	China ≈60% of primary, ≈77% of refined [3525]	Chinese export control since 2023. Silicon substitutes in some detectors.	Byproduct of zinc concentrates and coal fly ash.
As, P	GaAs, InP, InGaAs and AlGaAs photonics and detectors.	Arsenic: China. Phosphorus: China, Morocco and USA.		Arsenic is toxic, and phosphate rock processing generates phosphogypsum at scale.
Yb	$^{171}Yb^+$ trapped-ion qubits, Yb neutral atoms, Yb fiber lasers	Heavy rare earth. China ≈69% of mine output, ≈90% of separation, ≈99% of heavy rare earth separation.	^{171}Yb isotopic purification. No substitute once ion species is chosen. Chinese heavy rare earth export controls tightened in 2025.	Bastnäsite, monazite and ionic clay routes. Thorium-bearing tailings, acid leaching and radioactive residue management.
Ba	$^{133}Ba^+$ and $^{137}Ba^+$ trapped ions, and BaB_2O_4 (BBO) nonlinear crystals	Barite from China, India, Morocco, Kazakhstan and Mexico. Barium metal and enriched isotopes are a separate chain (Russia, ORNL)	^{133}Ba is radioactive and needs licensing, so ^{138}Ba is the practical choice. Isotope separation constraint.	Barite is a low-toxicity sulfate.
Sr	$^{88}Sr^+$ trapped ions, Sr neutral atoms	Celestite. Iran ≈200 kt/yr, plus Spain, Mexico and China	Handful of specialty suppliers	Shallow sulfate ore, low impact.
Rb	^{87}Rb neutral-atom arrays, and Rb clocks and magnetometers (Table B)	Byproduct of pollucite ($(Cs,Na)_2Al_2$) and lepidolite.	Sinomine controls both commercial pollucite sources, Tanco (Canada) and Bikita (Zimbabwe).	Pegmatite mining, small footprint. Impact dominated by lithium co-production.
Cs	Cs neutral atoms, and Cs primary frequency standards.	Same pollucite chain as Rb. Sinomine is sole world supplier of cesium formate	Tanco is mined out and Bikita is subject to Zimbabwean export restrictions. Formate brine recycled at about 85%, so stock erodes each cycle.	As Rb. The risk here is commercial concentration, not environmental.
^{12}C, CVD diamond	NV centers, carbon nanotubes, heat spreaders	^{12}C-enriched methane from a few isotope suppliers. CVD diamond from Element Six (UK, USA), Orbray (Japan), and Chinese HPHT and CVD producers.	Substrate quality, nitrogen incorporation control and ^{13}C depletion set the limit, not element supply [3524].	No mining, CVD growth is slow and electricity intensive.

Continued on next page.

Table 15 continued from previous page.

Material	Role in quantum computing	World output and leading producers	High-purity chokepoint and substitutes	Environmental burden
N	NV center formation, LN_2 cryostat precooling, purge and glovebox atmospheres	From air. Unlimited.	No supply risk even in liquid form.	Air separation and liquefaction electricity.
$LiNbO_3$ (Li + Nb)	Thin-film lithium niobate modulators and photonic integrated circuits	Lithium from Australia, Chile, China and Argentina.	TFLN wafer supply is Chinese-led [3526].	Lithium brine evaporation consumes water in the Atacama, and Australian hard-rock spodumene needs calcination.
Al_2O_3 (sapphire)	Substrates for Ta and Nb transmons, cryogenic windows, Ti:sapphire gain medium	Synthetic. Production in China, Russia, USA and Japan.	Large-diameter, low-loss cryogenic-grade boules are a specialty. Silicon substitutes with higher dielectric loss.	Very high melt-growth electricity demand.

Table 16: Raw materials and isotopes used in quantum sensing, timing and communications hardware. Production shares are 2025 estimates from [3523] unless stated otherwise. Environmental color code as in Table 15. (cc) Olivier Ezratty, 2026.

Material	Role in sensing, timing, comms	World output and leading producers	High-purity chokepoint and substitutes	Environmental burden
Cs	^{133}Cs primary frequency standards, chip-scale atomic clocks, Cs vapor magnetometers	Pollucite only. Sinomine controls Tanco (Canada) and Bikita (Zimbabwe) and is the only supplier of cesium formate [3532].	Rb clocks replaces Cs in most deployed GNSS and telecom roles.	Pegmatite mining, small footprint. Risk with commercial concentration.
Rb	^{87}Rb and ^{85}Rb clocks for GNSS payloads, vapor-cell magnetometers, atom interferometry for gravimetry and inertial navigation.	Byproduct of pollucite and lepidolite.	Same Sinomine chokepoint as Cs [3532].	As Cs, impact dominated by lithium co-production from the same ore.
Sr	^{87}Sr optical lattice clocks, candidate for a redefined second.	Celestite. Iran ≈200 kt/yr, plus Spain, Mexico and China.	High-purity Sr metal and getter ampoules from a few specialty suppliers. Yb is the competing optical species.	Shallow sulfate ore.
Yb	^{171}Yb optical clocks, Yb fiber lasers and amplifiers, Yb-doped crystals	Heavy rare earth. China ≈69% of mine output, ≈90% of separation, ≈99% of heavy rare earth separation.	Sr is the competing optical clock species.	Thorium-bearing tailings, acid leaching and solvent-extraction cascades in the separation step.
^{4}He	^{4}He optically pumped magnetometers, cryogenic SQUID magnetometry, MEG and MRI cooling.	≈190 Mm^3 (2025e). USA 42.6%, Qatar 33.2%, Russia 9.5%	Alkali-vapor OPMs (Rb, Cs, K) are the substitution path and are cryogen-free, which is why SQUID-based MEG is losing ground.	Impact allocated to natural gas, but fugitive losses are irreversible.
^{3}He	^{3}He NMR gyroscopes, polarized ^{3}He neutron spin filters, hyperpolarized lung MRI, sub-Kelvin detector platforms	Tritium decay.	Competes with dilution refrigerator demand for the same molecules.	Short supply.

Continued on next page.

Table 16 continued from previous page.

Material	Role in sensing, timing, comms	World output and leading producers	High-purity chokepoint and substitutes	Environmental burden
^{14}N, ^{12}C diamond	NV center magnetometry, thermometry, electrometry, gyroscopes, and imaging.	Nitrogen from air. ^{12}C-enriched methane from a few isotope suppliers.	Diamond substrate quality, NV density control and ^{13}C depletion are the real limits, not element supply [3524]	CVD growth is slow and electricity intensive.
Er	Er-doped fiber amplifiers, Er:Y_2SiO_5 telecom-band memories, quantum repeaters, C-band single-photon sources	Heavy rare earth, same Chinese separation chokepoint. Named as a NATO-relevant dependency [3533]	The 1550 nm transition is what makes Er unique, so there is no functional substitute for telecom-band operation	Rare earth separation chemistry, thorium-bearing tailings
Eu	Eu:Y_2SiO_5 and Eu:Y_2O_3 long-lived optical and spin memories, hours-scale coherence demonstrations	Light-to-mid rare earth. The same Chinese separation dominance applies	Pr and Tm are alternative memory ions with shorter coherence. Host crystal growth quality dominates performance	As Er, identical processing route
Pr, Tm	Pr:YSO and Tm:YAG memories, Tm-doped fiber lasers for cold atoms and 2 µm sources	Rare earths, same chain. The original table rated thulium as less concentrated than the other rare earths, which is not correct	Interchangeable with Eu and Er at a coherence and wavelength cost	Identical processing route to the other rare earths, so identical tailings profile
Nd	Nd:YAG and Nd:YVO_4 pump and trapping lasers, frequency-doubled 532 nm sources	Light rare earth, the largest rare earth market by volume through NdFeB magnets. China ≈69% mined, ≈90% separated	Yb-doped fiber lasers are displacing Nd:YAG in many roles, a genuine substitution path that also removes a supply dependency	Bayan Obo tailings. Quantum is a price-taker here, magnet demand sets the market
Y	YAG, Y_2SiO_5 and YIG host crystals, garnet substrates for magnonics	Rare earth, Chinese separation dominance. Also a US Defense Logistics Agency stockpile item until it was dropped in 2023 [3531]	Host crystal growth, not yttrium supply, is the constraint	As the other rare earths
Nb (NbN, NbTiN)	SNSPD films for QKD receivers, LiDAR, deep-space optical links	Brazil ≈93%, Canada ≈5%. High-RRR refining is a much narrower chain	MoSi and WSi substitute with different jitter and efficiency tradeoffs [3527]	Carbonatite mining, moderate tailings, energy-intensive ferroniobium step
Mo, W	MoSi and WSi amorphous SNSPD films, TES absorbers	Mo: top five ≈93%, China ≈110 kt of ≈260 kt [3529]. W: China ≈83% mined [3525]	Mutually substitutable with NbN and NbTiN, but each swap forces a system redesign [3528]	Porphyry copper byproduct for Mo, concentrated APT chemistry for W
Ga, In, As, P	SPAD and APD detectors, InGaAs photodiodes, laser diodes, InP photonic integrated circuits	Ga: China 98–99% of primary, refined ≈320 t/yr. In: China ≈69% of 1,100 t refinery output	Both under Chinese export control. Compound semiconductor wafer supply, and SPAD qualification, are the narrow steps [3531]	Ga and In are byproducts with modest allocated impact, but arsenic is acutely toxic across the whole handling chain and dominates the row
Ge	Ge and SiGe detectors, IR optics, fiber core dopant	China ≈60% primary, ≈77% refined [3525]	Under export control since 2023. Silicon substitutes below 1100 nm only	Byproduct of zinc concentrates and coal fly ash
$LiNbO_3$, TFLN	High-speed modulators and phase shifters for QKD and photonic links, PPLN for frequency conversion	Lithium from Australia, Chile, China and Argentina. Niobium from Brazil. TFLN wafer supply is narrow and Chinese-led	Named as a NATO-relevant exotic material for both computing and sensing [3533]. Thin-film barium titanate and silicon-organic hybrids are emerging alternatives	Atacama brine water consumption, Australian hard-rock spodumene calcination

Continued on next page.

Table 16 continued from previous page.

Material	Role in sensing, timing, comms	World output and leading producers	High-purity chokepoint and substitutes	Environmental burden
TeO_2	Acousto-optic deflectors and modulators for qubit addressing, beam steering and pulse shaping	High-quality TeO_2 single crystal is produced mainly in Ukraine, with China holding ≈77% of refined tellurium [3525, 3531]	The clearest non-China single-point dependency in either table, and it sits in an active war zone. Quartz and KTP deflectors substitute with a worse acousto-optic figure of merit	Tellurium is a copper-refining byproduct at very small volumes, so allocated impact is low
BBO, KTP, LBO, PPLN	Nonlinear crystals for SPDC photon-pair sources, second-harmonic generation, squeezed-light generation	Ba, K, Li and Nb feedstocks are not constrained. Crystal growth is concentrated in China (CASTECH, CRYLINK) and a few Western houses	Growth expertise and coating quality, not element supply, set the limit	Melt and flux growth over long cycles, electricity intensive
Ti, Al_2O_3	Ti:sapphire lasers for cold atoms and NV excitation, sapphire windows and vacuum viewports	Sponge titanium China ≈69% [3525]. Synthetic sapphire growth in China, Russia, the USA and Japan	Ti:sapphire is being displaced by diode and fiber lasers, a real substitution path that also removes a supply dependency	Kroll process for titanium plus long melt-growth cycles for sapphire, both coal-heavy where they are concentrated
Si, ^{28}Si	Silicon photonics, SiN waveguides, Si SPADs, MEMS for vapor cells	China ≈85% of silicon metal [3525]. ^{28}Si from four enrichment suppliers	Foundry access, not silicon supply, is the constraint for photonic integrated circuits	Carbothermic smelting electricity, predominantly coal-powered
Au, Ag	Vapor cell coatings and electrodes, mirrors, plasmonic structures, RF plating	Diversified for gold. Silver from Mexico, China, Peru, Chile and Poland	Fully substitutable in most of these roles, unlike in the cryostat	Artisanal gold mining mercury emissions dominate, even at the small masses used here

2.6.16 Bibliography and notes

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This **Raw materials** subsection contains 35 bibliographical references and notes containing at least 534 pages.

2.7 Quantum enabling technologies key takeaways

- Quantum enabling technologies cover a broad field with cryogenics and vacuum pumps, control electronics, photonics including lasers, photon sources and detectors, photonic integrated circuits, semiconductor manufacturing techniques and even specific materials production. They are strategic to enabling future quantum systems, particularly scalable quantum computers. From a business standpoint, they are the equivalent of shovels in the gold rush. Many of these technologies have use cases beyond quantum technologies.

- Cryogenics is a key enabling technology for quantum computing, particularly for solid-state qubits operating at temperatures between roughly 15 mK and 1 K. Dilution refrigerators use mixtures of ^{3}He and ^{4}He to reach the lowest temperatures. Other cryogenic technologies target approximately 3 K to 10 K and can be used for some photonic sources and detectors. Large photonic quantum-computing projects may also require substantial cooling in the 2 K to 4 K range for sources, circuits, detectors and control electronics. A new trend for large-scale cryogenic systems for superconducting qubits is the use of helium centralized liquefiers (LHe).

- Cabling and filters play another key role, particularly with solid-state qubits. Cryogenic and superconducting cables can be expensive, with prices and supplier availability depending strongly on cable type, attenuation, thermal load, bandwidth and connector specifications. Signal multiplexing may reduce cabling requirements, including microwave multiplexing and microwave-to-optical conversion approaches.

- Microwave generation and readout systems used with superconducting and quantum-dot electron-spin qubits are other key enabling technologies. The challenge is to miniaturize them, lower their power consumption and, where useful, place some control electronics closer to the qubits at cryogenic temperatures while simplifying system cabling. This is important for physical-qubit scalability and quantum error correction. Many different technologies compete here, mostly around cryo-CMOS and SFQ superconducting electronics. Other components deserve attention, including circulators and parametric amplifiers that we cover in detail. Lastly, error correction requires extensive classical processing that is frequently omitted from fault-tolerant quantum-computing resource estimates.

- Many lasers and photonic components are used with cold atoms, trapped ions and photonic qubits, as well as in quantum telecommunications, cryptography and sensing. These include indistinguishable single-photon sources, single-photon detectors and photon-number-resolving detectors. The laser field is also very diverse, with products covering different wavelength ranges, powers and continuous-wave or pulsed operation. Cold-atom technologies can require relatively high optical power with low phase noise. Laser reliability is also a concern for production use. Cold-atom systems additionally rely on light-shaping devices such as SLMs, AODs, optical arrays and metasurfaces designed to control large numbers of atoms.

- Manufacturing electronic components for quantum technologies is a strategic topic covered extensively in this book with a description of generic fab techniques and some that are specific to quantum technologies as with the fabrication of superconducting qubits and quantum dots.

- Quantum technologies use many different raw materials, some of them rare but required only in small quantities. Some materials may carry significant environmental or supply-chain costs, while others are available from multiple sources. Examples include ^{3}He for sub-1 K cryogenics, isotopically enriched ^{28}Si for silicon-based quantum technologies, and atomic isotopes such as ^{87}Rb and ^{171}Yb. A key challenge is to analyze full product life-cycle costs and reduce the environmental footprint of emerging quantum technologies, particularly for components that may eventually be manufactured at scale.

3 Unconventional computing

This part consolidates a set of technologies and companies that propose to significantly increase the power of computing machines without relying on quantum technologies. Quantum computing belongs to the broad unconventional computing field like digital annealing, reversible and adiabatic classical computing, superconducting computing, analog computing, neuromorphic computing, spiking neural networks, probabilistic computing, photonics computing, chemical and DNA computing. The category is quite broad since it also includes nanomagnets (energy efficient, non-volatile, used with neural networks), spintronics and memristive devices (for neural networks and spiking neurons), magnetic excitations (spin wave, skyrmions), in-memory digital or analog processing [3534–3536], dynamical systems (Ising machines) and brain inspired computing [3537, 3538].

Some of these avenues have been explored by major players such as IBM for superconducting computing or by startups and with ups and downs. Some, such as MemComputing and InfinityQ, go so far as to tout exponential computing accelerations versus traditional architectures while being based on classical CMOS components and to the point of asserting a capability to solve NP-complete problems in polynomial time, including large integer factorization.

Unconventional computing paradigms differ in one way or another from Turing-machine-based computation and from the von Neumann architecture based on control units, computing, registers and memory that are the basis of today's classical computers. A bit like quantum computing, their benefit compared to classical computing could be about bringing some speedup but not only. It can also deal with system energetic footprint or with the ability to solve specific types of problems.

It is particularly true with **natural computing** solutions that use physical elements from nature or are inspired by nature as shown in Figure 468. This includes computers based on biological components like DNA, probabilistic computers, chemical computers, membrane computers, as well as spintronics and neuromorphic processors that are adapted to artificial intelligence processing [3539, 3540]. I will not cover them all since they are not necessarily relevant to bring some computing speedup vs classical computing.

For many of the domains in unconventional computing, you will find a couple startups and even large established companies trying to create viable products, based on various levels of fundamental research TRL (technology readiness level). But, after nearly 60 consecutive years of CMOS-based Moore's law expanding the scope of classical computing, none of these paths really got traction.

What are they missing? It depends. First, it may not work at all. Then, it may operate at small scale but not beyond, when it could exceed the performances of classical computers. Then, it may cover very narrow use cases, making it difficult to find a market. Also, it may have a hard time competing with the progress of classical computing both in the hardware and software realms.

It can also be economical, with not enough funding fueling the domain. At last, these technologies have a very small ecosystem of scientists, vendors and users. Only a few are fact-checking each other. It makes it hard to assess the viability of all these diverse technology paths.

General-purpose analog computing is a good example of a path that lost ground, with most of its work done between the 1950s and the 1970s. It was progressively abandoned in favor of programmable digital systems, not because the latter are free of noise, which they are not, but because they offer better reproducibility, precision, programmability and scaling. It could be revived thanks to bringing some energetic advantage [3542]. In some respects, quantum computing is a return of the analog computing paradigms.

This energetic advantage is a preeminent argument in favor of all these unconventional computing paths. They are also frequently positioned as alternative solutions to classical computing implementations of neural networks like the recent large language models (LLMs) such as ChatGPT.

Research in unconventional computing may have interesting side effects. For example, superconducting classical computing and electronics could be useful to allow quantum computers to "scale" with reducing the load of control electronics and enabling it to work at low temperature. We can therefore also evaluate these different technologies from the point of view of their complementarity, rather than competition, with quantum computing.

3.1 Supercomputing and HPCs

The so-called "quantum supremacy" announced by Google in October 2019 systematically referred to power comparisons with supercomputers, in particular with the **IBM Summit** installed at the Oak Ridge laboratory of the US Department of Energy since 2018. We'll see in a later part that this comparison was non-sense and was mixing apples and oranges in an unfair way towards

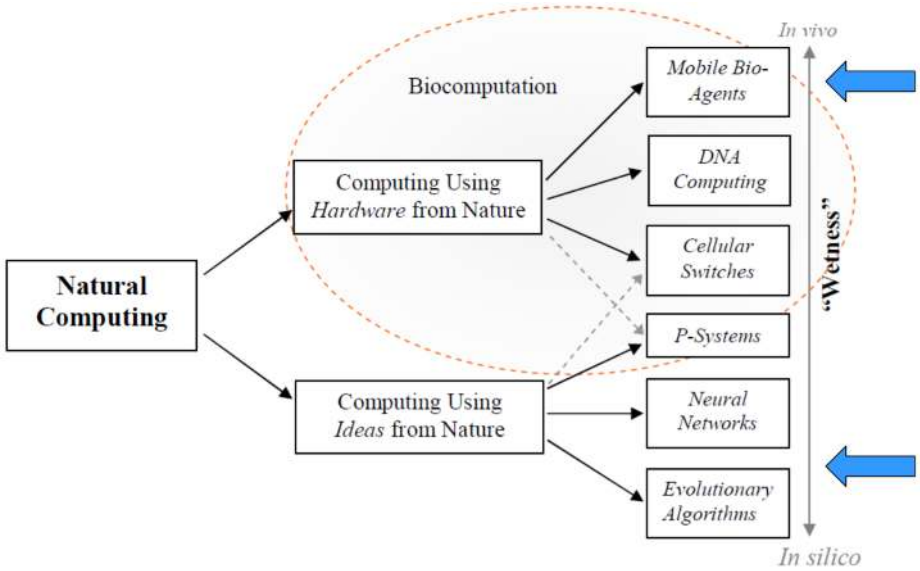


Figure 468: How biomimetics is used in computing. Source: [3541].

the IBM Summit and HPC overall. Classical simulation of Sycamore's random circuit sampling has been revisited many times since, and its cost depends entirely on the circuit family, the depth, the targeted linear cross-entropy fidelity and the algorithm used. Tensor-network contraction methods reaching a fidelity of about 0.002 of the 53-qubit, 20-cycle experiment have been tested on GPU clusters.

This kind of supercomputer falls within the field of "High Performance Computing" (HPC), which we will study briefly here to put it into perspective in relation to quantum computing.

3.1.1 Definitions

The notion of HPC has not always been well defined, particularly since it is a moving target. The power of a supercomputer from the 1980s is now available in a simple recent server if not in your smartphone. However, it is possible to describe the category with its application requirements. HPC and supercomputers are essentially used for digital simulation and the analysis of complex data. These tools are provided to both researchers, public services and industry for their most advanced computational needs [3543].

HPCs are used for weather forecasting [3544], organic and inorganic chemistry simulations, aerospace and automotive simulation, nuclear weapon simulation, in financial services, in machine and deep learning and, we tend to forget, also to create advanced computer graphics in movie and TV series productions. The mathematical models used in supercomputers are used in particular to solve partial differential equations and to carry out N-body simulations.

These systems are demanding in several ways: in computing capacity, often evaluated in floating-point operations per second, if possible, in double precision (FLOPS), in data storage capacity, and above all, in the ability to transfer data rapidly between storage, memory and processing units. It is in these areas that supercomputers are most distinct from commodity servers used in data centers.

These systems however do not belong to the "unconventional computing" domain since they are based on relatively classical computing systems: CPU, GPU, memory and storage.

3.1.2 History

When the mainframe computers era started in the 1960s, you had general purpose solutions coming for example from IBM with its famous family of 360 systems with a range of power of 1 to 25 depending on the configuration. Then, you had specialized vendors like Control Data who targeted the scientific market with more specialized systems.

The **Cray** 1, launched in 1976, is a landmark rather than the starting point of supercomputing, which was already well underway with the CDC 6600 in 1964, itself designed by Seymour Cray, and with systems such as the ILLIAC IV. Seymour Cray had participated in the creation of one of the first startups in computing, ERA, and later cofounded Control Data. Cray supercomputers relied on home-grown vector processors and various proprietary massively parallel systems. Cray was acquired by HPE in 2019.

These proprietary systems were progressively displaced in the early 2000s by cluster-based architectures using standard CPUs, later complemented by general-purpose GPUs like those from Nvidia. GPU acceleration entered the TOP500 around 2008 with the first CUDA-based clusters and became mainstream after 2012, the 2017

Volta generation marking its acceleration in AI-oriented systems rather than its beginning.

A cluster contains several nodes, each containing several CPUs and/or GPGPUs, themselves multi-core, and fast interconnection between these nodes, between clusters, and fast access to data storage, increasingly based on SSDs, which are much faster than hard disks, and at last fast networking access.

According to Precedence Research, the current size of the HPC market was estimated at around $59.85B in 2025, to nearly double by 2033 (Figure 469). Quantum computing market sizes can be compared to this gauge when accounting for the potential with scientific applications and considering the funding of the organizations hosting these HPCs.

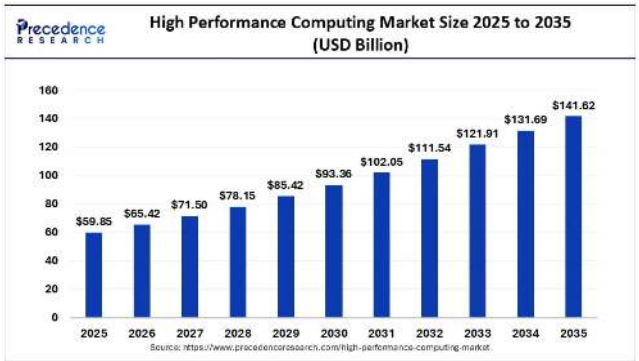


Figure 469: HPC market size forecast by Precedence Market in 2026. In 2022, they forecasted a market of $50.78B in 2025, below the estimated actual of $59.85B in 2026. Source: [3545].

3.1.3 HPC architecture

Clusters based on standard microprocessors now account for over 90% of the 500 largest supercomputers in the world [3546]. The Top 500 is based on a standardized benchmark, the HPL for High Performance Linpack. It is used to solve a set of linear equations using Gaussian elimination using dense matrices and double-precision floating-point computation. The list ranks systems by Rmax, the best measured HPL performance, which is distinct from Rpeak, the theoretical peak, and from the HPCG and HPL-MxP benchmarks published alongside it.

The CPUs most often come from Intel (Xeon), AMD (Opteron and then EPYC), IBM (Power9, who withdrew from that market) while Nvidia dominates the accelerator market with its general-purpose GPUs, including the famous V100 generation Volta launched in 2017 and its successors A100 Ampere announced in May 2020, the H100 Hopper in March 2022 with 80 billion transistors and a data transfer speed of 3 TB/s with its associated HBM3 RAM and the Blackwell launched in 2024. 40% of the top 500 HPC were equipped with Nvidia GPGPUs as of June 2025 while AMD is providing the CPU for 34% of them, including 19% with both a CPU and GPU Figure 470. This trend accelerated as the OpenMP and OpenACC frameworks were ported to Nvidia GPUs, making these easier to use for a host of existing scientific applications.

This is a form of commoditization of supercomputing, even if these are still heavyweight systems installed in large machine rooms and data centers rather than in cleanrooms. The technology added value shifted to interconnection, memory and storage architecture as well as, of course, software.

Interconnection in cluster nodes uses technologies such as Nvidia's NVLink, which connects GPUs and CPUs at high speed. Cluster nodes are interconnected by multiple 200 Gbit/s fiber optic links such as InfiniBand, often from **Mellanox**, Nvidia's subsidiary since 2019, or more regular Ethernet. On a larger scale, HPE is promoting the **Gen-Z** architecture optimized for data access in distributed "data-centric" systems.

Operations on supercomputers are programmed with different development tools and middleware, the parallel application development library for Fortran, C and C++ MPI is very commonly used for scientific computing, as well as **OpenMP** directive-based standard. On top of this, applications for numerical simulation can be developed in-house, open-source such as **OpenFOAM**, an open-source SDK used to simulate fluid mechanics, chemical reactions, heat transfer, solid mechanics, electromagnetism and in finance, or commercial from ISVs (Independent Software vendors) such as **LS-DYNA** for structural simulation. Supercomputers are also increasingly used for AI workloads, or hybrid HPC-AI workflows. Let's not forget also that there are many optimization algorithms based on practically acceptable approximations, such as for traveling salesperson type problems.

Vendors from Japan and China are creating their own custom supercomputers microprocessors, to limit their dependence on USA companies.

In Japan, the **Fujitsu** Fugaku supercomputer uses Fujitsu A64FX chips comprising 52 Arm cores and 32GB of HBM2 memory delivering a nominal power rating of 2.7 TFLOPS (processor layout *below*). The Fugaku, which is not a poisonous fish but is another name for Mount Fuji, has a total of 415 double precision PFLOPS with 396 racks and 152,064 processors (Figure 471).

Its installation was completed in June 2020 and enabled Fujitsu to win first place on the podium of the world's most powerful supercomputers ahead of the USA with the IBM Summit [3548–3551].

As of the June 2026 TOP500 list, China's largest declared supercomputer is the **LineShine** installed at the National Supercomputing Center in Shenzhen. Its HPL performance is 2.2 EFLOPS Rmax and it uses 45,360 home-built LineShine LX2 64-bit RISC processors with 304 cores each. It is the most power hungry system on that list with 42 MW of measured power, a figure that should not be confused with Rpeak, with the HPL-MxP

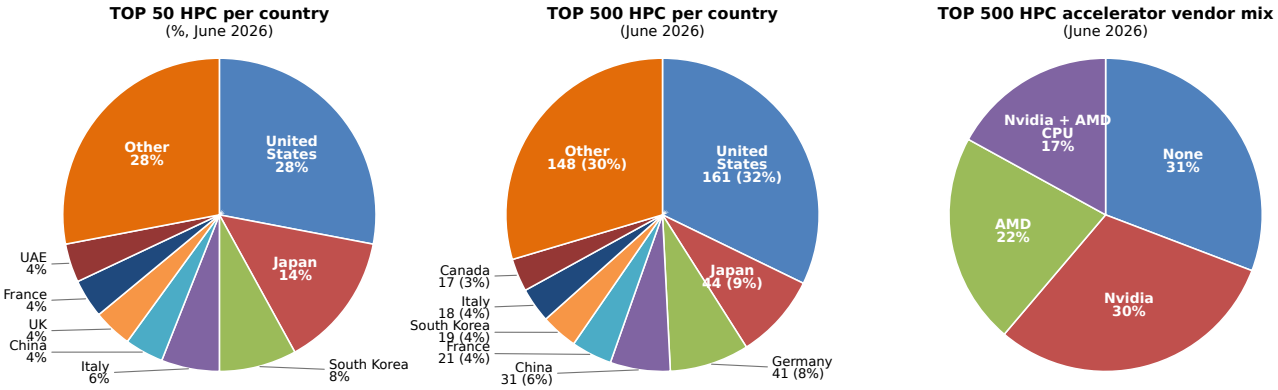


Figure 470: The TOP 50 and 500 HPC in number of systems per country, and the share of Nvidia and AMD GPUs in the top 500 HPC in percentage of systems, all in June 2026. It shows the dominance of Nvidia but also the growth of AMD as a CPU and GPU provider. Source: [3547]. Updated in September 2026.

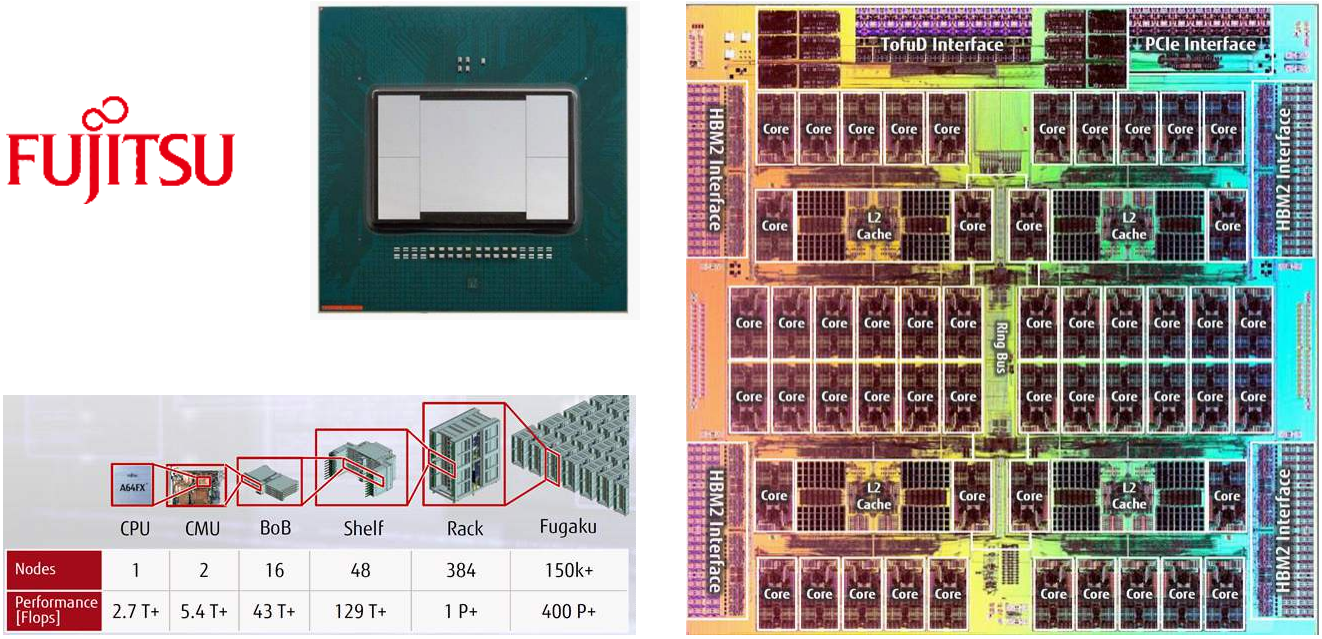


Figure 471: Fujitsu's Fugaku supercomputer is one of the largest in the world. It uses Fujitsu A64FX chips containing each 52 Arm cores and 32GB of HBM2 memory. Source: Fujitsu.

mixed-precision result or with HPCG, which measure different things. On the same list, China accounted for 6% of the systems and the USA for 28% (Figure 470).

The second largest supercomputer is El Capitan, an HPE system installed at LLNL in the USA, with 1.8 EFLOPS Rmax and a peak power of 29.7 MW.

In 2018, the European Union launched the **EPI** (European Processor Initiative), a project aiming to bring technology independence with supercomputers multicore microprocessors. It mainly involves German, Spanish, and French players, notably **Eviden, CEA and SiPearl**. The productization and commercialisation effort of the arm track of EPI is carried out by the startup **SiPearl**, led by Philippe Notton. It is part of the **EuroHPC** programme to create supercomputers encompassing processors designed in Europe. EuroHPC's first two exascale systems planned in Germany and in France, will use SiPearl technology. EuroHPC R&I projects such as EPI are co-funded evenly between the European Union and EuroHPC participating states.

In France, GENCI invests in a coordinated way in supercomputers for public research, on behalf of the Ministry of Research, together with CNRS, CEA, as well as France Universités and INRIA. GENCI's main systems are deployed and operated in three national supercomputing centres, resp. at CNRS/IDRIS, CINES and CEA/TGCC. Use case for these systems are scientific simulation and machine learning. IDRIS is more specifically specialising in HPC-fuelled AI, and TGCC on quantum computing.

The GENCI **Jean Zay** supercomputer is deployed at CNRS/IDRISS. It is equipped with 3,642 Nvidia V100 GPUs and over 3,462 Intel Xeon Cascade Lake CPUs (Figure 472). It is cooled by "hot water", from 30°C to 42°C. Its GPU AI-oriented extension was deployed in

2021 as part of the French AI plan announced in 2018 with 52 8-GPU nodes.

In June 2024, Pasqal shipped a 100 qubit Orion QPU to CEA-TGCC, acquired EuroHPC and operated by GENCI within the HQI France 2030 plan and co-funding. It was opened to users in April 2025, integrated into TGCC HPC environment. Many other European HPC centers have similar plans and deployments, in Germany, Italy and the Netherlands, among others.

Figure 472: The Jean Zay supercomputer in France is typical of the new generation of HPCs launched since 2018 with a mix of CPUs and GPGPUs from Nvidia. This mid-size supercomputer is built by HPE. It hosts 3,642 CPUs from Intel, 2,696 Nvidia V100 GPU, 1.3 PB of storage, had a peak power of 28 PFLOPS in 2020. It was cooled with hot water (32°C-42°C). Source: GENCI.

3.1.4 HPC in the cloud

Since the advent of "the cloud", HPC and supercomputing resources are now available on demand. Cloud data centers do not necessarily provide HPC resources. This depends on the servers and clusters deployed architectures and on the packaging of the cloud vendor's offering. This notion can be associated with the notion of hyperscale, which covers the capacity of a cloud infrastructure to adapt to the increasing customer computing needs.

Machine learning and deep learning applications are the most recent applications implemented on supercomputers, particularly since they are using GPGPUs that run tensors enabling efficient matrix operations, which are very common in neural networks. In practice, however, most supercomputers continue to run scientific simulation applications.

The market for microprocessors dedicated to machine learning and deep learning acceleration has been booming for several years. A wide variety of approaches have been adopted by its vendors. It can be represented as in Figure 473 on two axis: in the Y axis, the level of cores specialization, and on the X axis, the number of cores.

Google's TPUs (Tensor Processing Units) are highly specialized for training neural networks, especially convolutional image recognition networks. Nvidia's GPUs contain thousands of classical arithmetic calculation cores as well as hundreds of tensors for matrix computing, which optimizes their versatility.

The most extreme processor is the **Cerebras WSE** initially launched in 2021 with 850,000 cores. It is a 21 cm square chip containing a hefty 2.6 trillion 7 nm transistors and 40 GB of integrated SRAM ultra-fast cache memory. Their first version launched in 2019 is deployed in two test servers at the DoE in the USA with one and two of these chips. The first benchmarks published late 2019 did show excellent performance in neural networks training. In 2022, TotalEnergies found 100× speedups vs conventional GPGPU with various material simulations applications [3552]. The WSE-3 followed in 2024 with 900,000 cores, 4 trillion transistors on a 5 nm node and 44 GB of on-chip SRAM and the WSE-4 in August 2026, with a doubling of its clock speed to 2.8 GHz.

Finally, **FPGA**s are dynamically programmable circuits that allow the creation of custom circuits at rather low cost and high flexibility. The FPGA market is currently dominated by two vendors: Intel, after its acquisition of Altera in 2015, and AMD, after its acquisition of Xilinx in 2020. In 2019, Xilinx had a 52% revenue market share and Intel about 35%.

FPGAs are used by some cloud vendors such as Microsoft (with its Brainwave chips) and Chinese cloud companies like **Alibaba** and **Baidu**. The FPGA field is also lively with two trends, one is the integration of DSA (domain specific architecture) modules like arm cores, GPU cores, NPU cores and the like next to programmable arrays. The other is the CGRA (Coarse Grain Reconfigurable Array) which is about using higher level of abstraction modules than implementing just typical lookup tables logic [3553].

Some of these cloud players are developing their own supercomputers. **Google** has created its TPU pods over several generations for its data centers. A TPU v3 board contains four TPU chips, each with two cores, with 16 GB of HBM memory for each TPU core. A TPU v3 Pod has up to 2048 TPU cores and 32 TB of memory. In May 2024, Google announced its 6th generation TPU called Trillium with a 4.7x improvement in compute performance.

Graphcore (2016, UK, $692M) is another contender in this crowded market. It was acquired by SoftBank in July 2024 and is no longer an independent player. It is now using 3D chips bonding using a TSMC technology, the main chip containing processing units and the secondary underneath chip containing connectivity between the computing chips cores. Its current processors have 1,472 cores and 900MB on-chip SDRAM memory, which helps them outperform Nvidia chips on some tasks [3554].

Nvidia integrates its A100 GPUs in SuperPods totaling 140 DGX A100 and 1120 A100 servers and 4 Po of storage, for 700 PFLOPS (and now, more recent GPGPUs). These FLOPS are, however, not necessarily the same as those used to evaluate the TOP 500 supercomputers. Vendor communication is sometimes misleading.

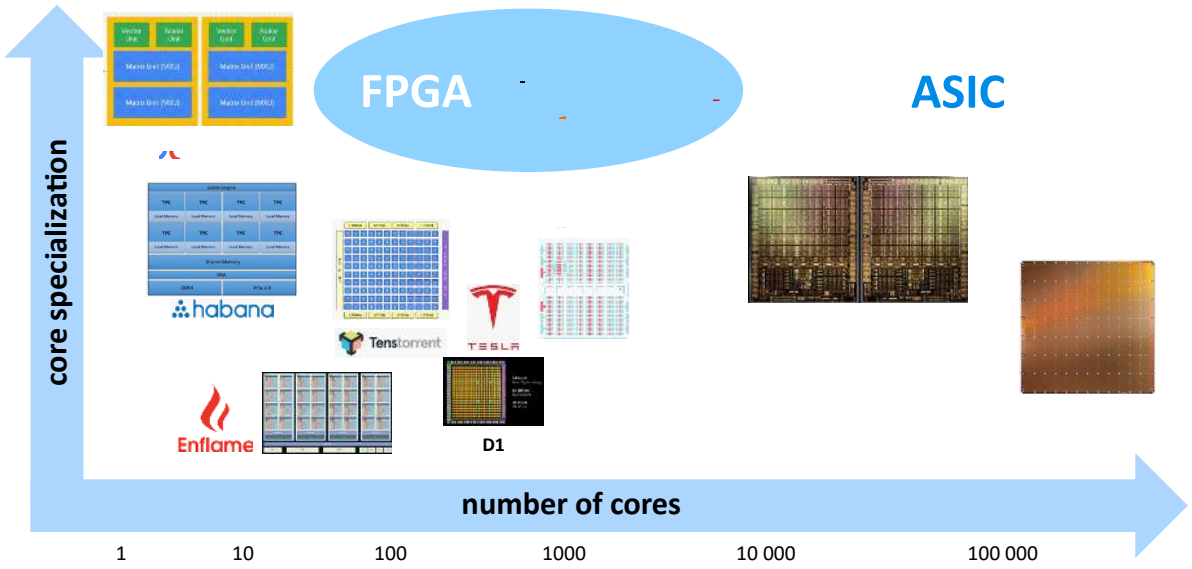


Figure 473: Map of the tensor-based processors with two dimensions: the number of cores and their specialization. The more specialized cores are in Google's TPU with large tensor operations capacity (128×128 values) while Cerebras' wafer scale chip has 850,000 relatively simple cores. Olivier Ezratty, 2022-2023.

Both to improve performance and to reduce energy consumption, there are a number of ways to make these calculations more efficient:

- **Approximate Computing**, which reduces precision in neural network training and/or inferences without affecting the results.
- **Quantization**, which switches from floating-point calculations to integer computing during or after training.
- **Binary Neuron Networks**, which is even simpler with 1 bit output neurons taking us back to the Perceptrons era of 1957.
- **Sparse Computing**, which allows computations to occur on compressed representation of matrices, this being useful only for sparse matrices, without prior decompression.

Quantum Silicon Inc

Canada, 2011, $80K

Quantum Silicon Inc is developing spin qubit chips using the donor spin variety. It is supposed to operate at room temperature. It seems not to be quantum computing per se, with qubits, but nano-classical computing using single-atom silicon quantum dots.

It is non quantum atomic scale computing. The surface of a pure silicon substrate is hydrogenated and the dots correspond to silicon where the bounded hydrogen atom has been removed with atomic probe microscopes. It used the process of hydrogen lithography, also prototyped at IBM. The careful arrangement of atoms and holes enables the implementation of classical Boolean gates like the OR two-bit gate. Two key benefits could come from this: faster operations and 100x less energy consumption. QSi was created by Ken Gordon (CEO), Robert A. Wolkow (CTO), James Chepyha (CFO). Given the company's creation date and funding, it seems that the technology may be hard to turn into a real product. They may, however, pivot in the sensing market.

Whatever happens with quantum computers, supercomputers will always be relevant. Applications using large amounts of data are not suitable for quantum computing, even with zillions of qubits. Indeed, data loading time in qubits is a huge bottleneck because it relies on very long series of quantum gates that are not as fast as classical data processing. Applications adapted to quantum computing should not rely on high-volume data feeds. This is the case with weather forecasts which require heavy data sets.

3.1.5 Power efficiency

A word of caution: FLOPS/W, TOPS/W, application speedups and annealing performance are only comparable when the numeric precision, the benchmark and instance distribution, the time to solution, the solution quality, the power boundary (chip only, or chip plus host, network, memory and cooling) and the baseline implementation are documented and comparable. Most vendor and press figures in this field state none of these.

Supercomputers are quite power hungry. Their increasingly powerful microprocessors consume several hundreds of Watts. There are still data centers where a third of the electrical energy consumed by a data center is spent on cooling, but many HPC centers are now doing better. Specialized server racks now easily consume

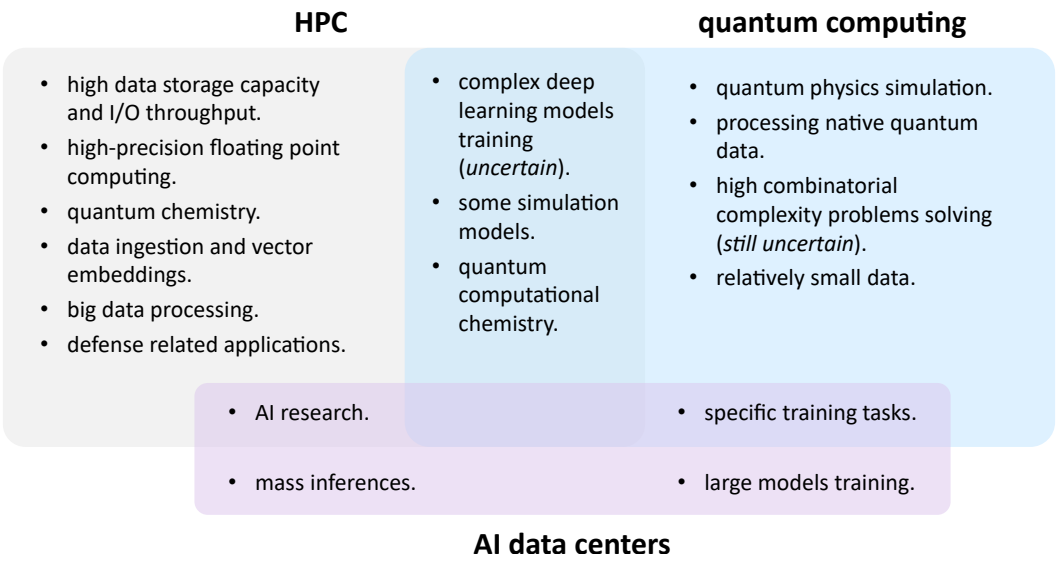


Figure 474: How to position HPCs vs (scalable) quantum computers and AI datacenters. HPCs are for big data and high-precision computing. Quantum computing will be adapted to high complexity problems but with relatively reasonable amounts of data. There's some cross-over between both systems and they will work in sync in many cases. Olivier Ezratty, 2021-September 2026.

up to 30kW. It has now reached the point where liquid cooling is preferred for removing heat from components, usually with water. This provides greater efficiency.

The table in Figure 475 describes the power consumption gap between computing and memory access, which are becoming increasingly expensive, the further away memory is from computing.

The ratio goes up to more than 1 to 1,000! It explains the attempts to bring memory closer to computing units like what **UpMem** (France) does with its DRAM memory modules integrating dozens of RISC-V cores to perform in-memory computing and speed-up certain processes by a factor of 10, particularly for big data applications.

HPC power efficiency comes from progress in CPU/GPU designs and architecture. It also depends on software tools and libraries efficiencies which have significantly contributed to the improvement of HPCs energy efficiency [3555] (Figure 476). However, most organizations running the largest supercomputers have created a sort of top limit on the power drain of their systems, around 20 MW. This is one of their motivations to be interested in quantum computers since they may potentially bring some energetic advantage on top of some computing advantage.

3.1.6 Quantum computing in HPC centers

Even if and when scalable quantum computers become available, with exponential gains in computing power, classical HPCs will still be needed, as shown in Figure 474.

The main reasons are that quantum computers, even in the FTQC regime, are not meant to boot operating systems and will not be able to handle big data efficiently. They will always rely on HPCs to process and prepare complex data in order to feed quantum computers with simpler data, compile/transpile circuits, if not support error-correction greedy processing. Quantum computing is made for solving high-complexity problems with relatively small data while HPCs may be limited in the size of addressable problems but have much better capabilities. You understand this with the bandwidth of typical classical systems shown in Figure 477.

As a comparison, you can only feed a quantum computer very slowly. Let's say you can use 4,000 logical qubits. You will be able to feed one bit for each qubit at each gate cycle. Current circuit repetition rates are 2 to 10 kHz with IBM systems, without the burden of quantum error correction. Individual two-qubit gates are much faster, in the 20 ns to 500 ns range, but the usable injection rate is set by the full prepare, run, measure and reset cycle rather than by the gate duration. It is even much slower with trapped ion systems.

You end up being able to feed roughly a couple of megabytes per second in such a quantum computer! Some architecture ingeniosity will be required to accelerate this pace, including using quantum memories and fastening the QPU cycle rate (measured in CLOPS).

3.2 Digital annealing computing

Digital annealing runs simulated annealing. It classically minimizes the same Ising and QUBO cost functions with a Metropolis-type simulated annealing process, differing from plain simulated annealing by a parallel-trial scheme and a dynamic escape mechanism, and using custom chips to parallelize the trial moves [3558].

Function	Energy in Picojoules	
8-bit add	0.03	computing
32-bit add	0.1	
FP Multiply 16-bit	1.1	
FP Multiply 32-bit	3.7	
Register file access*	6	cache and memory access
Control (per instruction, superscalar)	20-40	
L1 cache access	10	
L2 cache access	20	
L3 cache access	100	
Off-chip DRAM access	1,300-2,600	

Figure 475: In classical computing, the biggest energy cost comes with moving the data and not computing. It may be the same with quantum computing, if not worse given data loading in a QPU will be quite slow and energy consuming. Source: [3556].

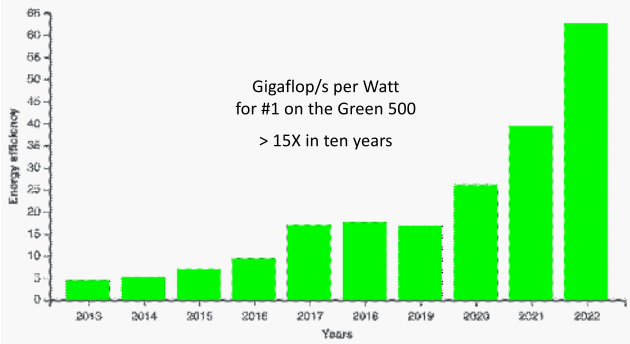


Figure 476: HPC energy efficiency progress over time. Source: [3557]. Added in 2023.

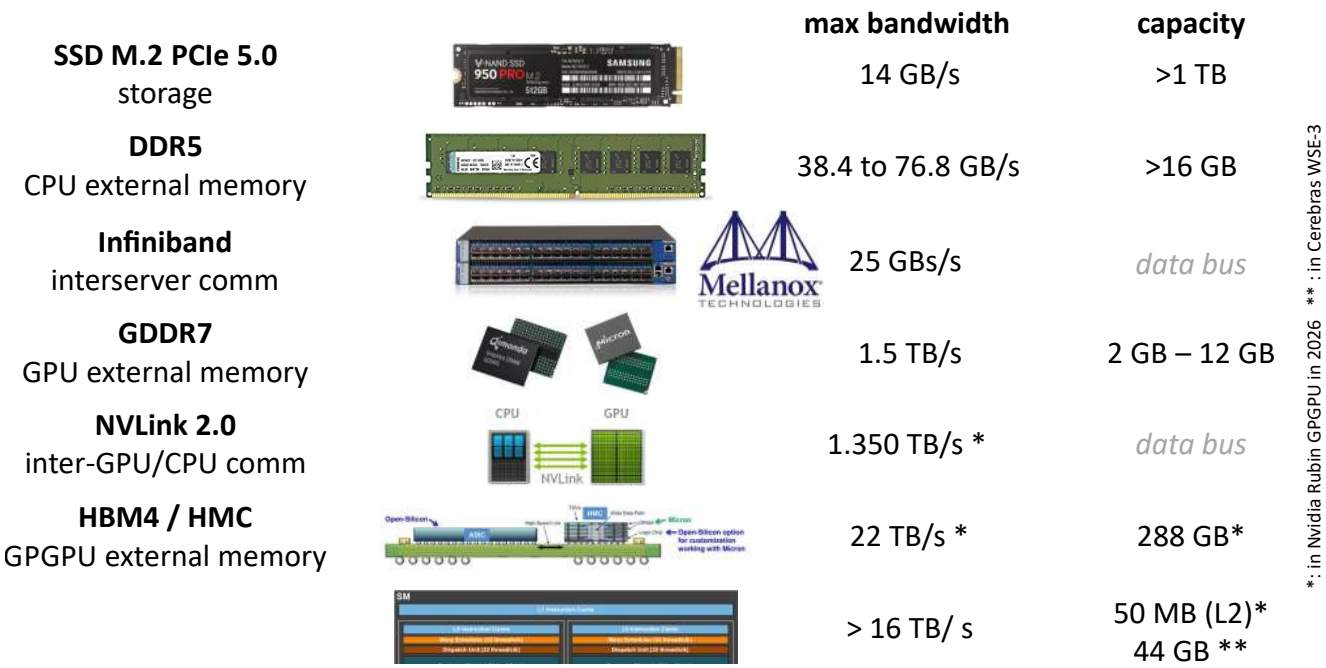


Figure 477: Data bandwidth and capacity of typical systems memory, storage and interconnect. The larger the capacity, the slower data read and write can be, and the other way around. Notice the speed in GB/s for input/output with memory close to the processor. It is useful when making comparisons with how data can be loaded in a quantum computer. ⓒ Olivier Ezratty, 2020-September 2026.

Several industry vendors are in this market with **Fujitsu** and **Hitachi**, plus **Toshiba**, whose Simulated Bifurcation Machine uses a different classical dynamics, simulating adiabatic bifurcations in a network of nonlinear oscillators [3559], and **NEC** with its vector annealing service. This part also includes some related solutions coming from **MemComputing** and **InfinityQ**. Research in that area comes for example from the University of Toronto (Canada) and the University of Rochester (USA) [3560].

Fujitsu

Japan

Fujitsu announced in early June 2018 a digital annealing computer operating at room temperature. Fujitsu is one of the world leaders in the supercomputer market with HPE and Eviden/Atos.

It was therefore logical that they explored ways to upscale their HPC offering. It is supposed to scale much better than D-Wave quantum annealers [3561].

Their digital annealers use custom CMOS DAU chips developed in partnership with the University of Toronto. It is proposed as a cloud offering and is used to solve optimization problems and to carry out molecule screenings. The dedicated chip contains 1,024 bit update blocks incorporating memory to store their weights with a precision of 16 bits, logic blocks to perform value in-

versions and the associated control circuits (Figure 478). This is reminiscent of memristor-based neural networks. As with D-Wave, problems are loaded into the system in the form of graphs with biases in the links between elements and the system looks for a minimum energy state to solve the problem. It has some familiarity with the Ising model used in D-Wave.

Some case studies are available in optimization tasks [3562, 3563]. Toray Industries (Japan) has also been working with Fujitsu since at least 2021 for the development of a new model for drug discovery optimization. **Hidetoshi Nishimori** of the Institute of Science Tokyo, who coauthored the founding paper of quantum annealing in 1998 [184] and advises Fujitsu rather than having designed the Digital Annealer, believes that Fujitsu will be able to create solutions that outperform D-Wave.

In 2019, Fujitsu announced its second generation of chips with 8,192 blocks followed by a third generation with 100K blocks in 2020 and a fourth generation with a 10x speed improvement. They have sold only a few of these machines in Japan and one in Taiwan [3564]. Development tools are provided by **1QBit**, in which Fujitsu has made an investment. Fujitsu has been collaborating since April 2020 with **Quantum Benchmarks** (Canada) on quantum algorithms and error suppression codes, based on an IA Fujitsu algorithm and their experience with their digital annealing [3565, 3566]. Fujitsu is also partnering with **Entanglement** (USA) which developed a Covid vaccine logistics optimization solution with its annealer.

Some announced case studies involve **Toyota Systems Corporation** for supply chain optimization, stadium seat allocation optimization in Berlin, and peptide drug discovery with **Pepti-Aid Corporation**. These are vendor-announced customer engagements rather than independently benchmarked results.

Hitachi

Japan

Hitachi also launched a related initiative although, contrarily to Fujitsu, it seems it did stay in research lab and didn't reach commercialization.

Their system is implementing a hardware solution to solve Ising models. It is mixing probabilistic and deterministic approaches running in a CMOS component to find some energy minimum of a combinatorial problem expressed as an Ising model [3567–3569] (Figure 480). It doesn't find the absolute minimum to the problem but an acceptable solution. The CMOS uses SRAM to store the virtual "spin states" of the Ising model problem. Hitachi stated that it could help solve combinatorial optimization problems such as the travelling salesman problem efficiently. The architecture was first relying on FPGAs which makes sense given it didn't reach volume production.

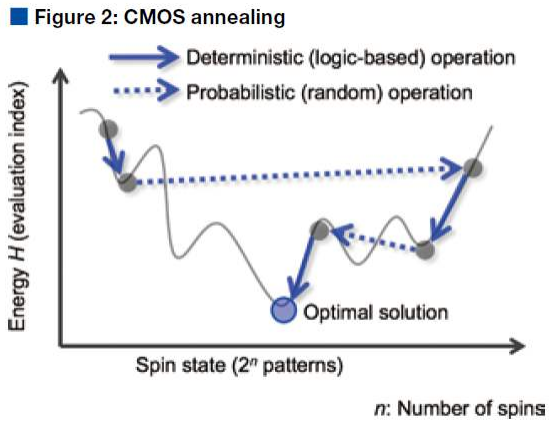


Figure 480: Hitachi CMOS annealing principle.

MemComputing

USA, 2016

MemComputing was created by **John Beane**, a serial entrepreneur, with two physics researchers, **Massimiliano Di Ventra** and **Fabio Traversa,** who have done extensive work on memory computing [3570, 3571].

It can be positioned in a category close to Fujitsu's offer. It is a solution inspired by quantum annealing computation. They use the principle of invertible computing units, able to circulate data both ways, from input to output and output to input.

It also uses oscillating Boolean gates implementing a non-Von-Neumann computing model and some sort of tunnel effect [3572]. Their hardware solution MemCPU Coprocessor is to place memory next to computing units in processing unit [3573] (Figure 481).

These memristor-like computing cells have symmetrical inputs and outputs interconnected to neighboring cells. It computes exclusively with integer numbers. There is no floating-point computing at all. They would automatically find a complex balance of a parameterized system. This is the principle of SOLGs (Self Organizing Logic Gates) shown in Figure 482 [3574, 3575].

The company positions its technology as competing with quantum computing with a market ready solution although its real existence and packaging is in question [3576]. Their architecture is supposed to solve various classes of NP-complete and NP-difficult problems in polynomial time such as 3-SAT problems [3577, 3578]. They tout significant performance gains such as four orders of magnitude for machine learning applications, i.e., performance multiplied by 10,000! Their solution is emulated in conventional computers like with the AMD EPYC microprocessor and provided as an SDK operated in the cloud, which they have designed in partnership with **Canvass Labs** (2017, USA). Their electronic architecture was also prototyped at a small scale using **Analog Devices** standard analog multiplier circuits [3579].

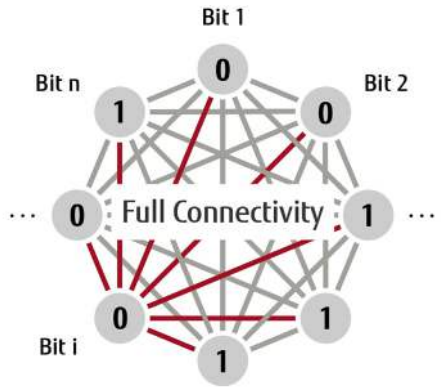


Figure 478: Fujitsu's DAU classical connectivity. Source: Fujitsu.

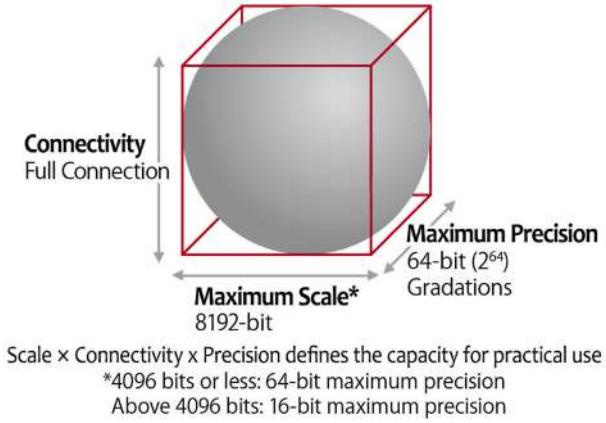


Figure 479: Fujitsu's DAU high-level architecture. Source: Fujitsu.

The application domains include the resolution of planning and optimization problems such as the traveling salesperson problem, combinatorial optimizations and searches [3580], bioinformatics, neural network training [3581] and even integer factoring [3582], each time with the promise of an exponential gain in computing time compared to traditional computing [3583]. They announced that they would need to embed some memristor technology in their component, which could create significant delay in the manufacturing given this technology is not really mature. They handle problems such as MIPLIB (Mixed Integer Programming Library), which are considered intractable with a 60-second response time on a server running Linux and have even beaten a D-Wave. This is used to find a combination of given integers that can generate zero when added together (the "Subset Sum problem").

The company presents speedups of a magnitude usually associated with quantum computing while emulating its process on classical computers. Empirical speed on selected heuristic instances does not establish a polynomial-time worst-case algorithm for an NP-complete problem, and no such claim has been verified independently. Analog dynamics also raise the questions of the precision required as instances grow, of convergence guarantees and of how the encoding size scales, none of which are settled by runtime measurements alone.

In April 2020, MemComputing announced that it would make its XPC (Xtreme Performance Computing) software stack available in the cloud for researchers working on Covid-19 [3584].

Several shortcomings remain unaddressed. The initialization procedure that would place the system close to a global minimum is not described, and the ability to implement SOLGs in current CMOS components at scale has not been demonstrated in hardware.

How is noise managed in their system [3585]? Is the system scaling well? Their approach would not be scalable according to several specialists including Scott Aaronson [3586–3588].

In 2022, MemComputing published two papers in partnership with a scientist from the DoE Los Alamos lab on the potential effect of a tunneling effect with memristors to find global minimum, a task commonly used to solve various optimization and machine learning problems [3589–3591]. All this remains very theoretical.

In 2023, MemComputing published a preprint on its platform capability to factorize large bi-prime integers [3592]. The paper contains a projected estimate of the time needed to factorize an RSA-2048 key, about 100 years on a classical emulation of their platform and tens of minutes on an ASIC version that does not exist. This is an extrapolation from small instances, not a measurement, and it assumes that the convergence behavior and the analog precision required do not degrade over the many orders of magnitude separating the tested instances from a 2048-bit one. The research was funded by the US Air Force.

InfinityQ

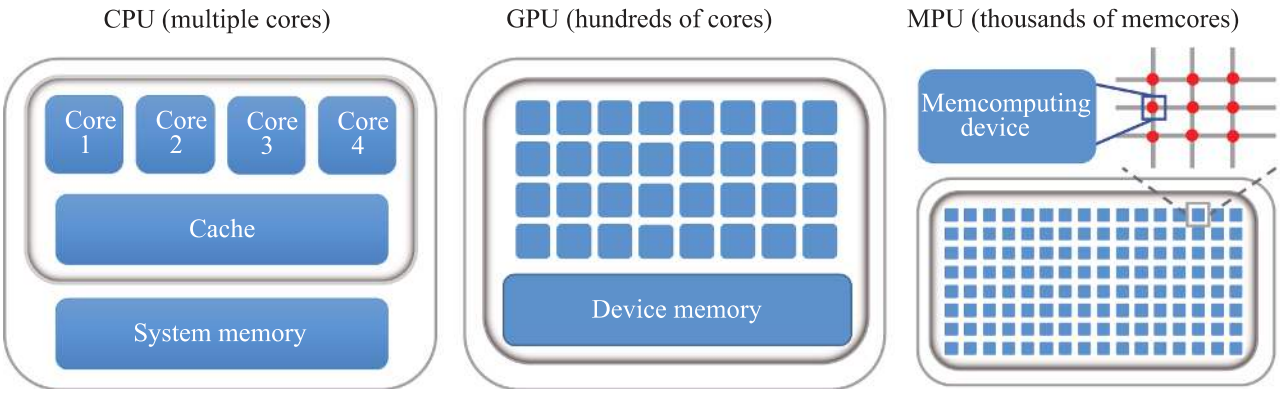
Canada, 2019, $6M

INFINITY|Q⟩

InfinityQ stated initially that they had built the "*first quantum computing CMOS microchip technology to work at room temperature*".

The company was launched by Aurelie Hélouis (CEO) with Kristina Kapanova (CTO, who later left the company) and John Mullen, former Assistant Director of the CIA. Their qubit architecture was presented as an analog quantum computer with between 1,000 and 5,000 qubits. and "*based on an artificial atom in a lambda configuration*" which "*exploits superposition and entanglement to achieve quantum computing without the burden of maintaining very fragile quantum objects*".

It was a cloud native platform and quantum analog-computing technology that could run any coding language, any problem up to 100,000× faster than an av-



(Color online) Comparison of CPU, GPU, and MPU.

Figure 481: MemComputing architecture compared with classical computing. It is basically a mix of in-memory processing with bidirectional computing. Source: MemComputing.

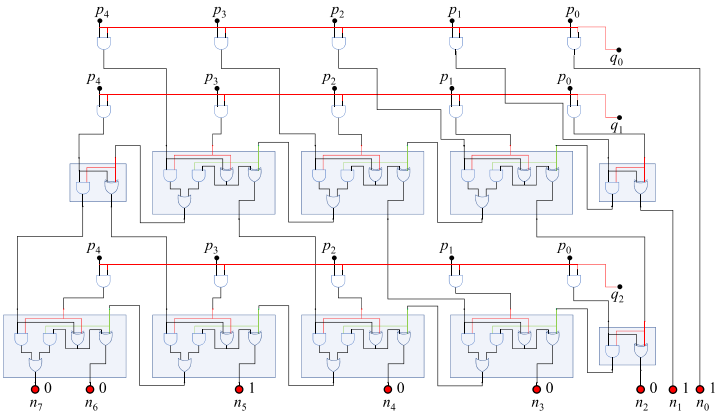


FIG. 2. A possible Boolean circuit that multiplies two integers p and q to give $n = 35 = (100011)_2$ (in the little-endian notation).

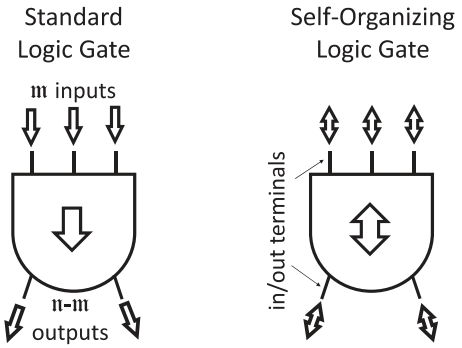


FIG. 3. Left panel: sketch and symbol of a standard $\mathcal{N}$-terminal logic gate with $\mathcal{M}$ inputs and $\mathcal{N} - \mathcal{M}$ outputs. Right panel: sketch and symbol of the corresponding self-organizing logic gate.

Figure 482: SOLGs (Self Organizing Logic Gates) from MemComputing. Source: MemComputing.

erage laptop, with the same energy consumption as a lightbulb. Their first-generation machine was supposed to solve complex optimization problems, linear system and FFTs (fast Fourier transforms). None of these claims was accompanied by a benchmark, a baseline implementation or a stated power boundary.

They created a proof of concept with 10 qubits late 2020 and announced a 100 qubits MVP in 2021 with full commercialization planned after 2025. In April 2021, they mentioned that they had solved a traveling salesperson problem with 128 cities while other "*non-classical machines*" have solved such problems with a maximum of 22 cities, the actual record being 7,515,755,956 steps [3593]. They also made business claims such as having projects starting with major unnamed UK and Canada banks, with a Swiss pharmaceutical and the Canadian government. Their technology could be classified as some sort of reservoir computing running on CMOS doing rabi flops emulation [3594]. Their quantum, superposition and entanglement claims seemed totally overexaggerated.

In 2022, the company made a pivot, reset its website and claimed that its solution was "*A quantum-inspired technology to serve gaming & metaverse's intensive computation demands*", without any hardware being shown. In 2023, they came back with another story, about "the World's largest Ising machine able to handle 112,000 variables, based on a Restricted Boltzmann Machine (RBM), with methods coming from research done by their new CTO Saavan Patel and Sayeef Salahuddin from UC Berkeley. They can solve QUBO and MaxCut formatted problems. The underlying hardware is using one Nvidia A6000 GPU card using an A100 chip. In the end, the company became a service shop providing quantum inspired classical computing solutions, working for example with Siemens Energy Ventures.

3.3 Neuromorphic computing

Neuromorphic processors mimic biological neuron features with integrated memory and processing using memristors [3595]. They can be implemented with spintronics electronics, that imitate how brain cells work with their own memory [3596]. Their main benefit is very low power consumption and good inference performance. Their shortcoming is that in most cases the neural net-

work must be trained classically on another system, although the Loihi family does support on-chip learning rules [3597].

Most neuromorphic processors are currently experimental, like **IBM**'s TrueNorth and its successor NorthPole (Figure 484), the latter being a digital inference accelerator with distributed on-chip weight memory rather than a spiking chip [3598], as well as **Intel**'s Loihi 2 (Figure 485) [3599]. A 2024 benchmark did show that Loihi 2 performed better than a D-Wave annealer using a QUBO reformulation for computing a sparse binary representation of an image [3600].

There is an international proposal to create a neuromorphic computer using quantum memristive devices which play the role of a tunable Mach-Zehnder interferometer. It is actually an optical computing system [3601].

Startups are also present in this domain with **SpiNNcloud Systems** (2021, Germany), a TU Dresden spinout commercializing the SpiNNaker2 chip designed in Christian Mayr's group and derived from Steve Furber's SpiNNaker architecture at the University of Manchester, which is an academic project and not a startup. Their Dresden machine entered operation in April 2025 with 35,000 chips and over five million Arm cores [3602]. **GrAI Matter Labs** (France/the Netherlands) was acquired by Snap in 2023. Interestingly, LLMs including GPT-4 can be used to design such systems, as proposed by researchers from Johns Hopkins University [3603].

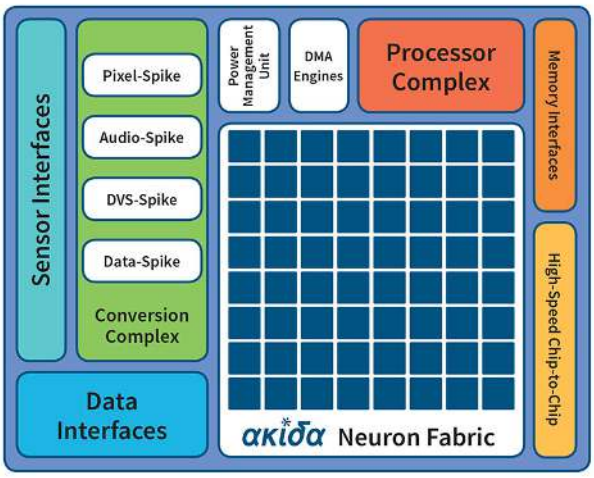


Figure 483: Brainchip Akida NSoC with 1.2 million neurons, 10 billion synapses and 156 mW.

Dynex (2020, Switzerland) is a company specialized in cryptos and Blockchain which developed a concept of neuromorphic computing distributed across either FPGAs or GPGPUs like the ones from Nvidia [3604]. They label it "n-quantum-computing" although nothing in the described architecture is quantum [3605, 3606]. This architecture which supports "one million algorithmic qubits" seems to be based on work from Christof Wetterich from Universität Heidelberg [3607, 3608]. It has some similarities with the architecture proposed by MemComputing. The company published some papers including one on how to conduct integer factorization efficiently on their system, through a QUBO reformulation [3609]. The company was created by Daniela Herrmann, Clifford Mapp, Ivan Petliokha and Samer Rahmeh.

3.4 Analog computing

Analog computing was popular in the 1960s but vanished since then, when all-digital solutions took the helm, including analog signals processing being handled with ADC (analog to digital conversion) and digital computing [3610]. Some startups are starting to revive the technology due to the appetite for energy-saving solutions. They are used for executing deep neural networks [3611] and solving linear equations [3612]. Analog computing, however, has to fight an enemy similar to the one plaguing qubits: noise. And it is hard to evaluate the effect of this noise at scale. At reasonable scales, analog computing may indeed create some energetic computing advantage.

Precision is the historical bottleneck of analog computing. A 2025 result from Peking University attacked it with an analog matrix equation solver on 40 nm 1T1R RRAM arrays with only 3-bit cells, combining a low-precision analog matrix inversion with a high-precision analog matrix-vector multiplication in an iterative loop, plus a block matrix algorithm named BlockAMC. They solved 16×16 real-valued inversion problems, reaching an effective 24-bit fixed-point accuracy after iterative refinement, and matched an FP32 digital baseline on massive MIMO signal detection in three iterations [3613]. That FP32 equivalence is relevant for this kernel size, this condition-number range and this application, and does not generalize. The refinement loop stays analog, avoiding the analog-digital conversions that ate most of the benefit in earlier hybrid schemes, although the ADC and DAC boundary still frames any end-to-end energy accounting. The press coverage turned this into a 1,000× speedup over high-end GPUs, which is a throughput extrapolation for one narrowly defined kernel, not a measured system-level result. A 16×16 block inversion is also several orders of magnitude away from the matrix sizes that would matter in HPC or AI training, and RRAM conductance drift over time remains unaddressed at that scale.

Mythic

USA, 2012, $172M

Mythic creates analog and in-memory processing modules for embedded systems. Their chips embed an ADC array, an analog matrix computing unit using tunable resistors and an ADC array that translates back the results into digital format. It is used for neural network matrix operations, for multiplying an input vector by a weight matrix.

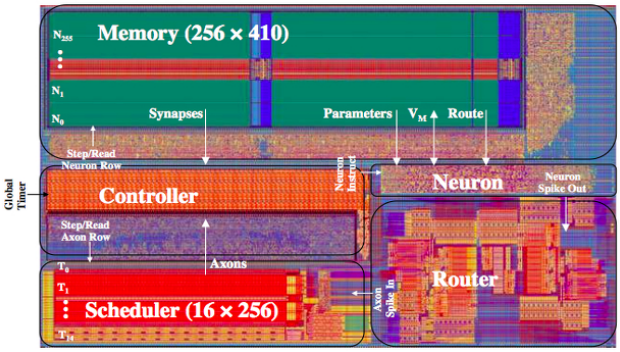


Figure 484: IBM TrueNorth processor, with one million neurons and 256 million synapses and 70 mW power.

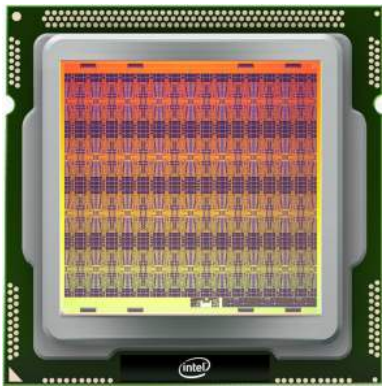


Figure 485: Intel Loihi 2 with 1 million neurons and 120 million synapses.

Anabrid

Germany, 2020

Anabrid is a manufacturer of classical analog computers for the industry. They are participating in the DLR project REDAC (Reconfigurable Discrete Analog Computer) [3614].

3.5 Reversible and adiabatic computing

Since the 1960s, researchers have been considering reducing computer power consumption by several orders of magnitude based on the principle of adiabatic reversible computing [3615] (Figure 487). The goal is primarily energy-based. It does not accelerate computing. In most cases, it is even contradictory with Moore's law, as the main techniques used result in a calculation speed decrease.

3.5.1 Science

All this is due to our understanding, since the 1960s, of the link between computation and thermodynamic processes. **Rolf Landauer** showed in 1961 that a logically irreversible operation, typically the erasure or reset of a bit, must dissipate a minimum amount of energy into the environment, under specified thermodynamic assumptions of an isothermal reservoir at temperature T and a quasistatic process [3616–3621]. The bound applies to logical irreversibility, not to information processing in general.

The erased information is turned into heat sent to the environment, increasing its entropy. The dissipated energy per erased bit is at least $\mathbf{k_B T \ln 2}$, k_B being the Boltzmann constant (1.380649×10^{-23} J K^{-1}), T the reservoir temperature in kelvin and ln 2 the natural logarithm of 2 (about 0.69315). At room temperature (300 K), this gives 2.87×10^{-21} J, or 0.018 eV.

This is the famous Landauer limit. Landauer's limit was experimentally verified fifty-one years later, in 2012, by a team from ENS Lyon in Sergio Ciliberto's group [3622–3625] (Figure 488).

More generally, Landauer's limit illustrates the link between the notions of logical and physical reversibility of computation. The first is linked to the ability to determine the input values of a calculation according to the output values.

The second is that the execution of a physical process in reverse may not violate the laws of physics, including the second law of thermodynamics, according to which the entropy of an isolated system never decreases. Total entropy production can approach zero only in the limit of an ideal quasistatic reversible process, which also takes an unbounded amount of time.

Today, a CMOS logic transition dissipates of the order of 5,000 eV, almost 300,000 times more than the Landauer bound. That comparison depends on the technology node, the supply voltage, the operation considered and the energy boundary used, so it is an order of magnitude rather than a specification. One could gain an order of magnitude and go down to 500 eV, but that would still be 30,000 times more than the Landauer limit. So, in order to reduce the computing energy consumption, why not avoid erasing information and, in the process, make all computing physically and logically reversible? This would require a review of all current computational logic that relies at low-level on irreversible logic gates that destroy information, such as NAND or XOR gates that generate one bit from two bits.

In 1973, **Charles Bennett**, another IBM researcher and colleague of Rolf Landauer's, imagined a calculation method that would avoid this energy-dissipating erasure of information without requiring an infinite memory [3626].

He was followed by **Edward Fredkin** and **Tommaso Toffoli** who, in 1978 and 1982, imagined reversible logical gates inspired by a metaphorical physical model based on billiard balls, the BBM for billiard ball model [3627]. These logic gates have as many outputs as inputs and it is easy to understand why they become

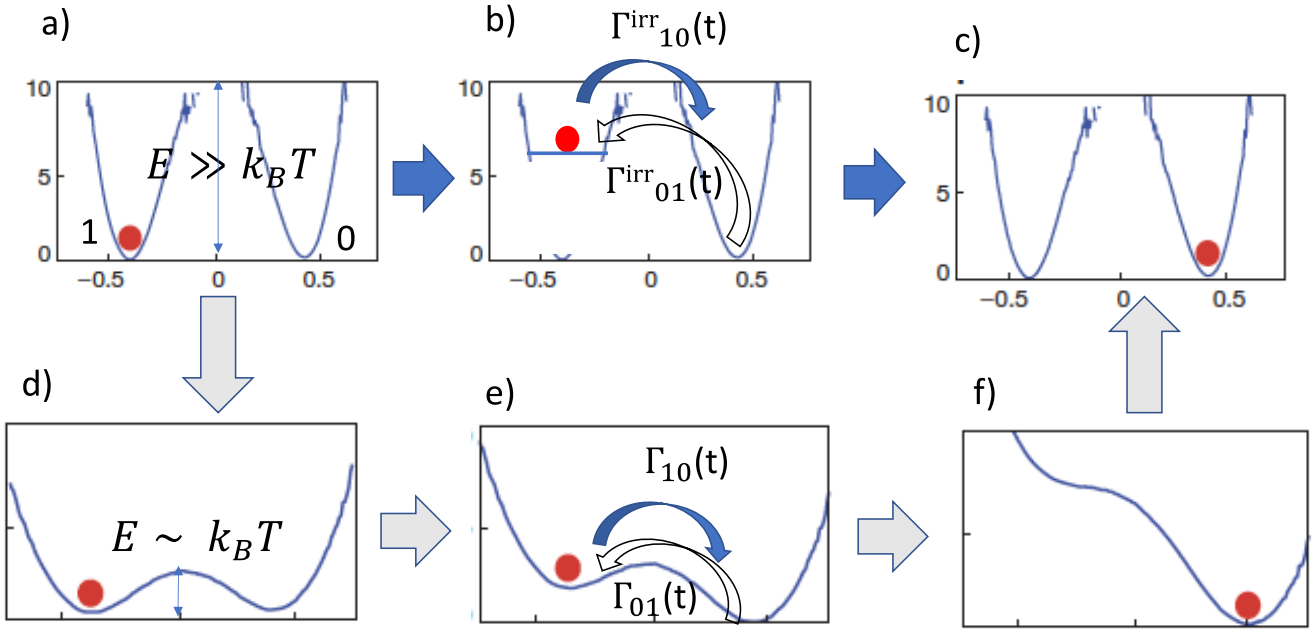


Figure 486: The thermodynamic principle of reversible computing. Source: "Thermodynamics of computing, from classical to quantum" by Alexia Auffèves, May 2020 (11 pages), adapted from [3622].

reversible. Although their model was not practically feasible with contemporary electronics, it was then applied to the quantum equivalent of these gates that we already covered.

Konstantin Likharev proposed in 1976, then in 1982, to implement this reversible computational logic by manipulating the energy levels of superconducting Josephson junctions, under the name of "parametric quantrons" [3628].

This became the "Quantum Flux Parametron" (QFP), capable of operating up to 10 GHz, invented by Eiichi Goto's group in the mid-1980s and developed by a Japanese team into the Josephson supercomputer element described in 1991 [3629].

This led then in 2003 to **Vasili Semenov**'s idea to use nSQUID circuits to realize these circuits, the n meaning "negative" because of a negative inductance that connects two SQUIDs of the device. As for any Josephson junction, it works under cryogenic temperature. nSQUIDs are double SQUIDs (Superconducting Quantum Interference Device) connected by a negative inductance, a system used to accurately measure the magnetism of superconducting Josephson effect loops. These nSQUIDs were manufactured by Hypres [3630].

Reversible computing is often associated with adiabatic computing but one could work without the other. The general principle of adiabatic computing is illustrated in Figure 486: in a classical calculation, the energy barrier to switch the state of a system between a) and c) is high. In a quasi-adiabatic calculation, a physical system lowers the state energy transition barrier (in d) to trigger it (in e) and then in f, by raising the level of the barrier to its normal state.

The processing energy cost is thus lowered by approaching Landauer's limit. The high level of the non-calculation barrier guarantees the stability of the information managed outside of this operation. Lowering the barrier and raising it are often managed by trapezoidal voltage control of the transistors instead of looking like a square wave signal.

Between 1985 and 1993, reversible or partially reversible CMOS and CCD computing components were designed. **Craig Lent** then proposed in 1997 an adiabatic computation system based on quantum dots and cellular automata (QCA for Quantum dots Cellular Automata) to operate up to 100 GHz [3631].

In the same manner, **Krishna Natarajan** suggested in 2004 to use MEMS (electro-micro-mechanical components) to drive the trapezoidal voltage control necessary to create adiabatic CMOS components with a very low energy dissipation of 1 eV [3632].

The idea was pursued by a team from **CEA-Leti** and **Delft** in the Netherlands in 2017 and **Ralph Merkle** in 2019, with prototype circuits based on this kind of technology [3634].

In 2012, **Alexei Orlov** et al. experimentally probed Landauer's bound with a few discrete classical electronic components, resistors and capacitors [3633] (Figure 488). Their experiment showed that a bit copy, which is a logically reversible operation, can be performed with an energy below $k_B T \ln 2$, at the price of slowing down the operation. This does not overcome the erasure bound. The copy leaves the information in the system, and the logically irreversible reset that eventually clears it must still pay at least $k_B T \ln 2$ per bit.

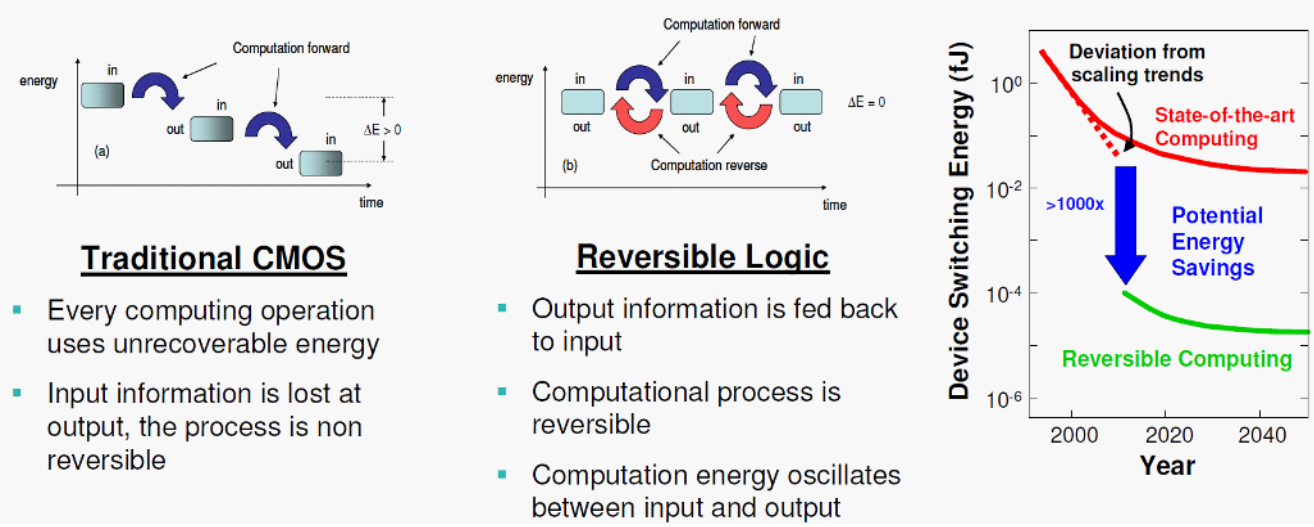


Figure 487: Why reversible logic could help save energy. But it won't make it faster. Source: [3615].

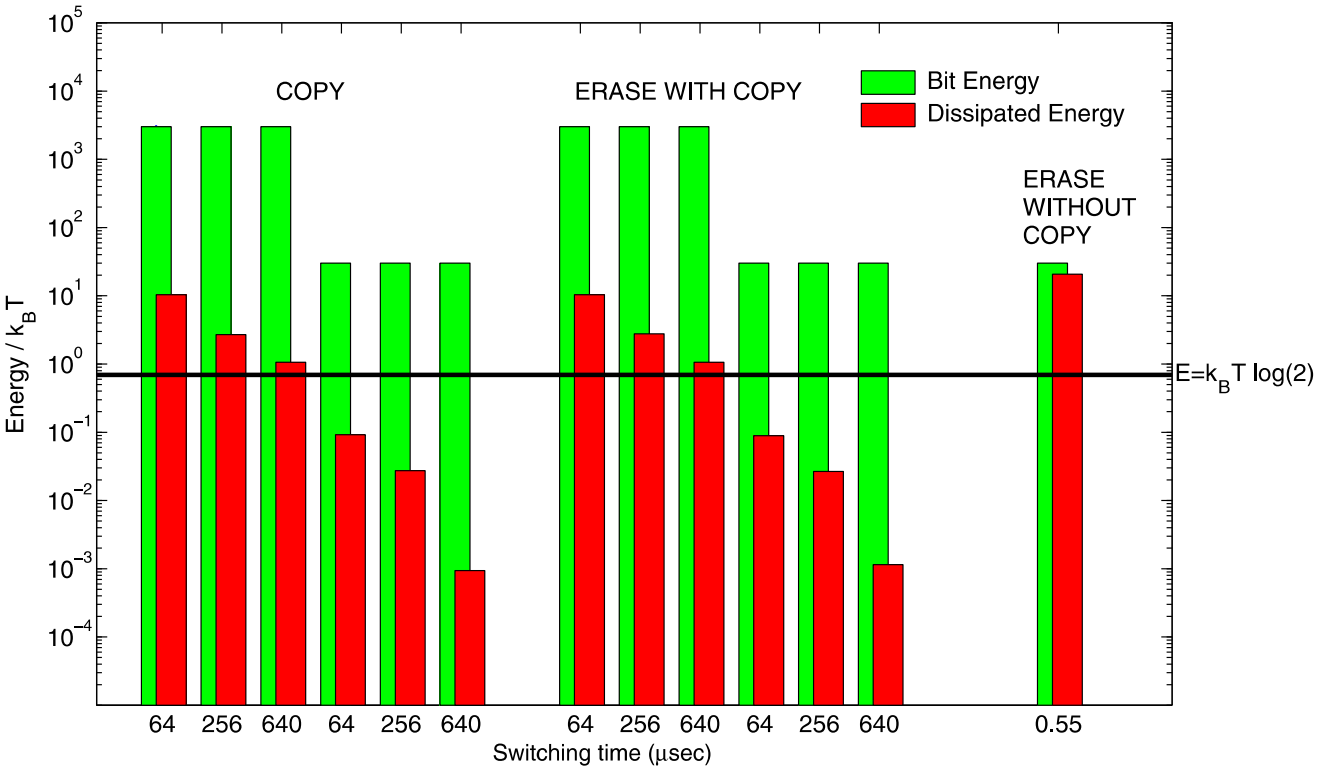


Figure 488: Alexei Orlov Landauer's validation experiment in 2012. Source: [3633].

Plain erasure did consume more energy than the Landauer bound, as the model requires, and the whole experiment worked at room temperature. In 2019, Alexei Orlov's team from Notre Dame University in Indiana produced the equivalent of an 8-bit microcontroller using a subset of a RISC-type MIPS instruction set with 5,766 transistors, 40% of which are adiabatic [3635, 3636]. This seems to be, to date, the most successful realization of a reversible adiabatic processor. It remains, however, experimental and far from industry requirements. Its industrialization could be of interest to create microcontrollers for low power connected objects.

However, this adiabatic CMOS technique requires a larger number of transistors. Therefore, emerges a new trade-off between a larger and more expensive to design and manufacture power saving component vs cheaper but more energy hungry conventional counterparts. Still, the environmental cause has revived interest in reversible and adiabatic computing. It is promoted by the Computer Community Consortium group of the American **Computing Research Association** with the lead from Michael P. Frank's team at **Sandia National Labs**. It published in 2019 a manifesto to develop thermodynamically responsible computing inspired by biomimicry. The document was the result of a work-

shop with about 40 participants, almost all American except one researcher from London and another from Luxembourg, from universities and a few private actors such as Google, Rigetti, HPE, Knowm (which develops memristor-based circuits for AI applications, their kT-RAM technology) and Daptics (ex Protolife, created by Norman Harry Packard (1954) and which develops chemical simulation algorithms) [3637].

They position it as an intermediate architecture between classical and quantum computing, but on quantities that are not necessarily relevant (dimension of components and duration of state fluctuation, see Figure 490) [3621, 3638]. The purpose of the manifesto was to obtain US federal credits to finance this research. So, the story is not over!

A different path was proposed in 2026 by **Daniel Loss** now affiliated with KFUPM in Saudi Arabia and the University of Basel. It proposes to implement classical reversible logic with the coherent spin dynamics of a semiconductor spin quantum-dot array, with inputs and outputs staying in classical basis states and no algorithmic use of superposition [3639]. The same spin stores, transports and computes, unitary rotation replacing irreversible switching. It is neither quantum computing nor adiabatic CMOS since the logic acts on spin instead of charge. Dissipation then comes from applied voltages, decoherence, readout, reset and information erasure. The paper includes an energy analysis of the classical control electronics. It remains a proposal, with just a one-bit reversible adder. The application domain would be the implementation of energy-efficient AI inferences.

Momentum computing is another way to escape the speed vs energy trade-off of adiabatic computing. It was proposed in 2021 by **Kyle J. Ray** and **James P. Crutchfield** from the Complexity Sciences Center at UC Davis [3640]. Instead of storing a bit in the position of a particle in a double-well potential and moving it slowly to stay close to equilibrium, the information is temporarily carried by momentum degrees of freedom. During an operation, the barrier is lowered, the system evolves ballistically in phase space like a pendulum swinging from one well to the other, and the barrier is raised again once the target state is reached. The dynamics are far from equilibrium and non-Markovian, outside the scope of the usual stochastic thermodynamics which assumes detailed balance. As a result, the work cost does not scale as $1/\tau$ with the operation duration τ as with adiabatic protocols, and there are optimal durations which are both fast and energy efficient.

In 2023, the same team proposed an implementation with a gradiometric flux logic cell, a two-Josephson junctions superconducting loop similar to the quantum flux parametron seen above, operating in the classical regime below 1.5 K. The building block of the Fredkin gate and thus, of universal reversible computing, has ns-scale operations with a fidelity above 99% and a work cost as low as 0.43 $k_B T \ln 2$, most explored protocols staying under 10 $k_B T \ln 2$, to be compared with 10^3 to 10^4 $k_B T \ln 2$ for a CMOS gate [3641]. Fidelity and energy efficiency both improve. In July 2022, James Crutchfield anticipating a 1,000 to 10,000-fold energy reduction, simple circuits within a couple of years and full microprocessors by 2030. The "sub-Landauer" claim is questionable. A swap is logically reversible and its Landauer cost is zero, $k_B T \ln 2$ being only used as a reference scale. But the simulations doesn't account for the energy of the flux control pulses and their control electronics, and the cryogenics. Junction critical current asymmetries also degrade performance. Irreversible gates were studied in 2026 with coupled quantum flux parametrons implementing a NAND gate, where a momentum-driven reversible step speeds up erasure, with finite-time work costs one to two orders of magnitude above the 0.347 $k_B T$ thermodynamic minimum [3642]. As of early 2026, momentum computing had not yet been demonstrated experimentally, even with a single gate. So Crutchfield's 2030 microprocessor target will be at least delayed!

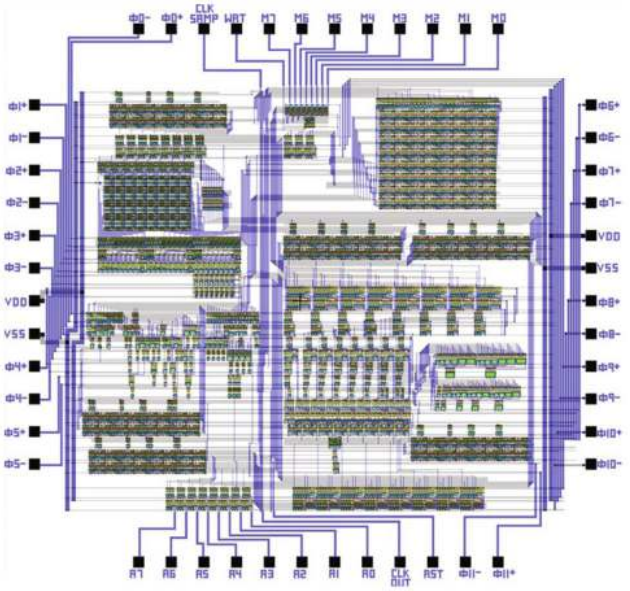


Figure 489: Notre Dame University's equivalent of an 8-bit microcontroller using a subset of a RISC-type MIPS instruction set with 5,766 transistors, 40% of which are adiabatic. Source: [3635].

3.5.2 Vendors

Vaire Computing

UK, 2021, $4.5M

Vaire Computing is using reversible computing to reduce the power consumption of AI applications. It was created by Rodolfo Rosini (CEO) and Hannah Earley (CTO), a Cambridge University researcher, and is based in London with a Seattle office. Michael P. Frank, whose Sandia team drove the CRA manifesto mentioned above, joined as chief scientist. They claim to implement "*near-zero energy computing*". In 2025, the company disclosed its first test chip manufactured in 22 nm CMOS, code-

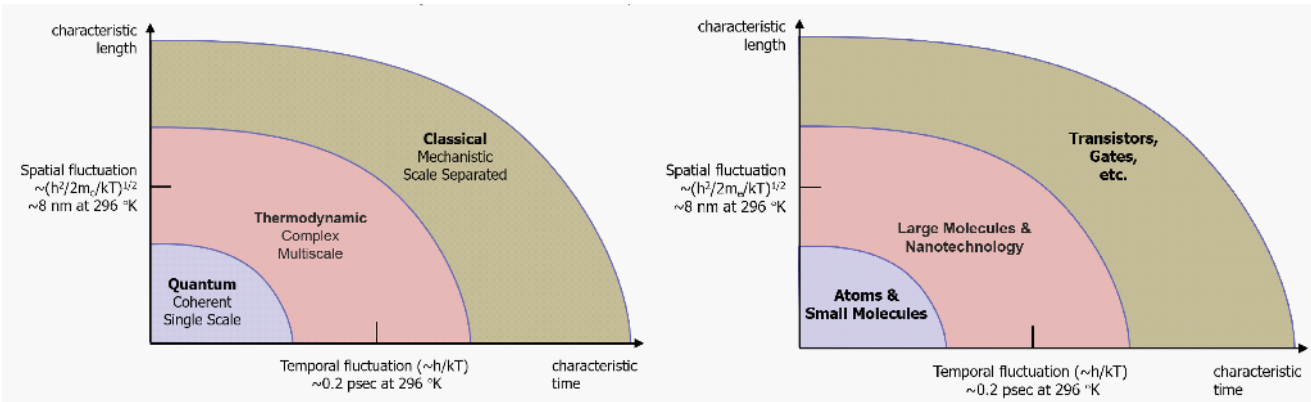


Figure 490: The range of thermodynamic computing, between quantum and classical computing, and between the quantum level and the usual macroscopic level. Source: [3637].

named Ice River. As reported by the company in 2025, it demonstrated energy recovery using an adiabatic resonator design, with an energy recovery factor of 1.77 on a capacitor array and about 1.4 on a shift register, for roughly 30% less energy than an equivalent square-wave driven circuit, running at 500 MHz with a 1 GHz target. These are component-level measurements on test structures, not processor-level energy figures, and the first-silicon claim comes from the company rather than from an independent measurement report. A 1.77 recovery factor also remains several orders of magnitude away from the Landauer bound and the trade-off with transistor count is unchanged.

3.6 Thermodynamic computing

Thermodynamic computing sits at the opposite end of the spectrum from reversible computing. Instead of fighting dissipation, it uses the natural relaxation of a physical system towards equilibrium as the computation itself. A system is programmed by encoding a matrix in its energy landscape, released, and its equilibrium statistics are read out. Gaussian sampling, matrix inversion and linear system solving then become physical processes rather than instruction sequences [3643]. The main benefit is energy related, since the samples the hardware produces are what costs with generative and probabilistic AI. The catch is thermalization time, which grows with the condition number of the encoded matrix and can wipe out the advantage.

That bottleneck is being attacked algorithmically. Mattia Moroder, Felix Binder and John Goold at Trinity College Dublin proposed a hybrid digital-thermodynamic scheme where a classical processor computes an initialization that suppresses the slow relaxation modes, inspired by the Mpemba effect, after which the physical system finishes the job through its own dynamics [3644]. Working on overdamped Langevin dynamics with quadratic energy landscapes, they derived the optimal initial covariances from the spectrum of the Fokker-Planck operator and obtain a predictable thermalization speedup set by the spectrum of the encoded matrix. It is still some analytical work on an idealized model.

Normal Computing

USA, 2022, $75M

Normal Computing was created in New York by former engineers from Google Brain, Google X and Palantir, including Faris Sbahi. They implement thermodynamic computing to solve linear algebra problems, including matrix inversion, and optimize AI applications in an energetic efficient fashion [3645]. Their first circuit was labelled a "*stochastic processing unit (SPU)*", eight RLC unit cells all-to-all coupled through switched capacitances on a printed circuit board, demonstrating Gaussian sampling and 8×8 matrix inversion in 2023 [3646].

In 2025 the company moved away from that analog route and taped out CN101, a digital thermodynamic computing chip built in standard CMOS using stochastic computing primitives. The accompanying paper formalizes equilibration-style thermodynamic computing in a substrate-independent way, the point being that physical relaxation primitives can be realized entirely in digital logic [3647]. This makes scaling far more credible than an RLC board, at the cost of giving up the free physical randomness that was the original selling point. They also work on Normal EDA, an AI-for-chip-design software tool.

3.7 Superconducting computing

The idea of creating superconducting computers capable of taking advantage of the lack of resistance of low temperature electronic components dates to the early 1960s. Its history evolves in parallel with reversible and adiabatic computing. It started with the discovery of the Josephson effect in 1962. This effect was later used to create two-states superconducting qubits with research starting in the early 1980s.

3.7.1 Science

The expected benefits of superconducting logic are an increase in clock frequency and a decrease in power consumption. The power gain is usually quoted between 10 and 1,000, but the figure depends entirely on whether the refrigeration input power is included, on the logic family, on the fabrication node and on the workload. Most published numbers count only on-chip dissipation at 4 K, where extracting one watt typically costs several hundred watts of wall power. The integration level is currently low, of the order of 200 nm, compared to the 2 nm and 3 nm marketing nodes of the densest CMOS processors in 2026, which correspond to physical transistor dimensions of about 48 nm. But it is steadily increasing. There are even investigations to combine superconducting transistors, optoelectronics and neural networks [3220, 3648].

The gain is more significant with the clock frequency than with energy consumption. For example, a Japanese SFQ 8-bit multiplier realized in 2019 ran at 48 GHz while dissipating 5.6 mW on chip, which the authors translate into about 2.5 TOPS/W, in the range of the deep learning CMOS chips of the same period [3649] (Figure 491 and Figure 492). That efficiency figure counts on-chip dynamic power only, at a single arithmetic precision, and excludes the 4.2 K refrigeration input power.

Several generations of superconducting components have been developed over time [3650, 3651]:

- **SFQ** (Single Flux Quantum) was a first-generation circuit, limited to clock frequencies between 300 MHz and 1 GHz. IBM's Josephson computer program ran from 1969 to 1983, was partly funded by the NSA and was abandoned in 1983, but it used latching Josephson logic rather than SFQ proper, single flux quantum logic emerging afterwards from Likharev's group [3652]. D-Wave's superconducting qubit use SFQ-type components for generating and reading qubit control signals [213].

- **RSFQ** (Rapid Single Flux Quantum) was coinvented in Russia in the mid-1980s by Konstantin K. Likharev and his then-PhD student Oleg Mukhanov. Mukhanov then moved to the USA and joined Hypres in 1991 to launch the industry development of RSFQ. The first ones were produced in the mid-2000s [3250] (Figure 493). They have the advantage of being able to operate up to 750 GHz. They can be used to create ALUs (Arithmetic Logic Units [3653]) running at 20/30 GHz as well as ADCs (analog to digital converters) running up to 40 GHz.

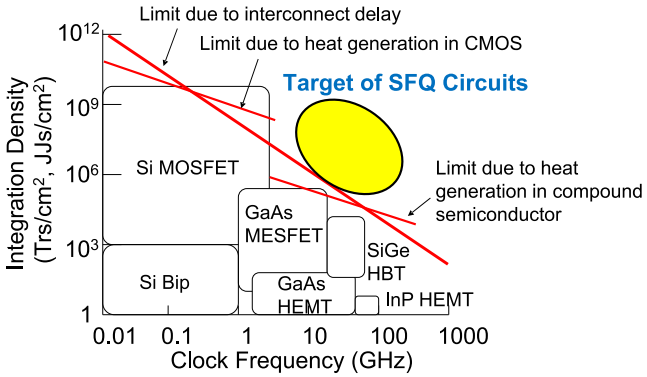


Figure 491: Schematic positioning SFQs in terms of clock speed and integration compared to traditional electronic components. Source: [3654].

- In SFQ logic, information is represented by quantized magnetic-flux states and transferred as picosecond voltage pulses associated with single flux quanta [3655]. The computation does not use coherent qubit superposition or entanglement as in superconducting qubits. **Hypres** develops radio frequency reception systems using two superconducting components: **SQUID** (Superconducting Quantum Interference Device) based antennas that allow magnetism to be captured with precision (invented in 1964) and an RSFQ chip running at 30 GHz with 11K JJ (Josephson junctions) [3656]!

- **AQFP** (Adiabatic Quantum Flux Parametron) which comprises two superconducting Josephson loops connected together by an inductance, reminiscent of the nSQUID principle [3657, 3658]. The process is very energy efficient due to its ability to be reversible. A recent work from Japanese researchers prototypes an AQFP processor using 20,000 Josephson gates operating at 4.2 K [3659].

- **RQL** (Reciprocal Quantum Logic) [3660], **eRSFQ** (Energy Efficient RSFQ) and **eSFQ** (Energy Efficient SFQ) are variants of the RSFQ that are more energy efficient due to the absence of bias resistance, replaced by an inductance. This is the variant chosen by Hypres and its subsidiary SEEQC. Their SFQs combine eRSFQs, of which they are the originators, and eSFQs. RQLs are studied to create superconducting memories.

- **SFETs** (Superconducting FETs, Field Effect Transistors) which implement a concept similar to adiabatic CMOS, but with a superconducting component. These components have been developed since the 1980s [3661, 3662].

There are a few other variants of superconducting components that I will just mention (SSV, SVJJ, STTJJ, S3JJ) because they do not seem to be common, on top of JMRAM that is investigated for implementing superconducting memory.

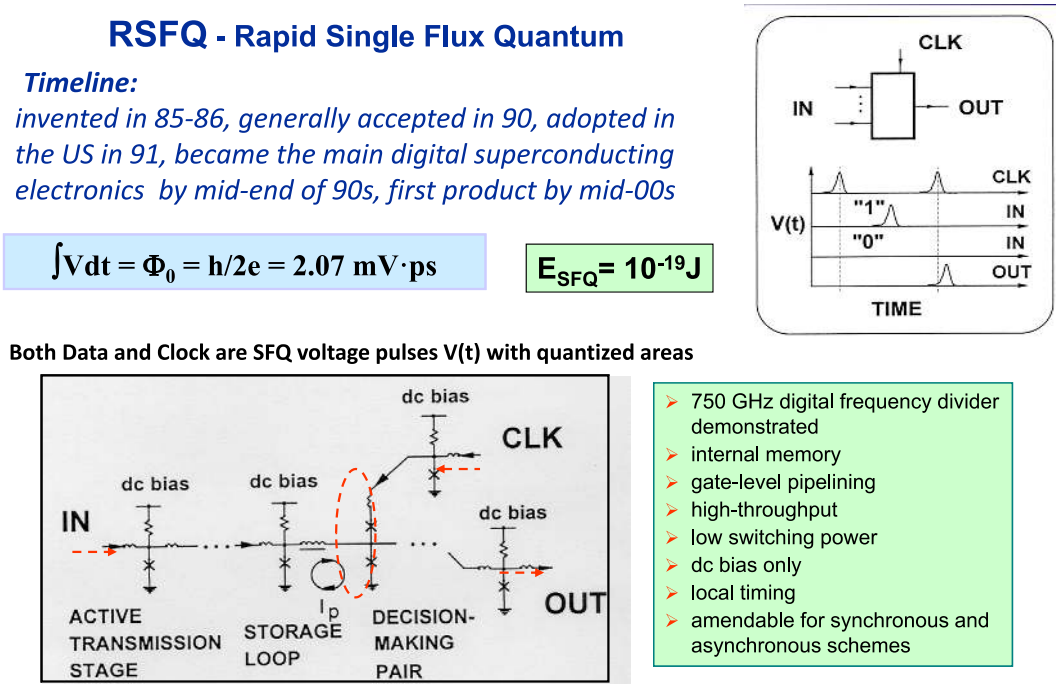


Figure 492: RSFQ basic architecture.

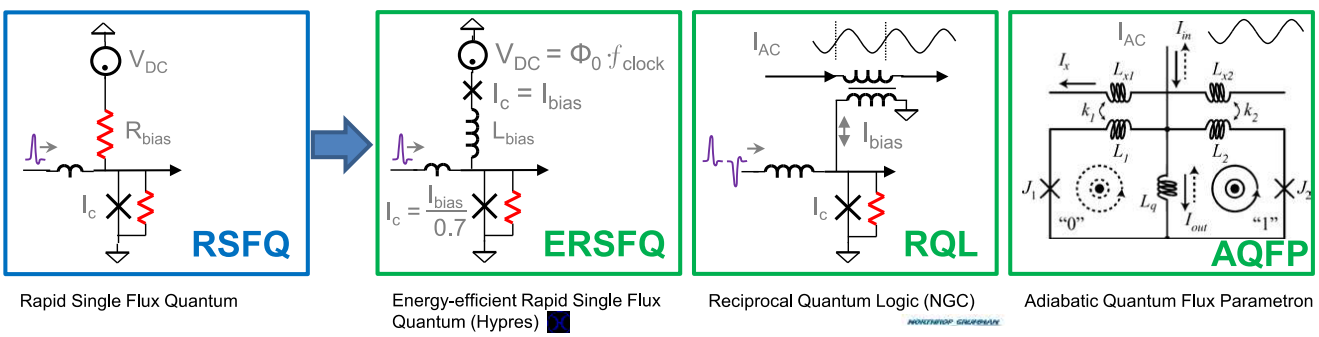


Figure 493: RSFQ and its evolutions, ERSFQ, RQL and AQFP. Source: [3250].

Some researchers are also looking into the way to create superconducting diodes using the Meissner effect, which could be useful in creating superconducting computing solutions [3663].

To date, the integration record for this type of component is only 144,000 Josephson junctions in a chip, realized in a 248 nm integration [3664] if we don't account for D-Wave's Pegasus chip with its million Josephson junctions including about 10,000 JJs used in their annealer qubits, the rest being used for qubit-control logic and for digital signal multiplexing and demultiplexing.

Another key component has been developed, superconducting diodes with zero resistance in one direction. It was experimented in 2022 with europium sulfide thin film separating a superconducting aluminum and a normal metal copper layer [3665] and, separately, with niobium bromide placed between layers of niobium diselenide [3666].

In the mid-2000s, the **NSA** invested $400M in RSFQ over the 2005-2010 period. Its goal was to create a processor with one million logic gates running at 50 GHz. The NSA document describing the project is surprisingly detailed and highly informative. It reveals the scope of the related technological challenges [3667] (Figure 494). In particular, for creating cryogenic memories, superconducting or not: CMOS-Josephson junction hybrid, spintronic based [3668, 3669], SFQ or monolithic RSFQ-MRAM. Then the communication between the cryogenic electronics and room temperature components, with a 25 Gbits/s optical fiber that we would probably now reach 100 or 200 Gbits/s, leaving aside the question of the optical signal modulation and demodulation.

Cryogenics must be sized to support a large number of components. For testing purposes, a simple pulse tube would be sufficient but more imposing installations are planned as computing power would grow, as in the illustration in Figure 495.

The project relied mainly on **Hypres,** the only American company entirely dedicated to the creation of superconducting components, who did run its own foundry from 1983 until about 2020. It then divested it to SEEQC

and now seems to rely on SkyWater's foundry. They were supplying radio frequency components for military use cases. Out of this, they developed an 8-bit RSFQ processor containing 28,000 Josephson junctions.

There is also **Northrop Grumman** with its foundry located in Linthicum, Maryland. Finally, **Chalmers University** in Sweden and various research laboratories in the USA (JPL, Berkeley, Stony Brook) as well as the **NIST** Boulder laboratory were also involved. **IMEC** has a lab in Florida that designs superconducting circuits with densities in the 10 nm to 20 nm range.

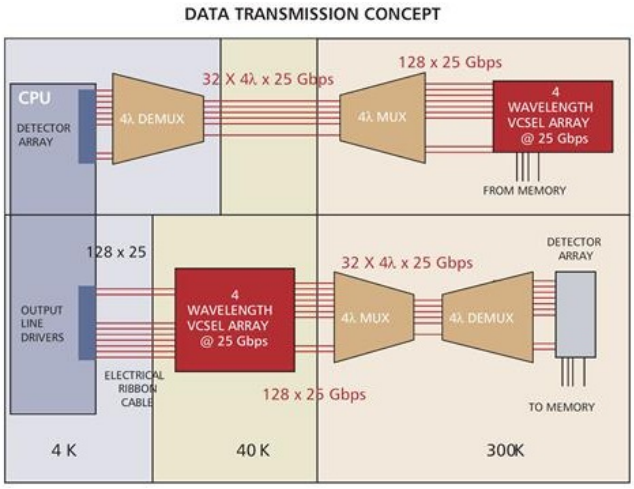


Figure 494: A 64-fiber system for bi-directional transmission totaling 6.4 Tbps between a superconducting processor operating at 4K and high speed mass memory at ambient temperature. Optical connections are shown in red and electrical in black. This technology was planned to be available by 2010. Source: [3667].

The **IARPA** agency has taken over with the **Cryogenic Computing Complexity** (C3) project launched in 2014. It involved IBM, Northrop Grumman (Quentin Herr, who worked at IMEC in Florida since May 2021 and launched with his wife Anna Herr the startup Snowcap Compute in 2024), Raytheon and Hypres and was due to end in 2018 [3670] (Figure 499). It ended in 2022. A total of $700M was spent on R&D there given the project was considered to be strategic. Some of the showstoppers there were the lack of EDA tools (electronic design automation) adapted to superconducting circuits and of scalable cryogenic cabling (leading to the Supercables project). There are solutions based on frequency up-conversion of the signals to optical wavelengths with VCSEL chips, but these are consuming a lot of energy. This project was part of the **National Strategic Computing Initiative** (NSCI) launched in 2015 by the White House, which focused on the development of supercomputers. It is difficult to find out what this project has achieved (Figure 498).

In the USA, the **DISCoVER** (Design & Integration of Superconductive Computation for Ventures beyond Exascale Realization) expedition is working on a "SuperSoCC" SFQ-based niobium chip (superconductive system of cryogenic computing cores) operating at 4.2 K. The project is led by Massoud Pedram, Timothy Pinkston and Murali Annavaram from USC. They are working on on-chip memory design and interface between room electronics and cryo-electronics. The team targets a potential energy reduction by a factor of 100 compared to classical computing, or a 10× speed improvement at the same energy consumption, neither figure being tied yet to a stated workload or cooling boundary.

With a relatively modest funding of $15M coming from the NSF, the project also involves Auburn University, Cornell University, Northeastern University, Northwestern University, University of Rochester and Yokohama National University in Japan.

Outside the USA, the **Japanese Superconducting Computing Program's** ambition in 2004 was to create a processor running at 100 GHz generating 100 GLOPS in SFQ, supplemented by 200 TB of DRAM running at 77K to generate a 1.6 PFLOPS system comprising 16,384 processors (Figure 500).

All this with a cryostat consuming 12 MW and generating a thermal power of 18 kW at 4.2K. It has not yet seen the light of day more than twenty years later.

They managed to create the CORE1α in 2003 at 4,999 JJ (Josephson junctions) running at 15 GHz, the CORE1β in 2006 at 10,955 JJ running at 25 GHz, the CORE1γ with 22,302 JJ also at 25 GHz, the CORE100 in 2015 at 3073 JJ and 100 GHz, the COREe2 in 2017 at 10,655 JJ and 50 GHz with an integrated memory [3654]. This continued in 2019 with an 8-bit multiplier containing 20,251 JJ running at 48 GHz and consuming 5.6 mW [3649].

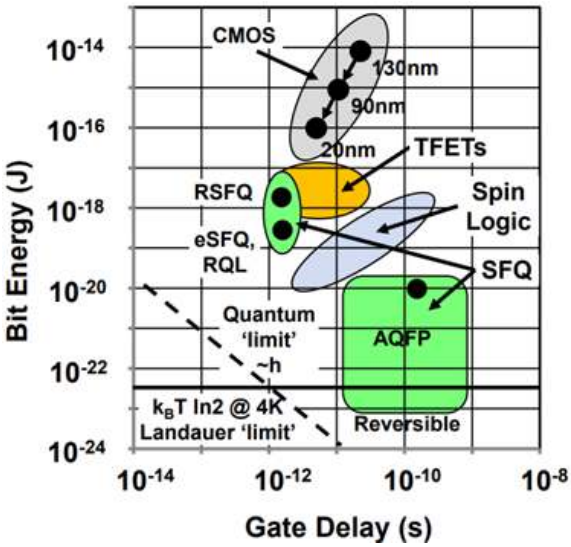


Figure 498: Superconducting approach and gate delay. Source: [3670].

Meanwhile, the IBM Summit supercomputer using traditional processors and GPUs generated 200 petaFLOPS consuming 13 MW, so why bother? Researchers from the US Navy are working on a superconducting cir-

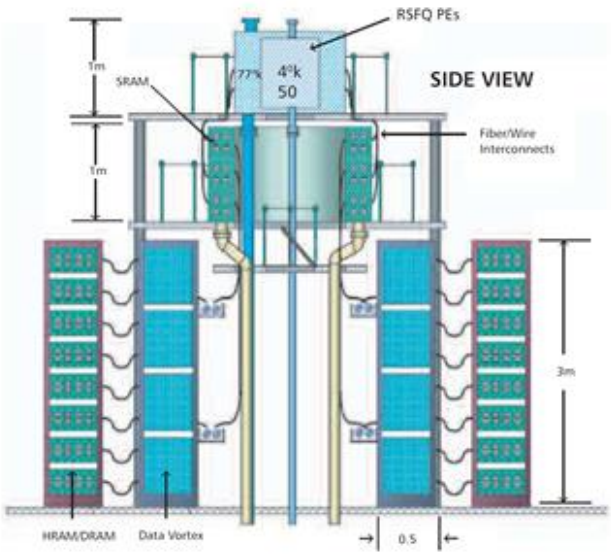


Figure 495: Concept for a large-scale system including cryogenic cooling unit for supercomputers. Source: [3667], pages 100 and 125.

TABLE 3.2-2. STATUS OF LOW-LATENCY CRYO-RAM CANDIDATES

Type/Lab	Access Time	Cycle Time	Power Dissipation	Density	Status
Hybrid JJ-CMOS (UC Berkeley)	500 ps for 64 kb	0.1 - 0.5 ns depending on architecture	12.4 mW read 10.7 mW write (Single cell writing)	64 kb in < 3x3 mm²	All parts simulated and tested at low speed
RSFQ decoder w/ latching drivers (ISTEC/SRL)	?	0.1 ns design goal	107 mW for 16 kb (Estimate)	16 kb in 2.5 cm² (Estimate*)	256b project completed (Small margins)
RSFQ decoder w/ latching drivers (NG)	?	2 ns	?	16 kb/cm² *	Partial testing of 1 kb block
SFQ RAM (HYPRES)	400 ps for 16 kb (Estimate)	100 ps for 16 kb (Estimate)	2 mW for 16 kb (Estimate)	16 kb/cm² *	Components of 4 kb block tested at low speed
SFQ ballistic RAM (Stony Brook University)	?	?	?	Potentially dense Requires refresh	Memory cell and decoder for 1 kb RAM designed
SFQ ballistic RAM (NG)	?	?	?	Potentially dense Requires refresh	SFQ pulse readout simulated
MRAM (40K)	Comparable to hybrid CMOS	Comparable to hybrid CMOS	< 5mW at 20GHz (Estimate)	Comparable to DRAM (Estimate)	Room temperature MRAM in preproduction; Low temperature data sparse

*Densities of JJ memories are given for the technologies in use at the time of the cited work. Greater densities can be expected when a 20 kA/cm² process is used. The symbol ? signifies insufficient data.

Figure 496: Cryo-RAM projects also related to C3.

cuit implementing Josephson tunneling to compute time dependent Hamiltonians [3672].

China announced in 2018 a $145M plan to build a superconducting computer by 2022. They had then created a chip with 10,000 Josephson junctions. Not sure they are ready for this milestone. **Russia** also has ambitions in this field [3673].

In **France**, the laboratory CMNE (Micro Nano Electronic Components) of the IMEP-LaHC (Microelectronics, Electromagnetism, Photonics, Microwave) of the UGA (Grenoble) was working in this area, under the responsibility of Pascal Febvre who is based in Chambéry.

In **Korea**, researchers from Seoul National University have proposed another path, creating computers with CryoMOSFET chips operating at a relatively hot temperature of 77K, reducing cooling costs. Its benefits are less impressive than superconducting computing with an improvement of only 41% in single thread performance for the same power budget or a power reduction of 38% for the same performance, all this including of course the cooling power budget [3674].

One lone warrior in that space is **Quentin Herr**, a former engineer of Northrop Grumman who now works at IMEC in Florida. He and his wife Anna Herr and his team at IMEC are working on superconducting electronics in many areas [3675].

He is expecting superconducting HPCs to reduce power consumption by a factor of 100 compared to classical HPCs, refrigeration included [3676]. His team is working on improving superconducting components density with multilayers chips [3677], on creating Josephson based memories [3678, 3679], on synchronous and asynchronous data communication [3680, 3681] and on amplifiers [3682].

In the end, this branch of the superconducting computer industry is still immature for the moment. It has suffered from the uninterrupted advance of Moore's Law in the last few years and the difficulties of its practical implementation. The elementary components of these superconducting circuits are still bulky and not easy to miniaturize to create large scale circuits [3683]. It is not impossible that synergies will develop between quantum computing and this somewhat neglected branch. They can help each other, as can be seen with superconducting circuits for driving superconducting qubits or silicon. As we know, quantum computing will perhaps indirectly revive this sector.

There is a potential for a two-order-of-magnitude improvement in energy efficiency with superconducting supercomputers, cryogenics included. On top of the various variations of SFQ, RQL and SQUID superconducting circuits. One of the limitations of superconducting circuits is their low potential miniaturization. Josephson junctions density seems limited to 2.5 million junctions per cm^2. To be compared with billions of CMOS transistors at the 2 nm and 3 nm nodes [3684].

Not far from superconducting classical computing, a research team in China is developing memristors with magnetic topological insulators which could work as a cryogenic in-memory computing scheme based on the coexistence of a chiral edge state and a topological sur-

TABLE 2-2. SUPERCONDUCTOR RSFQ MICROPROCESSOR DESIGN PROJECTS					
Time Frame	Project	Target Clock	Target CPU Performance (peak)	Architecture	Design Status
1997-1999	SPELL processors for the HTMT petaflops system (US)	50-60 GHz	~250 GFLOPS/CPU (est.)	64-bit RISC with dual-level multithreading (~120 instructions)	Feasibility study with no practical design
2000-2002	8-bit FLUX-1 microprocessor prototype (US)	20 GHz	40 billion 8-bit integer operations per second	Ultrapipelined, multi-ALU, dual-operation synchronous long instruction word with bit-streaming (~ 25 instructions)	Designed, fabricated; operation not demonstrated
2002-2005	8-bit serial CORE1 microprocessor prototypes (Japan)	16-21 GHz local, 1 GHz system	250 million 8-bit integer operations per second	Non-pipelined, one serial 1-bit ALU, two 8-bit registers, very small memory (7 instructions)	Designed, fabricated, and demonstrated
2005-2015 (est.)	Vector processors for a petaflops system (Japan)	100 GHz	100 GFLOPS/CPU (target)	Traditional vector processor architecture	Proposal

Figure 497: Various superconducting electronic projects launched about 20 years ago with processors reminding us how long these projects can last or have their ups and downs. These projects became the C3 IARPA project that lasted until 2022. Source: [3667], pages 28 and 53.

face state. It would operate between 1K and 2K [3685]. Another potential use case would be the implementation of qubit drive and error correction at cryogenic temperatures.

Machine learning on superconducting logic is also explored, with an unusual algorithmic choice. Rather than porting neural networks, a Berkeley Lab team implemented in 2024 a **Tsetlin machine** in RSFQ. Tsetlin machines, named after Mikhail Tsetlin who defined learning automata in the 1960s, learn collections of propositional clauses built from finite state automata instead of floating-point weights. They are interpretable, work with bitwise operations only and converge faster than neural networks on some tasks, which makes them a natural match for logic-based superconducting circuits. Their Super-Tsetlin design learns the XOR task under high noise with only eight clauses, at an estimated dynamic dissipation below 0.5 mW and a 10 GHz clock [3686].

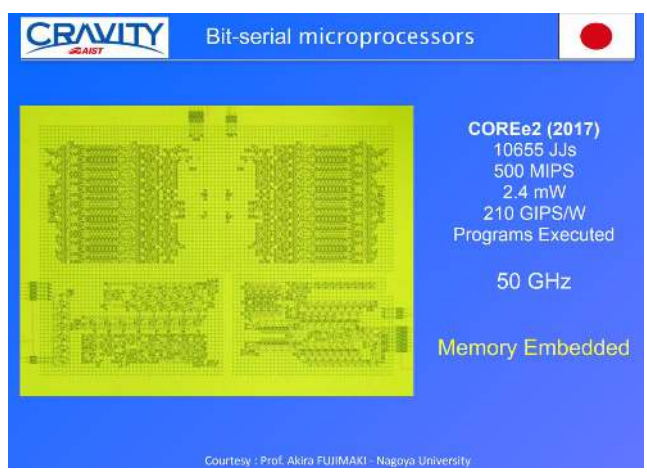


Figure 501: Small-scale 2017 prototype SFQ based superconducting microprocessor. Source: [3671].

PROCESS	Current density [kA/cm²]	minimum area [µm²]	Maximum integration	Maximum frequency [GHz]
Hypres #03-10-45	0.03 1.0 4.5	~ 3.14	15,000	80 GHz RnIc=1.3mV @ 4.5 kA/cm²
Hypres #S45/100/200	0.1 1 4.5 10 20 30	~ 0.4	10,000	200 GHz @ 30 kA/cm²
MIT Lincoln Lab SFQx	10 20 50	~ 0.06	~ 800,000	240 GHz RnIc=2.17 mV @50 kA/cm²
ADP2	10	1.0	1100 JJ/mm²	80 GHz
STP2	2.5 - 20	0.25 - 4.0	100 JJ/mm² - > 2,000 JJ/mm²	30 GHz - 150 GHz
HSTP	10	1.0	70,000	80 GHz
Fluxonics standard	1	12.5	100 JJ/mm²	40 GHz RnIc =0.256 mV
INRiM SNIS	up to 100	25	1,000 JJ/mm²	300 GHz RnIc =0.1mV - 0.7mV
NIST Nb/Nbx Si1-x/Nb	up to 110	?	70,000	300 GHz
INRiM SNIS 3D FIB	up to 100	0.1	10,000 JJ/mm²	300 GHz RnIc=0.1mV - 0.7mV

Figure 499: Comparison between different types of superconducting components. Source: [3671].

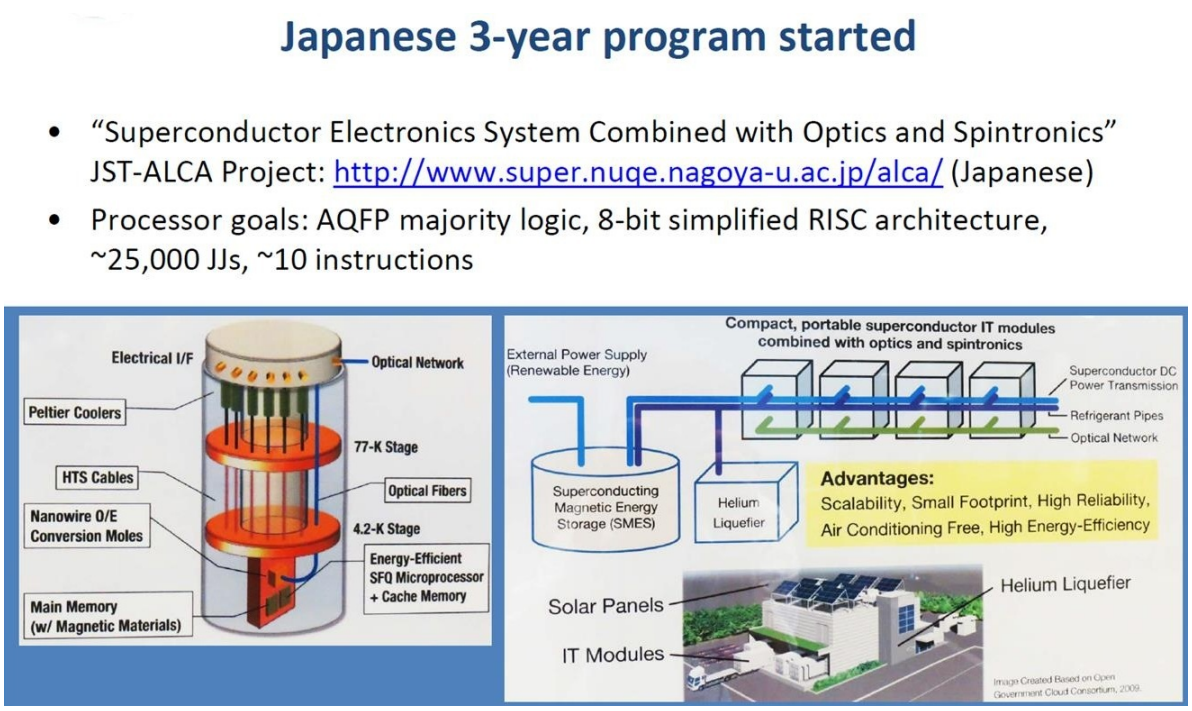


Figure 500: Japan past superconducting electronics plan. Source: [3670].

3.7.2 Vendors

Snowcap Compute

USA, 2024, $23M

Snowcap Compute is developing a superconducting based computing platform for AI and HPC that operates at 4.5K. The chips are manufactured on a 300 mm wafer process. The company was created by Anna and Quentin Herr, from IMEC.

3.8 Probabilistic computing

Probabilistic processors are another variation of exotic processors. They use probabilistic p-bits that can fluctuate rapidly between 0 and 1 with a low transition energy level. They are supposed to allow the resolution of so-called "quantum" problems without relying on quantum mechanisms. p-bits can be realized with nanomagnets [3687, 3688], with magnetic Tunnel Junctions (MTJs) which are spintronic devices that exhibit stochastic switching behavior due to thermal noise [3689], with regular transistors [3690–3694], with photonic devices

and Ising machines [3695–3697] and with the weird membrane computing field [3698].

Various applications are promoted such as the creation of neural networks called BSN (Binary Stochastic Neuron), restricted Boltzmann Machines (RBM) as studied at UCSB [3699, 3700] and the resolution of optimization problems like those treated by quantum annealing and gate-based quantum computing. The accelerations obtained are not qualified as exponential. It may be just polynomial, which is still interesting if the related time threshold is reasonable (at what computing time length is the approach faster than classical methods). Cryptanalysis applications are even investigated, like for solving the Closest Vector Problem, one of the lattice problems relevant to lattice-based cryptanalysis [3701].

Work in this direction is quite recent and comes from the **MIT**, **UCSB**, **Cornell University**, **Purdue University** in Indiana [3702, 3703] and from **Tohoku University** in Japan [3690, 3704]. The field got its own focus session at IEDM 2025, tellingly titled "From p-bits to Qubits". Kerem Camsari's UCSB group and Shunsuke Fukami's Tohoku group presented there, with TSMC, a fully digital p-bit that removes the digital-to-analog converters previously needed to set each p-bit's bias, the DACs being the bulky and power-hungry part that was blocking scaling [3705]. The same group then networked FPGAs into a single machine holding one million p-bits, performing Gibbs sampling at over a trillion flips per second while keeping every coupling weight in local on-chip memory and exchanging only 1-bit boundary states between devices [3706]. Their analysis identifies a single timing ratio, the boundary-exchange frequency over the local p-bit flip frequency, that determines whether a partitioned machine behaves like an unpartitioned one, which is a useful and rare piece of honest scaling theory in this domain.

One application worth watching is the sampling of neural quantum states. Combining sparse Boltzmann machine architectures with a multi-FPGA p-computer, a UCSB and Radboud University team obtained accurate ground state energies for the two-dimensional transverse-field Ising model at criticality on lattices up to 80×80, i.e. 6,400 spins, and introduced a dual-sampling algorithm to train deep Boltzmann machines by replacing intractable marginalization with conditional sampling over auxiliary layers [3707]. Here the p-computer is not competing with a quantum computer but accelerating the classical variational method that quantum computers must beat.

Hawai

France, 2020

HawAI.tech, a Grenoble-based startup, is positioned on the same niche and targets applications in the field of AI in embedded systems using data from various sensors [3708]. Hawai's roadmap was to lead to the creation of a complete probabilistic computer by 2024.

One original application of probabilistic computing is the simulation of quantum algorithms by mapping each qubit on 8 probabilistic bits, but it doesn't describe how it is handling entangled states [3709].

Extropic

USA, 2022, $14.1M

Extropic is a startup created by Guillaume Verdon (coming from Alphabet) and Trevor McCourt which wants to disrupt classical computing in AI to provide significant energy savings. They initially planned to leverage a thermodynamic process in classical superconducting chips using Josephson junction non linearities. They then pivoted to using probabilistic transistors using regular CMOS chips, implementing denoising and diffusion-like generative models at the device level. The proposed device could match GPU inference performance while using roughly 10,000× less energy in that benchmark regime. It has not yet been benchmarked at scale and is at best aimed at running some low-level primitives or LLM systems [3710].

They label their component a *thermodynamic sampling unit* (TSU), which uses the thermal fluctuations of ordinary subthreshold CMOS transistors to sample directly from programmable probability distributions. The XTR-0 development platform was released in late 2025 alongside thrml, an open-source Python and JAX library for hypergraphical models, with a production part named Z1 announced for later. In July 2026, the company signed a letter of intent with the US Department of Commerce for up to $75M through the CHIPS R&D office, to scale the TSUs and qualify a domestic foundry path, which is much larger than its $14.1M seed round. Extropic could equally have been placed in the thermodynamic computing subsection above, the boundary between p-bits and thermodynamic sampling being mostly a question of which physical noise source is exploited.

Quantum Dice

UK, 2020, $8.9M

Quantum Dice is a spinout from Oxford University's quantum optics laboratory which created a quan-tum entropy source. It was created by Ramy Shelbaya (CEO), Marko von der Leyen (CTO), and Zhanet Zaharieva (COO), initially for the development of some QRNG. In 2025, it pivoted with the development of p-bit computing. Their QRNG hardware became the basis of a probabilistic compu-ting platform, ORBIT, which powers the Lagrange 0 system, using p-bits that fluctuate between logical states with controllable probability, enabling the fast execution of probabilistic algorithms for complex optimisation problems. The QRNG photonic feeds quantum randomness into the p-bit system [3711]. The architecture currently runs on FPGA, with a roadmap toward ASIC. The current prototype implements and manipulates 64,000 logical p-bits. p-bits are suited for probabilistic and combinatorial algorithms

like Boltzmann machines, probabilistic graphical models, spin-glass models and cryptanalysis [3712], Markov Chain Monte Car-lo, Bayesian models, and combinatorial optimisations. These span portfolio optimisation, electrical grid optimisation, and supply chain logistics.

3.9 Optical computing

Optical computing is not a new idea and its recurring failure modes were already well diagnosed forty years ago. In a 1986 issue of Optics News, H. John Caulfield laid out the hard questions the field kept avoiding, essentially whether optics could ever beat electronics on anything other than a narrow set of linear operations [3713], while Demetri Psaltis asked in the same issue whether optical computing was revolutionary or merely evolutionary [3714]. Both concluded that the useful role of optics was as a specialized coprocessor for interconnect-heavy and transform-heavy tasks, not as a general-purpose replacement for digital electronics. That is almost exactly the position the surviving startups have converged back to, after a detour through more grandiose claims.

Many research laboratories and startups are working on the creation of analog optical processors that are not based on photon qubits [3715]. Some are creating classical optical neural networks, others are adapted to convolutional neural networks or spiking neurons, the latter being closest to the way the human brain works [3716, 3717].

Others are even proposing to handle vector/matrix manipulation, and heuristically attack NP-complete problems reformulated as Ising models, beyond the coherent Ising model machines I briefly discussed in the part dedicated to photon qubits. The potential advantages of these solutions are computing speed and power efficiency.

Further upstream sits lightwave electronics, which drives the electronic response of a solid with the carrier oscillations of an ultrashort pulse rather than with a voltage. Transistor switching cannot exceed about 800 GHz because it is limited by charge-carrier transit times, but driving valley pseudospin in a two-dimensional material is limited only by the optical cycle. A team led by Giulio Cerullo at Politecnico di Milano used in 2026 a sequence of phase-locked few-optical-cycle visible pulses to excite and switch the valley pseudospin in a WS_2 monolayer, timing the carrier oscillations with sub-femtosecond precision. They demonstrated logic operations above 10 THz [3718]. This was presented as light-based computing running at 10,000 GHz and being a thousand times faster than today's processors, which associates a coherent two-state switching rate measured on a single monolayer with a processor clock. But a switching event is not an instruction, and no memory, interconnect or readout operates anywhere near that rate. The interest is real but the technology horizon is quite remote.

Here is an approximate segmentation of this diverse field [3719].

Diffractive optical architectures

These are using SLMs and Fourier lenses systems. They are used to program linear operations and summation by collecting light power encoded signal. They are sending an image generated with a DMD, DLP or SLM chip illuminated by a laser and sent on various structures such as random matrices or various metamaterials. They are often based on the principle of the Optical Fourier Transform which decomposes a 2D image into spatial frequencies, themselves represented in 2D. This transform is an image that contains key points representing shapes and repetitions in the analyzed images. This can be leveraged to build convolution layers in convolutional neural networks. These serve to detect the presence of shapes in an image, the shapes being represented by filters. The Fourier transform helps to automatically identify these key shapes in the image. These systems capture the result with a CMOS sensor, usually with a very high resolution, much higher than that of the DLP or DMD chip used upstream. The Fourier plane is an optical spatial-frequency representation of the input. The camera samples it at a higher resolution than the modulator, which increases the number of measured samples rather than the intrinsic dimensionality of the represented signal. All this is supported by serious mathematics [3720, 3721]. It can also support generative models [3722].

Cascaded metasurfaces are progressively replacing bulk SLMs in these architectures. A 2026 design interleaves TiO_2 nanoblocks of distinct geometries inside each optical neuron, exploiting the Pancharatnam-Berry phase to obtain independent and parallel phase modulation at the three RGB wavelengths, which allows one forward pass to return both the object category and its color [3723]. Wavelength thus becomes a free multiplexing dimension, at the cost of a fixed, non-reprogrammable network once the metasurface is etched. By the way, metasurface research can also potentially cross-pollinate to light-forming devices supporting a large number of cold atoms.

The most ambitious diffractive result to date came in December 2025 from Chen Yitong's team at **Shanghai Jiao Tong University** with **Tsinghua University**. Their LightGen chip integrates more than two million photonic neurons and runs a complete generative pipeline optically: a photonic encoder made of integrated diffractive metasurfaces occupying under 35 mm^2 extracts low-dimensional features, an optical latent space is held in a single-mode fiber array encoding both amplitude and phase, and a photonic generator produces the output. It handles 512×512 image generation, NeRF-style 3D generation, video and semantic manipulation, and is trained with an algorithm that does not require ground truth [3724]. The team reported two orders of magnitude gains in compute density and en-

ergy efficiency over an Nvidia A100. The comparison was against a 2020 GPU on a task the chip is physically specialized for, and the input and output devices, SLMs and cameras, are not counted in the optical path even though they set the real throughput ceiling. The theoretical 5.69×10^9 TOPS figure circulating in the coverage assumes next-generation modulators that do not exist yet.

These different solutions could accelerate the training of some complex neural networks but are quite immature. These accelerations seem to be rather polynomial and not exponential as quantum computing is supposed to generate. And they need specific training methods [3725].

Optalysys

UK, 2013, $5.2M

Optalysys is a spin-out of the University of Cambridge created by Nick New, Robert Todd and Ananta Palani. Their FT:X 2000 system is structured around the realization of optical fast Fourier transforms based on diffraction [3726] (Figure 502 and Figure 503).

They were involved in various projects, one in genetics to do genome sequence alignment, GENESYS, carried out with the **Earlham Institute**. The other project dealt with weather forecasting for the European center ECMWF and a third one for plasma and fluid dynamics simulation, for DARPA. They also did run a convolutional network in 2018 on a MNIST base with 60,000 letters for training and 10,000 for testing. Its classification accuracy was only 70%.

On-chip optical circuits

It can rely on wavelength multiplexing or beamsplitter meshes implemented in nanophotonic circuits [3727–3729]. These systems usually support linear and sometimes non linear matrix operations that are useful in deep learning applications like image recognition. One goal usually put forward is to save energy vs GPUs.

Various academic projects have been launched in this domain, like in Russia [3725].

Another Russian proposal, from MIPT and the Dukhov Research Institute, implements matrix-vector multiplication with a set of ring resonators coupled to a waveguide through Brillouin interaction between photons and phonons. The input vector is carried by the occupancies of the anti-Stokes optical modes pumped by spontaneous Brillouin scattering on thermal phonons, and the matrix is set by the scattering rates and the resonator-waveguide coupling constants, which allows parallel computation across a frequency band [3730]. Relying on thermal phonons makes the scheme elegantly passive but also caps its dynamic range.

A collaborative effort in photonic chips development is run by the **PhotonDelta Foundation** (the Netherlands, €1.1B including €470M from the Dutch government), a public and private European Integrated Photonics Ecosystem fund that supports photonic chip ventures, in collaboration with the MIT. They invested in 177 projects. The program launched in 2022 is supposed to last 6 years. IMEC, LioniX and Bright Photonics are among the industry partners of this fund which gathers 26 companies, 11 technology partners and 12 R&D partners.

Copac

EU

The **Copac** project funded as part of a H2020 project is creating an optical processor that could evaluate all the variables of a logical function in parallel.

It is based on a quantum-dot-based architecture that can be excited simultaneously on several frequencies by wideband lasers. The results are read by 2D spectroscopy of quantum dots. The machine would operate at room temperature. The process mixes classical computation (for the evaluation of functions) and quantum methods (to do it simultaneously on several sets of variables) (Figure 504).

The project is conducted with the Universities of Liège (Françoise Remacle), Hebrew University of Jerusalem (Raphael Levine), University of Padua, the CNR Institute for Physical and Chemical Processes of Bari, the company **KiloLambda** (2001, Israel) which manufactures the quantum dots and **ProBayes** (France), a subsidiary of La Poste which produces the compiler of the solution (Emmanuel Mazer and David Herrera-Marti, who now works at CEA-LIST) [3731]. The European project was funded until 2021 [3732].

The great uncertainty in this project, as is often the case, concerns its scalability. It depends on the superposition of optical frequencies. The project documentation does not describe well the application domains of the possible in terms of complexity classes of addressable problems.

Arago

France, 2024, 22.1M€

Arago is a Paris-based startup created by Nicolas Muller (CEO), Eliott Sarrey (CTO) and Ambroise Müller (CSO), the last two having met at ETH Zurich working on silicon photonics and AI algorithms. Their accelerator, codenamed JEF, combines analog and digital electronics, silicon photonics and free-space optics in what they call a multi-physics computing core. The optical part handles the cubic complexity tensor operations while a digital processor takes the quadratic complexity pointwise operations. They target a 10× to 30× energy reduction versus current GPUs at equivalent performance, in standard form factors and on conventional manufacturing processes. Their software stack, CARLOTA, exposes a PyTorch-compatible interface so that existing models run without code changes, which is the pragmatic lesson learned from a decade of optical

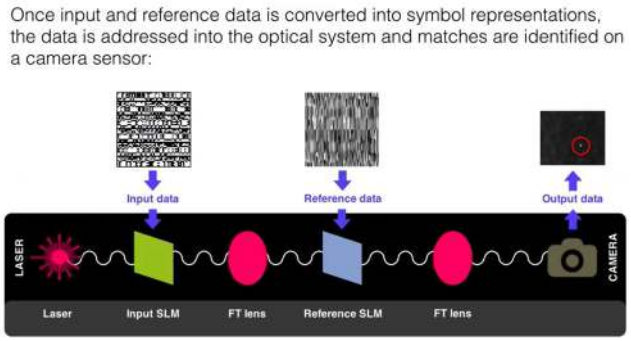


Figure 502: Optalysys process.

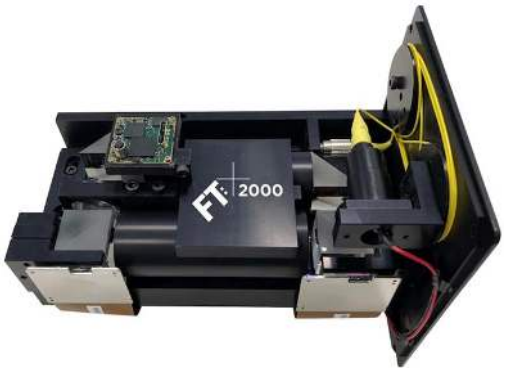


Figure 503: Optalysys apparatus. Source: Optalysys.

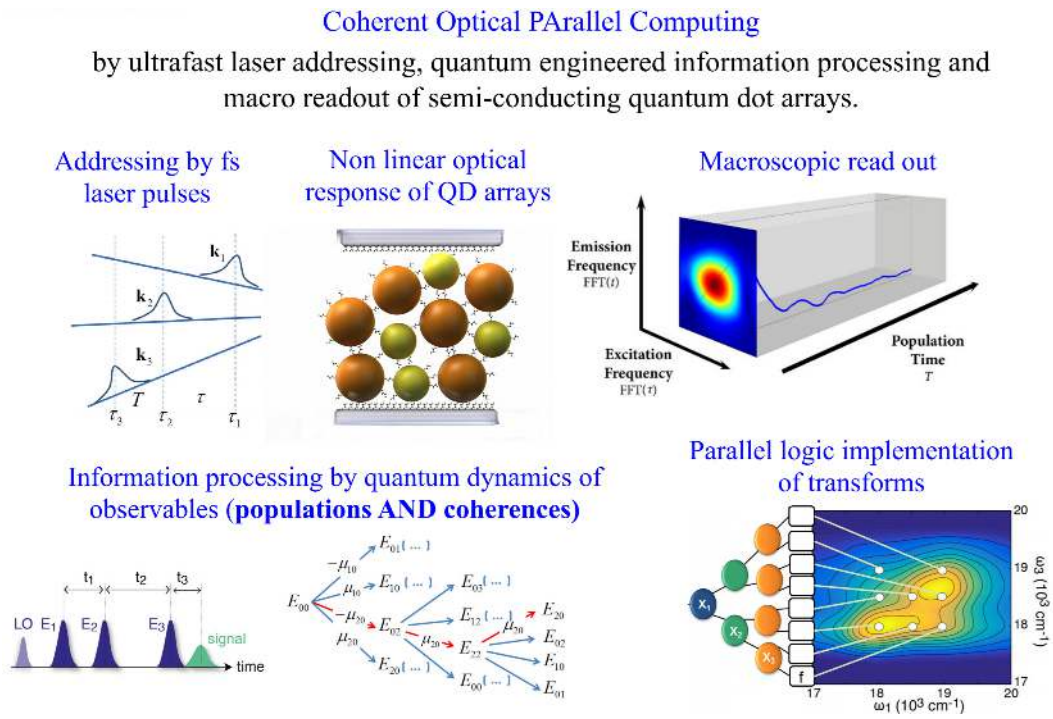


Figure 504: The optical technology behind the European Copac project.

computing startups that asked the ecosystem to adapt to them.

Neurophos

USA, 2020, $118M

Neurophos is an Austin-based startup spun out of Duke University and Metacept, an incubator run by David R. Smith, whose metamaterials work produced the microwave invisibility cloak experiments of the mid-2000s. It was cofounded by Patrick Bowen (CEO) and Andrew Traverso. Their claim rests on metasurface modulators about 10,000 times smaller than the modulators available from silicon photonics foundries, which lets them pack over a million optical processing elements on a single die and build a 1,000×1,000 optical tensor core, against the 256×256 matrices typical of AI GPUs. Since the computation happens as light crosses the metamaterial, the core is fully in-memory and the von Neumann bottleneck disappears for that operation.

Their announced Tulkas T100 OPU (optical processing unit) targets 470 petaOPS in FP4 and INT4 at 1 to 2 kW, with a 56 GHz clock and 768 GB of HBM memory in a dual reticle package, which they present as ten times the FP4 throughput of an Nvidia Vera Rubin NVL72 at comparable power. The T100 is not shipping before 2028, and the figures are design targets rather than measurements, only the matrix multiplication is optical while everything else stays electronic, and sustaining a 56 GHz core requires feeding it from SRAM and vector units at a rate that is itself an unsolved engineering problem. Optical cores also only consume energy for input and output, which means the efficiency argument improves quadratically with array size but says nothing about the conversion overhead that dominates at small batch sizes.

Lightelligence

USA, 2017, $36M

Lightelligence develops PACE, another photonic processor that is supposed to be 100 times faster than a Nvidia RTX 3080 GPU. It is designed to solve Ising models problems like D-Wave quantum annealers and Fujitsu digital CMOS-based annealers.

Their chip uses 12,000 thermal phase shifters and Mach-Zehnder interferometers (MZI) and runs at 1 GHz [3733, 3734]. It seems the system can parametrize an Ising model only with coupling graph nodes with the equivalent of a longitudinal field, but not by setting longitudinal interactions at the graph node level like with D-Wave quantum annealers. It implements parallel photonic recurrent network with the photonic part performing a unitary matrix product of a state-preparation rotation matrix R, the desired unitary (U or $U^\dagger$), and one of two homodyne detection matrices (h1 or h2). Phase-intensity reconstruction, a diagonal matrix multiplication, Gaussian noise addition, and a nonlinear threshold unit are performed classically. Now, how does it scale is yet to be shown.

Linque

Germany, 2024

Linque is a startup created by Samarth Vadia, Jonathan Förste and Victor Funk that develops a light-based processor using a photonic chip manufactured using CMOS-compatible processes. It supports matrix multiplications, convolutions, and signal transformation and can solve optimization problems and differential equations.

Q.ANT

Germany, 2018, €62M

Q.ANT is a photonic subsidiary of the TRUMPF group, also known for its power lasers that are used by ASML EUV systems. It develops an energy-efficient multiple-wavelengths photonic processors for AI and high-performance computing on thin-film lithium niobate. It computes the solution of complex and nonlinear mathematical equations. They claim to enable up to 30× energy efficiency and 50× performance gains over GPUs. It fits into a 4U rack and consumes only 45W. It is provided with a toolkit supporting Python and C++. Now, we need some benchmarks and actual case studies!

Salience Labs

UK, 2021, $11.5M

Salience Labs is a startup cofounded by Vaysh Kewada (CEO) and Johannes Feldmann (CTO) and spun out of Oxford and the University of Münster in Germany.

It develops a hybrid photonic-electronic silicon chip dedicated to AI applications. Other research participants are the Universities of Pittsburgh (USA) and Exeter (UK), EPFL and IBM Research Zurich. It implements fast tensor processing running at 100 GHz. It implements sort-of in-memory photonic computing implementing optical frequency combs coupled with a classical SRAM (Static Random Access Memory) [3735]. They could also use phase-change materials developed by Oxford University instead of SRAM. Oxford University researchers designed a light-based silicon photonic chip with hybridized-active-dielectric (HAD) nanowires enabling light polarization-selective tunability. They demonstrated the use of polarization as a parameter to selectively modulate the conductance of individual nanowires within a $Ge_2Sb_2Te_5$ (GST for germanium-antimony-tellurium, a phase changing material also used in RW optical discs and phase-change memories) and silicon multi-nanowire system [3736].

Laser networks

These are complex lasers (degenerate cavity lasers, multimode fiber amplifiers, large-aperture VCSELs) with many spatial degrees of freedom and controllable nonlinear interactions. These systems can be used for reservoir computing (RC) or for matrices computing (using for example SLMs, spatial light modulators, like the ones used in cold-atom quantum computing [3737]).

Akhetonics

Germany, 2021, €2.3M

Akhetonics is a startup created by Michael Kissner (CEO) that is designing an all-optical XPU, a cross-domain hybrid digital and analog optical processor for all-purpose, low power, high-performance computing and AI for edge operations. It targets an energy efficiency of 48 TOPS/s (INT8 bits)/W [3738].

LightSolver

Israel, 2020, €12.5M

LightSolver is a startup founded by Ruti Ben Shlomi (CEO) and Chene Tradonsky (CTO) from the Weizmann Institute that develops a quantum-inspired computing solution named LPU100 using optically coupled lasers and handling 100 continuous variables.

It solves Max-2-SAT and 3-Regular 3-XORSAT combinational optimization problems. Their target markets are finance, manufacturing and logistics. In 2024, the company got a funding of €12.5M from the EIC Accelerator Program (€2.5M in grant and €10M future equity investment).

Q/C Technologies

USA, 2025

Q/C Technologies, formerly TNF Pharmaceuticals, holds exclusive rights to LightSolver's LPU technology for the crypto and blockchain domain. It rebrands the hardware as the qc-LPU100 and markets it as "*quantum-class computing at the speed of light*", given since nothing

in the LPU is quantum. It is a network of coupled lasers solving Ising problems classically. The public claims are up to 100× the speed of state-of-the-art GPUs at a hundredth of the energy, and the roadmap given for the underlying LightSolver platform is 100,000 variables by 2027 and one million by 2029, against the 100 continuous variables of the current LPU100, which is a four order of magnitude jump in four years. The company announced a separate silicon photonic OPU initiative for AI inference in March 2026.

Luminous Computing

USA, 2018, $115M

Luminous Computing aims to create a high-performance optical component that would replace 3000 Google TPUs! It would exploit multicolor lasers and light guides. According to the publications of their CTO, Mitchell Nahmias, it seems that they use optical spike neurons [3739]. They can perform calculations very quickly, including in classical CMOS.

Neural network optical circuits

It can use wave mixers as shown in Figure 505. These optical neural networks can implement inferences as well as backpropagation training tasks depending on their architecture [3740]. In the case of large models, it could bring some significant energetic advantage compared to classical CMOS based inferences [3741–3744].

Optical parametric oscillators

These OPOs can be used to solve Ising models, like with the DOPO-based simulator and coherent Ising machines (CIM) (Figure 506) [3746, 3747].

A conceptually different encoding was demonstrated in January 2026 by Liam Quinn, Stéphane Coen, Miro Erkintalo, Stuart Murdoch and Yiqing Xu at the University of Auckland and the Dodd-Walls Centre, with the Université de Bourgogne and Strathclyde. Conventional CIMs encode spins in the phases of the oscillators, which forces phase-sensitive readout and elaborate phase stabilization. Their machine instead encodes spins in the polarization state through spontaneous polarization symmetry breaking in a coherently driven fiber Kerr resonator, so that the network state is read with plain intensity measurements using off-the-shelf telecom components. Operating in a regime where nonlinearity and topology lock the system's symmetry removes drift and bias, and they ran uninterrupted Ising trials at optical speeds for over an hour without manual intervention [3748]. Continuous unattended operation has been a real obstacle for this family of machines, so this matters more than the problem sizes reached so far.

Orbital Angular Momentum Photonic computing

It is mainly proposed for information storage [3750].

Reservoir computing

It is a specific category of recurrent neural networks used to process time series (in language processing, finance, energy, robotics). The concept was created in 2007 [3751–3755]. Their particularity is to use neuron weights and links between neurons randomly fixed in the reservoirs, all with nonlinear activation functions for these links. The hundreds of neurons in a reservoir are fed by data stored in the reservoirs. The activation functions nonlinearity makes this memory evanescent.

The training parameters of these networks are in the weights of the neurons that connect the reservoirs to the output data. Reservoir computing can be implemented with photonics as shown in Figure 507.

There are other implementations with memristors [3756], five types of optical reservoir computing and even quantum versions, for quantum reservoir computing [3757–3762].

3.10 Chemical computing

Chemical computing is yet another form of unconventional computing. The underlying physical phenomenon was discovered in 1951 by a Soviet chemist, Boris Belousov, with an oscillating chemical reaction alternating the color of a solution mixing salts and acids, then extended in the early 1960s by Anatol Zhabotinsky, hence the name Belousov-Zhabotinsky reaction. It would enable the creation of chemical logic gates. It was thought initially that it broke the second law of thermodynamics (a bit like time crystals…). It was found later that it was not the case and that some form of logic gate could be implemented using this phenomenon and a chemical oscillator that is akin to chemical concentration waves blocking or amplifying each other depending on their setting. One benefit is a low energy consumption [3764].

Research in the domain started to generate some experimental results in 1989 and onwards, particularly in the UK, at EMPA in Switzerland, Stanford, Harvard and the University of Washington. But the benefits of this architecture are not obvious, mainly due to its relatively slow speed.

The most recent work came in 2020 from the University of Glasgow that used 3D-printed programmable chemical processor with a 5 by 5 array of cells filled with a switchable oscillating chemical and magnetic stirrers to control their oscillations and compute binary logic gates to perform pattern recognition [3765]. The array has a configuration space of 2.9×10^{17} states, which is the size of the space rather than the number of states actually explored during a computation. The array is programmed by setting chemical relations between these chemical cells. It can implement a chemical autoencoder used for pattern recognition. Now, more comparisons must be made with classical computing to see how it scales [3766]!

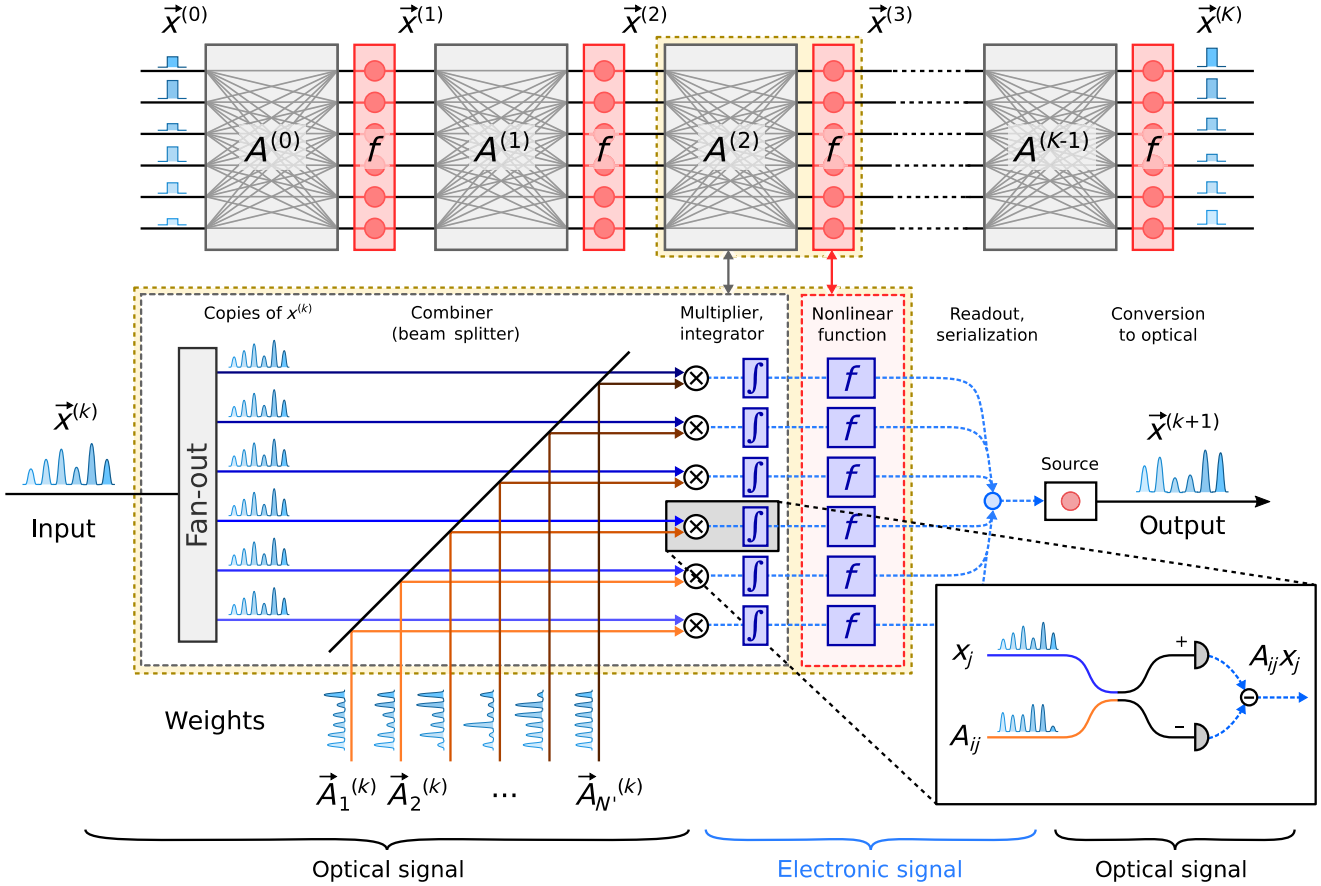


Figure 505: Source: [3745]. Added in 2023.

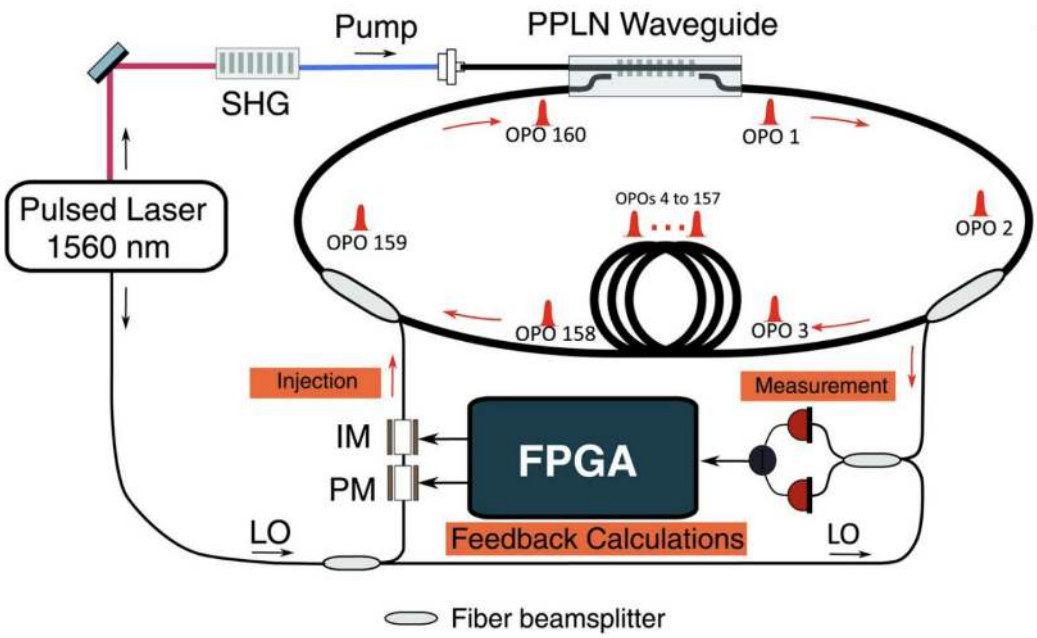


Figure 506: An OPO based optical computing system. Source: [3749]. Added in 2023.

You can include in that category all the work around DNA computing and DNA-based storage [3767, 3768]. These are quite far-fetched even in the classical world. Some researchers (in Mexico) think that such DNA computers could behave like quantum computers and bring some exponential speedups, thanks to A-T and C-G-base pairs manifold encoding [2978]. Of course, these claims are not yet tested practically.

A more recent angle treats chemistry as a reservoir rather than as a logic substrate. Connah Johnson and

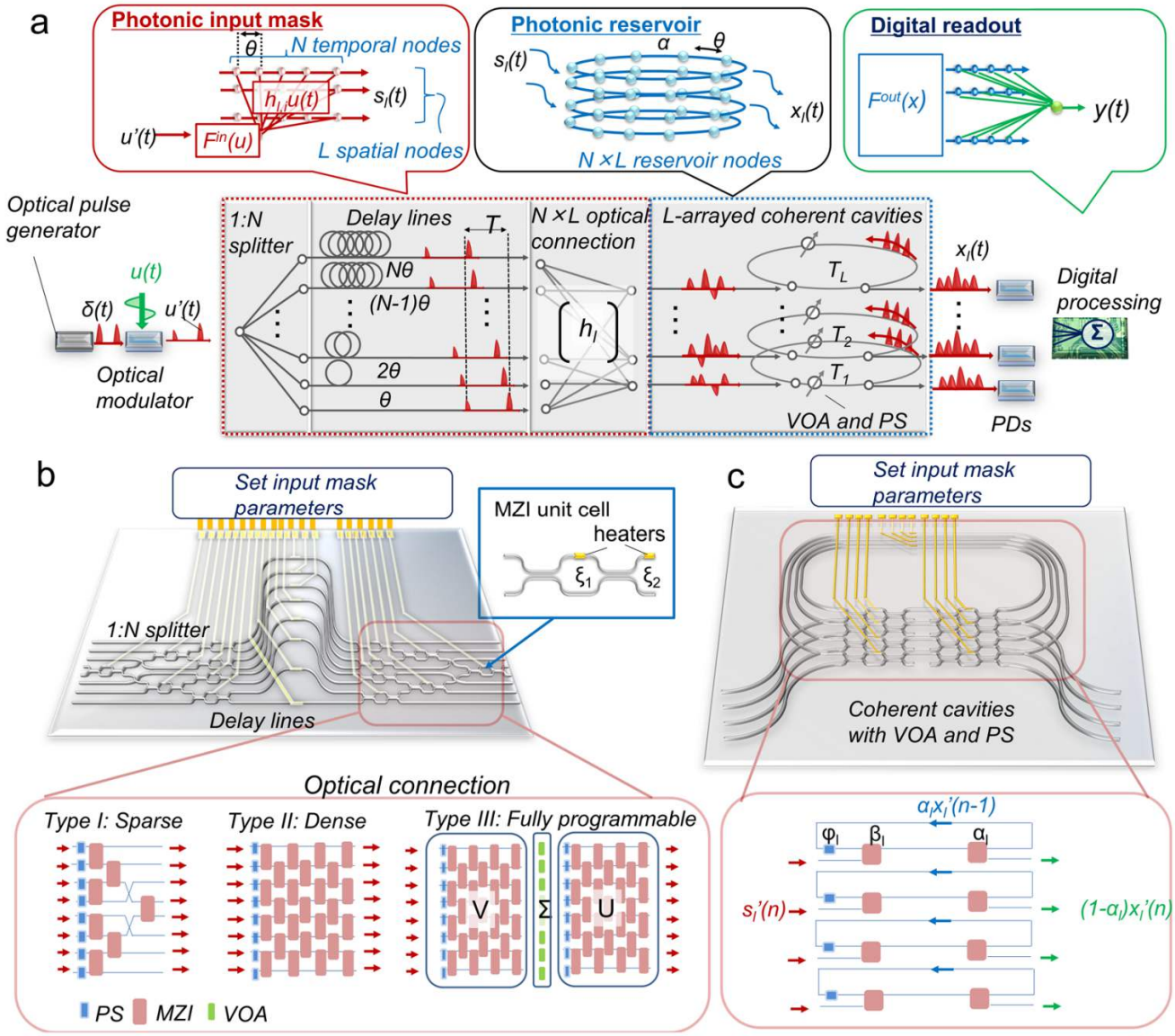


Figure 507: Source: [3763]. Added in 2023.

colleagues at Pacific Northwest National Laboratory propose using the dynamics of chemical reaction networks as the reservoir of a reservoir computing scheme, where the nonlinear transient dynamics of coupled reactions perform the high-dimensional projection and only the readout weights are trained [3769]. Again, the motivation is energy efficiency related rather than about speed. Indeed, the millisecond to second timescales of the underlying chemistry is quite large. This connects with the reservoir computing paragraph in the optical computing subsection above, the reservoir concept being substrate-agnostic by construction.

Other proposals abound for the development of synthetic biology intelligence, like what **Cortica Labs** is doing [3770].

Finally, the **Chemputer** from Leroy Cronin is not for doing actual computing per se, but for synthesizing molecules from a digital description. It is an experimentally demonstrated automated synthesis platform, with published syntheses executed from chemical code, rather than a theoretical concept. Its generality across arbitrary molecules remains the open question [3771].

3.11 Unconventional data storage

Storage belongs to this part since existing technologies are hitting physical limits and the alternatives are justified almost entirely by energy and durability rather than by speed. Magnetic tape lasts about 30 years and requires periodic migration, which for archival data means paying to copy the same bits forever. Both credible alternatives are zero-power at rest.

Atlas Data Storage (2025, USA, $155M) was spun out of Twist Bioscience in May 2025 with the acquisition of its DNA data storage assets, and is led by Varun Mehta (CEO), founder of Nimble Storage, with Twist cofounder Bill Banyai as CTO and George Kadifa. The technology combines semiconductor chips for massively

parallel on-chip chemistry with enzyme engineering for synthesis. Their announced Eon 100 claims 60 petabytes in 60 cubic inches, about a thousand times the volumetric density of LTO-10 tape, with a stated durability beyond a thousand years and cheap replication since copying DNA is what polymerases do. They partnered with IMEC in March 2026 to scale the write process. Write throughput and write cost remain the unsolved problems for all DNA storage ventures, synthesis being orders of magnitude slower and more expensive per bit than any electronic alternative.

Microsoft Research reached a more complete milestone with Project Silica, an effort started with the University of Southampton after their 2013 demonstration of femtosecond laser writing in glass. Their 2026 Nature paper reports the first end-to-end system, covering writing, storage and retrieval rather than optimizing density alone: 1.59 Gbit/mm^3 over 301 layers, for 4.8 TB in a 120 mm square of fused silica 2 mm thick, with a claimed data integrity beyond 10,000 years at room temperature [3772]. The commercially significant part is the extension to ordinary borosilicate glass, which reaches a lower 0.678 Gbit/mm^3 over 258 layers, or 2.02 TB per platter, using phase voxels based on isotropic refractive index changes instead of the birefringent voxels used in fused silica. Data is encoded as voxels, three-dimensional modifications of the glass, and read back with polarization or phase sensitive microscopy and machine learning decoding. Write throughput is 25.6 Mbit/s per beam at 10.1 nJ per bit, so over 150 hours to fill one fused silica platter, which is the real constraint and confines the technology to write-once, read-rarely archives. Since reading uses light too weak to alter the medium, the air gap is physical rather than administrative, which is an underrated security property. Microsoft announced the research phase complete in 2026. The remaining barrier is economic and specific. Femtosecond lasers are expensive, and without a mass-market application driving their cost down there is limited room for the price reductions commercialization would require.

3.12 Quantum unconventional computing key takeaways

- Various non-conventional computing technologies may compete with classical and quantum computing or provide useful enabling capabilities. Many of them are now positioned as enabling a reduction of the energy consumption for AI-related tasks. Reversible and superconducting technologies, for example, may help create cryogenic electronics for scalable quantum computers. Because these approaches rely on very different physical principles, they require careful evaluation and benchmarking by both physicists and computer scientists. None has demonstrated a scalable polynomial-time solution to generic NP-complete problems or a broadly applicable advantage over the best classical baselines. We also cover in this part the realm of classical supercomputing, which provides some comparable on system size and capabilities.
- Digital annealing computing is mostly proposed by Japanese companies like Fujitsu and Hitachi, using classical CMOS chipsets. These solutions are supposed to solve intractable problems faster than classical computers, but their scalability remains questionable according to existing benchmarks. Their commercial traction seems to be limited to the Japanese market.
- Reversible and adiabatic computation have been researched for a long time and has not yet developed into broadly deployed commercial computing products. It may be more useful for reducing energy dissipation than for increasing computational speed, with potential applications in quantum-computing enabling technologies as well as in artificial intelligence application inferences.
- Superconducting computing is an interesting area of research to create more energy efficient supercomputers, despite the cooling cost that, fortunately, is not as expensive as with superconducting qubits quantum computers. There are synergies between this research area and superconducting logic electronics that could be used to control superconducting and quantum dots spin qubits at low temperatures.
- Probabilistic computing is an interesting research area. These solutions may be competitive for solving specific combinatorial and decision problems.
- Optical processors are mainly investigated in the deep-learning space to accelerate training and inference for selected neural-network operations. Some variants target combinatorial optimization problems, where fault-tolerant quantum computers may also face substantial resource requirements. This is a dynamic sector with several well-funded startups.
- Chemical computing is one of the many other areas in unconventional computing that may be interesting but have probably various scaling limitations. Other unconventional computing such as DNA computing and other variations are not studied here, particularly since they are not deemed to solve intractable problems.

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This **Unconventional computing** section contains 244 bibliographical references and notes containing at least 5,188 pages.

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⟨ 137 | 1WQC | 3D NAND | 2DEG | Abelian | ABRC | Active space | Active Volume | ADAPT-VQE | Adaptive quantum circuits | ADC | AC Stark shift | Adiabatic | Adiabatic theorem | ADR | Advantage | aka | AKLT state | Algorithm | Algorithmic qubit | Amdahl's law | AFC | Amplitude | Amplitude amplification | Anharmonic oscillator | Angular momentum | Anomalous heating | Ansatz | Antibunching | Anyon | arXiv | Antisymmetry | AOD | Approximate Amplitude Encoding | Artificial atoms | ASIC | Assumptions | Atoms | Auger effect | Autonomous quantum error correction | AWG | Axion | BB84 | Back action | Backside power delivery | Balmer series | Band gap | Balanced beam splitter | Barren plateaus | Baryon | Base temperature | BCS theory | Beam splitter | Bell inequalities | Bell states | Bell test statistic | Bernstein-Vazirani | Basis encoding | Betti number | Bichromatic field | Bright/dark fluorescence readout | Bias-preserving gate | Biphoton | Black body | Blind Quantum Computing | Angle encoding | Amplitude encoding | Bloch states | Bloch sphere | Brightness | Bucket brigade | Block-encoding | Bond dimension | Born rule | Born-Oppenheimer approximation | Bose-Einstein Condensate | Bose-Hubbard model | Boson sampling | Boson | Bosonic codes | BQP | Bra-ket | Brane | Bravais lattice | Break-even | Brillouin scattering | BSM | cADR | Cap table | Capex | Carleman linearization | Carnot efficiency | Casimir effect | Cavity | Cavity quantum electrodynamics | CFD | CFET | Chandelier | Chern number | Chi | Chip | Chipset | Chiplet | CHSH inequality | CIM | Circuit quantum electrodynamics | Circuit synthesis | Classical shadows | Clifford group | Circulators | Circuit | Clock qubit | Cluster state | CLOPS | CMOS | CNOT | Coarse graining | Coaxmon | Code distance | Coherence | Coherence fraction | Coherence length | Cold atoms | Cold plate | Cold trap | Compatible properties | Commutativity | Commutator or commutation operator | Complementarity | Complementary variables | Complex number | Complexity | Compton effect | Computational basis | Concatenated codes | Condensed matter physics | Conjugate variables | Concurrence | Consistent histories | Constructor theory | Contextuality | Continuous variables quantum computing | Cooper pair | COP | Copenhagen interpretation | Coplanar waveguide (CPW) | CPLEX | Cryo-CMOS | Correspondence principle | Coulomb blockade | Coulomb force | Counterfactuals | Counterfactual models | CPTP map | Crosstalk | Cryocooler | Cryogenics | Cryopumping | Cryostat | CSCO | CSM | Butterfly velocity | Cuprate | CV-QKD | CVaR | CVD | DAC | DAQC | Data re-uploading | Dark count | Dark energy | Dark matter | Dark silicon | Dark state | Dark state protocols | DCE | DCQO | DDS | DQC | De Broglie wavelength | Decoherence | Degenerate | Delayed-choice experiment | Dennard scaling | Density matrix | Dequantization | Determinism | Deutsch-Jozsa | DFT | Dimon | DI-QKD | Dicke state | $k = 0$: | $k = 1$: | $k = 2$: | $k = 3$: | $k = 4$: | Diffraction | Dilution refrigerator | Dirac's notation | Dirac constant | Discrete log problem | Dissipation engineering | Distillation | DLA | DMRG | Domain specific architecture | Doppler cooling | Doppler effect | DV-QKD | D-Wave | DQI | DRAG | DRAM | Dressed state | Dual-rail encoding | Dual-species | E91 | EBL | EDSR | Eigenstate | Eigenvalue | Eigenvector | Einselection | Electromagnetic spectrum | EIT | Electron | Electron gas | Elliptic Curves Cryptography | Energetics of quantum technology | Engineering | Entanglement | Entropy | EPLG | EPDA | Epistemology | EPR paradox | EQA | Erasure error | ERC Grants | Ergodicity | Ergotropy | Error Correction Codes | Errors | ESR | Eta letter | EUV | Exchange-only qubit | Exciton | Exclusion principle | Expectation value | Euclidean networks | Extended Church-Turing thesis | Fabry-Pérot cavities | FBQC | FD-SOI | Feedforward | Fermi's golden rule | Fermi sea | Fermi-Hubbard model | Fermions | Fine structure | FinFET | First quantization | First quantum revolution | Floquet code | Fine-structure constant | FOFI | Fluxonium | Flying qubits | Fock space | Fock state | Flux biasing | Foliation | Fourier Transform | EPDA | Fredkin gate | Free Electron Laser (FEL) | FTQC | GAA | GAN | GAS | Gatemon | Gate-based quantum computing | Gate teleportation | Gaussian Boson Sampling (GBS) | Gaussian state | GBS | GGSA | GHS | GHZ | Gibbs state | Gifford-McMahon | Ginzburg-Landau theory | GKP qubits | Gleason's theorem | GPGPU | GQE | Graviton | Green's function | Grotrian diagram | Ground state | Grover | GSA | Gurobi | H-bar | Hadamard | Hafnian | Hall effect | Hamiltonian | Hamiltonian simulation | Hamming distance | Harmonic oscillator | Hartree-Fock | HBM | Heisenberg | Heisenberg cut | Heisenberg | Helium 4 | HEMT | Hermitian matrix | Heterostructures | Heuristic algorithm | Heralded single-photons | Helicity | Heterodyne | Hilbert | Holevo bound | Hong-Ou-Mandel effect | Hidden variables | HOBO | Homodyne measurement | Hopfion | FPQC | HTS | model | HUBO | Hybrid bonding | Hyperentanglement | Hybrid quantum algorithm | Hyperfine structure | Hyperf | Iceberg | IDR | computing | Indeterminacy principle | Indistinguishability | Indistinguishable photons | Integrated Quantum Phot | Interference | terposer | Int | ectivity | Invertible computation | Irreversible | Ion | Ion shuttling | Ion traps | IonQ | I/Q mixer | Ising | Isotop | Jaynes-Cum | gs Hamiltonian | ons paradox | JJ | Josephson | JPA | Kapitza resistance | Kerr effect | Ket | Klein-Gordon equation | Koche | ecker theorem | mey's law | Koo | n–von Neumann | Lamb shift | Lamb-Dicke regime | Landauer limit | Larmor frequency | Larmor precessio | aser | Lattice surg | LCHS | LCU | Le | e errors | Learning | Leggett-Garg inequality | Leggett inequalities | Kraus operators | Lie groups | Lindblad | ation | Linear algeb | Linear optics | Li | binson bound | Light cone | LNOI | Local Friendliness | Loophole-free Bell test | Lorentz factor | LPPT | | M-theory | Many | ds interpretation | LINSAT max-k-XORSAT | LLM | Locality | LOCC | Logical Qubit | Loophole | LRU | LSTM | MAGIC | c states distillatio | gic state cultivatio | Magneto-Optical Trap | Magnon | Majorana fermion | Manifold | Markovian process | Matchgate circuits | rix | Matter wa | UT | Maxwell's | on | MBE | MBQC | MCMC | MCMR | MDI-QKD | MegaQuop | Meissner effect | MERA | Mesoscopic | uristic al | layers | Meta | ce | Microring resonator | Mid-circuit measurement | MIS | Microwave-to-optical transduction | Mixing c | er | Moo | Moore | M | MZI | Mølmer-Sørensen gate | Motional mode | Micromotion | MNR | Mode-locked laser | Mott insul | Mott | tion | PO | MV | NLP | Mixed state | MNIST | Modality | Momentum | Multimode | Muonic atoms | Mutually unbiased ba | Na | et | ND | NEM | QC | SQ | No-go theorem | Non-Clifford gates | No-cloning theorem | No-signaling | Nonlinear optics | Nonlocality | kovian pr | s | MR | sical light | Non-demolition measurement | Non-selective measurement | NOON state | Noether's theorem | Normal | NP | NP | pace | NP | t | NQS | NV center | Observable | ODE | ODMR | OFHC | On-premise | Ontology | OPA | Opex | Operator norm | C | OTOC | cal mo | Optical pumping | Optical qubit | Optical tweezer | Oracle | Orbital angular momentum | Oscillator | Overhauser field | P | Pauli spin blockade | Pauli string | PBR theorem | PCA | PDE | PDK | Penning trap | PEPS | Permanent | Phase Estimation Algo | se classification | Phase kickback | Phase space | Phasor diagram | Phonon | Photoelectric effect | Photoionization | Photolithography | PIC | PIM | Photon | Photon measurement | Pilot wave | PKI | Planck constant | Planck length | Planck units | Plasmon | PMT | PNRD | Pockels effect | Poincaré sphere | Pointer states | Polarized Beam Splitter | Polaritons | Postselection | POVM | PQC | PQE | PQS | Prefactors | Prepare-and-measure | Private Key | Process Design Kit | Property | Psi-ontic and psi-epistemic | Public key | PUBO | PUE | Pulse tube | Purcell effect | Purcell filter | Pure state | Purification | PVD | PVM | Q factor | Q-Score | QAA | QAE | QAI | QACM | QAQM | QAOA | QAOA | QBER | QBism | QCCD | QCKA | QCaaS | QCNN | QCV | QFC | QET | QFHE | QFT | QGLM | QIP | QHO | QIR | QITE | QKD | QLBM | qLDPC | QLM | QLSA | QLSP | QMA | QML | QND | QNLP | QPE | QPINN | QPU | qRAM | QRC | QRNG | QROM | QSA | QSCI | QSP | QSDC | QSS | QST | QSVD | QROAM | QSVT | Quantics representation | Quantization | Quantronium | Quasi-locality | Quantum accelerator | Quadrature | Quantum advantage | Quantum algorithm | Quantum annealing | Quantum batteries | Quantum channel | Quantum Chaos | Quantum chromodynamics | Quantum circuit | Quantum cognition | Quantum computer | Quantum Conference Key Agreement | Quantum Darwinism | Quantum data center | Quantum dots | Quantum Electro-Dynamic | Pauli propagation | Quantum emulator | Quantum energetics | Quantum engineering | Quantum Field Theory | Quantum Fisher Information | Quantum foundations | Quantum gates | Quantum Hall effect | Quantum hydrodynamics | Quantum Internet | Quantum jump | Quantum kernel | Quantum capability learning | Quantum logic | Quantum matter | Quantum medicine | Quantum Non Demolition measurement | Quantum numbers | Quantum postulates | Quantum Physical Unclonable Functions | Quantum repeater | Quantum reservoir computing | Quantum reservoir engineering | Quantum resource estimator | Quantum simulator | Quantum speed limit | Quantum spin liquid | Quantum state | Quantum state tomography | Quantum Steering | Quantum supremacy | Quantum switch | Quantum teleportation | Quantum thermodynamics | Quantum transduction | Quantum trajectories | Quantum utili | | Quantum volume | Quantum walk | Quantum Zeno Effect | Quasiparticles | Qubit | Qubitization | QUBO | Qudits | Que | rt | Qu | Rabi | R | Raman cooling | Raman effect or Raman scattering | Raman spectroscopy | Ram | t | Rayleigh scattering | RBM | Ralph | Rebound effect | Reduced Planck constant | Reflectometry | Register | Relational quantum mechanics | Relaxation | ReLU | Renormalization | Renyi entropy | Repumping | Reticle limit | Retrodiction | Reversible computing | RIE | RSA | RUS | RSG | Rydberg state | Rydberg blockade | Sapphire | SAT | Scrambling | Scale-out | Scattering | Schrödinger | Schrödingerization | Schrödinger wave function collapse | SDP | LP | MIP | ILP | Second quantization | Second quantum revolution | SED | Semiclassical QFT | Semi-classical light | SFQ | Shelving | Shor | Shortcuts to Adiabaticity | Sideband | Silicon 28 | SIMD | Simon | Single mode | SKR | Singlet-triplet qubit | Sign problem | Sisyphus cooling | Skyrmion | SLM | SNAQ | SNSPD | SoC | SOI | SPAC | SPAD | SPAM | Spectral lines | Spectral decomposition | Spin | SpinBus | Spin-to-charge conversion | Spin-boson model | Spin glass | Spinor | Spintronics | Spontaneous emission | Spontaneous Four-Wave Mixing | Spontaneous Parametric Down-Conversion | SPOQC | Squeezed states of light | Squeezing | SQUID | SRAM | Stabilizer gates | Standard model | Standard quantum limit | Stark shift or Stark effect | State reduction | Retargetability | Strong simulation | State vector | Stationary qubits: stationary | Stern-Gerlach experiment | Still | Stimulated emission | String theory | Sturm–Liouville problem | Superabsorption | Superatom | Superconductivity | Superdense coding | Superdeterminism | Superfluidity | Supersonic propagation of correlations | Superoperator | Superposition | Superradiance | Superselection | Supersolid | Surface codes | Surface trap | SVD | SVM | SWAP | s-wave, p-wave and d-wave | SWSPD | SYK | Symmetry | Sympathetic cooling | Szilard engine | T gate | T-count | T-depth | Tachyon | Tau scaling law | TCI | TCO | TDA | TDP | Technology node | Tensor network | TF-QKD | TFLN | TES | THC | Theory of everything | TSP | T_1 | T_2 | Tabu search | TDSE | Tensor | TeraQuop | Thermodynamics first law | Thermodynamics second law | Time crystal | Time domain | Time reversal | Toffoli | Topological | Topological insulator | Time-bin entanglement | Tsirelson bound | Transmon | Transpiler | Transpilation | Transversal gates | Trapped ions | Trotterization | Trusted node | TSV | TTN | TTSB | Tunnel effect | Twistronics | Two-Level Systems | TWPA | Type I and type II superconductors | UCC | UHV | Ultraviolet catastrophe | Unary iteration | Unary gates | Uncompute trick | Unconventional Computing | Unitary operation | Universal quantum computer | Universal quantum gates | Unruh effect | Vacuum fluctuation | Vacuum polarization | Value migration | Variational

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