



# How to compare logical qubits?

One 2026 quantum prediction is that it will be the year when useful logical qubit based quantum computers will appear (dealt with prudently by **Riverlane** and **Innovation Origins**). In a sense, it would mark an irreversible transition from NISQ to FTQC.

Here, vendors face a complexity challenge not only to deliver what's in their roadmaps but also when communicating about it. There are many underlying concepts and figures of merit that deserve to be explained. All vendors logical qubit are not born equal and are also not necessarily yet useful. To be so, they should support larger (much) quantum circuits than current NISQ quantum computers who are currently limited to about a thousand operations, and 5 to 6 thousands when using quantum error mitigation techniques.

I am self-publishing here a paper designed to help you understand the field of quantum error correction, logical qubits, and fault-tolerance, from the scientific and technology standpoints. As I did in **other cases**, this is organized as a large FAQ, based on the typical questions you may ask yourself when looking at vendors logical qubits announcements. It shows the links between the concepts, techniques, figures of merit, software and hardware components. It is written for multiple audiences, and particularly for quantum circuit developers who want to understand how and when their large circuits will be supported by FTQC systems, and which associated figures of merit are relevant. I also consolidate the experimental and theoretical work from FTQC industry vendors.

You can [download it here](#) or with clicking on the image below (45 pages PDF).

<b>How to compare logical qubits?</b>		<b>I. Introduction</b>	
Olivier Ezratty <sup>1,2</sup> <sup>1</sup> EPFL Research Lab, <i>Le Kremlin-Bicêtre, France</i> <sup>2</sup> Quantum Energy Institute (Dated: March 10, 2026)		While several "quantum advantages" have been claimed with NISQ quantum computers (entry intermediate scale quantum computing) in several quantum physics simulation experiments [1–6], the consensus with quantum computer science academics and industry vendors is that industry utility quantum advantage will necessitate the use of FTQC (fault-tolerant quantum computing) [7, 8].	
As the transition from NISQ (entry intermediate scale quantum computing) to FTQC (fault-tolerant quantum computing) is going on, quantum scientists and industry vendors face a complex challenge not only to deliver what's in their plans, blueprints and roadmaps but also on how to communicate about it. Many underlying concepts and figures of merit deserve to be explained given all logical qubits are not born equal and experiments are quite different from one to the other. This paper is structured as a tutorial and review paper which describes how quantum error correction, logical qubits, and fault tolerance operate from a system engineering standpoint. It also helps understand what quantum computing industry vendors are planning and delivering. It shows the links between concepts, techniques, figures of merit, software and hardware components. It is of particular interest for quantum software developers and engineers who want to connect the dots between circuit size requirements and FTQC systems present in their capabilities. Which vendors are driving the development and experimentation of error correction and fault-tolerance engines, we outline that their critical path is in the improvement of the scaling of their hardware, physical qubit operation fidelities, and connectivity.		In most cases, NISQ algorithms face various limitations, particularly when being based on variational circuits, which are plagued by scaling problems like barren plateaus as the number of qubits increases [9]. These circuits can exploit techniques like quantum error mitigation [10] and improvements in physical qubit fidelities. It can currently extend their reach to about 7,500 physical gates and 100 to 200 physical qubits. But industry-grade algorithms require between a million gates ( $10^6$ ) [7] and a trillion gates ( $10^{12}$ ), at not beyond $\sim 10^5$ for some resource estimation (in computational fluid dynamics and complex chemical simulations) [8, 11]. Only this capability will enable the execution of large gate-based quantum circuits supporting a wealth of quantum algorithms for quantum chemistry simulations, solving various linear equations, up to, potentially, reaching the realm of quantum machine learning and combinatorial optimizations [12].	
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This paper is structured as follows:

- **Introduction** which looks at what computer information science specialists may look for in industry vendor achievements as well as roadmaps, and how to find it. It describes the difference between quantum error correction and fault-tolerant quantum computing. It summarizes in a large table the key figures of merit of QEC and FTQC to look at when evaluating vendor's achievements (*below*, look at the paper for the caption).

General information			QEC features							FTQC features										
quantum computing hardware vendor	number of logical qubits	supporting physical qubits	main QEC codes	logical memory experiment	break-even logical error rate	leakage error correction	erasure error correction	correlated error correction	< break-even fidelities	single qubit logical gate	single logical error rate	two qubit logical gate	two qubit error rate	lattice surgery	magic state preparation	gate teleportation	code switching	postselection or detection	logical GHZ fidelity	full universal gate set support
QuEra	96 [39]	448 [39]	color codes	[41]	[41]	[39]	[39]	[39]	[41]	[39, 41]	[39]	[39, 41]	[39, 41]	[39, 42]	[39]	[39]	[39]	[39]	[39]	[41]
Infleqtion	12 [43]	114 [43]	qLDPC variants	[43]	[43]	[43]	[43]			[43]		[43]								
Atom Computing	24 [44]	208 [44]	Bacon Shor, 4D code, and other codes [44]	[44]			[44, 45]			[44]		[44]						[44]		
Pasqal	2	4																yes		
Quantinuum	48 [46]	98 [47]	Tesseract, Iceberg, concat	[48]	[49]		[48]		[49]	[48, 50]	[49]	[48, 50]	[49]		[51]	[51]		[48]	[49]	[51]
IonQ	12 (2026)	256 (2026)	qLDPC bb [52]	[53]	[53]		[54]													
AQT	2	30	cc	[55, 56]	[57]	[58]				[56]	[56]	[59]	[60]	[57]	[59]	[59]	[59]			[59]
Google	1 [61]	105 [61]	sc, cc	[61]	[61]	[61]		[61]	[61]					[62]	[62]		[62]	no		
IBM	200 (2029)	nx120	gross code (bc)		[24]	[24]				[24, 63]		[24, 63]		[24]	[24, 25, 64-66]	[24]	[67]			
IQM	4-36 (2026)	54 (2025)	bc, tile codes (qLDPC)	[68]						[69]		[69]								
Alice & Bob	100 (2030))	2000 (2030)	LDPC, elevator codes							[70]		[70, 71]		[72]	[72]					
PsiQuantum	100 (2030)	1M (2030)	qLDPC, sc, dual rail				[73, 74]			[73, 74]		[73, 74]		[75]	[73-75]					
Xanadu			GKP, qLDPC, bb				[19, 76, 77]			[19, 76, 77]		[19, 76, 77]			[19, 76, 77]					
Quandela		12	Floquet							[78]		[79]								
ORCA Quantum		12	qLDPC, sc			not applic	[80]			[80]		[80]								

- **QEC basics** describes how quantum error correction works on a logical qubit memory, what types of errors are corrected and how. It is focused on surface, color, and qLDPC codes.
- **Logical qubits** describes some basics on the very notion of logical qubits and some related sizing aspects.
- **Fault-tolerance** describes the key features of fault-tolerance and how they are implemented, particularly for the realization of logical quantum gates. It quantifies the space, time and energetic overheads of QEC/FTQC.
- **Industry vendors QEC-FTQC outlook** describes the current achievements from industry vendors across multiple qubit modalities as well as maturity with a mix of experiments, theoretical work, and blueprints. This work often comes from the vendors and from the academic labs which are working with them.

The **TL;DR** summary is that vendors drive two heavy locomotives in parallel: develop error correction and fault-tolerance algorithmic solutions, and improving the scaling of their hardware as well as gate operations fidelities. The slower they are in the second, the harder it is for them to deliver fully functional logical qubits.

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