



an (educated) end-user view of hardware roadmaps

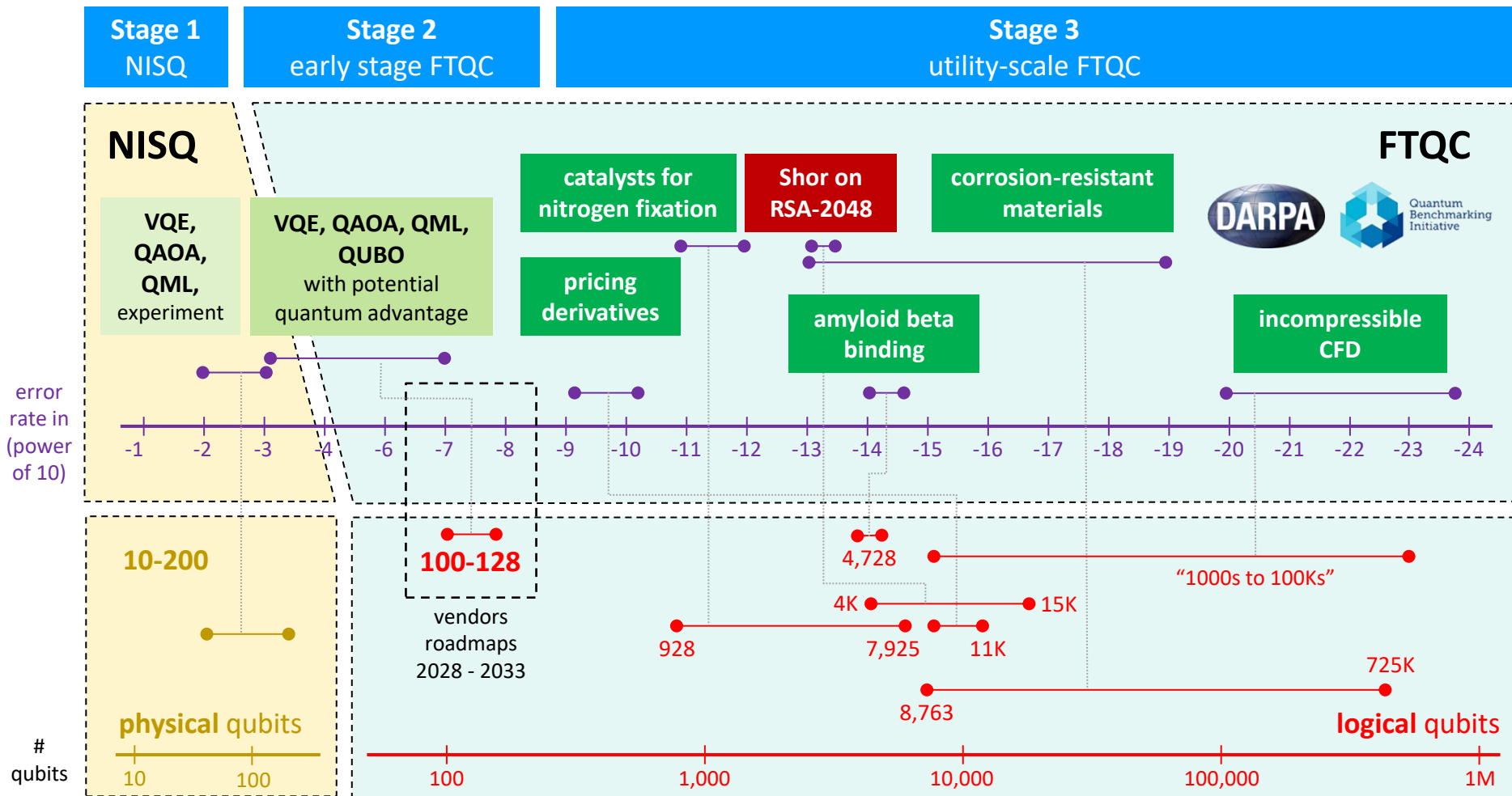


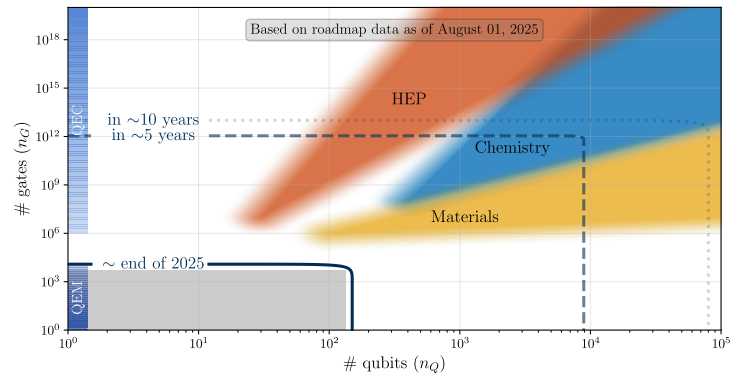
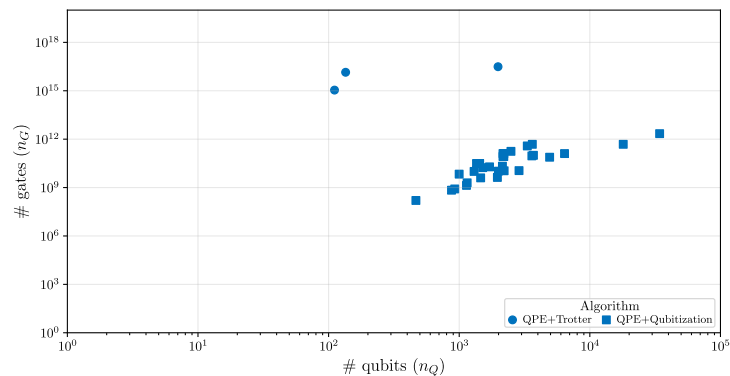
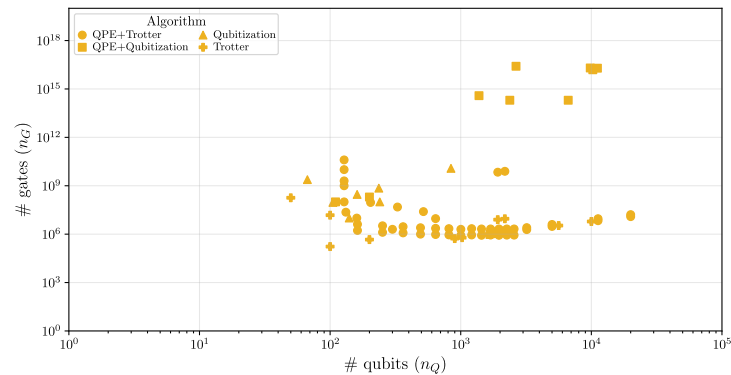
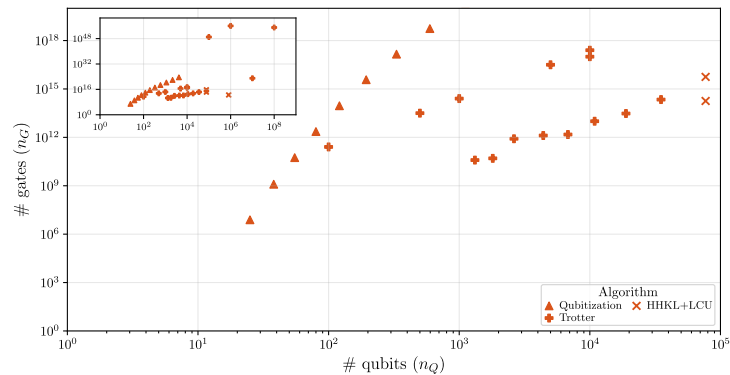
Olivier Ezratty

⟨ ... | free electron | QEI cofounder | ... ⟩

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Q2B Paris, September 24th, 2025

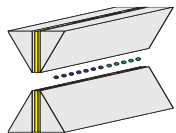




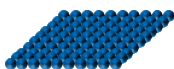
[Quantum Computing Technology Roadmaps and Capability Assessment for Scientific Computing - An analysis of use cases from the NERSC workload](#) by Daan Camps, et al, arXiv, September 2025 (69 pages).

>90 QPUs industry vendors!

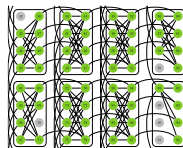
atoms



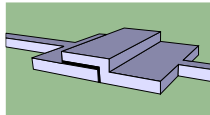
trapped ions



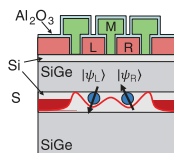
cold atoms



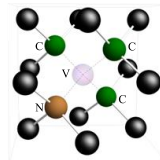
annealing



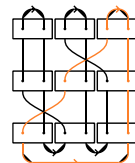
superconducting



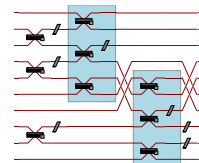
silicon



vacancies



topological



photons



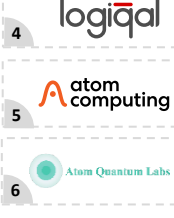
1



4



3



6



QILMANJRO

NEC



7



8



9



10



11



12



13



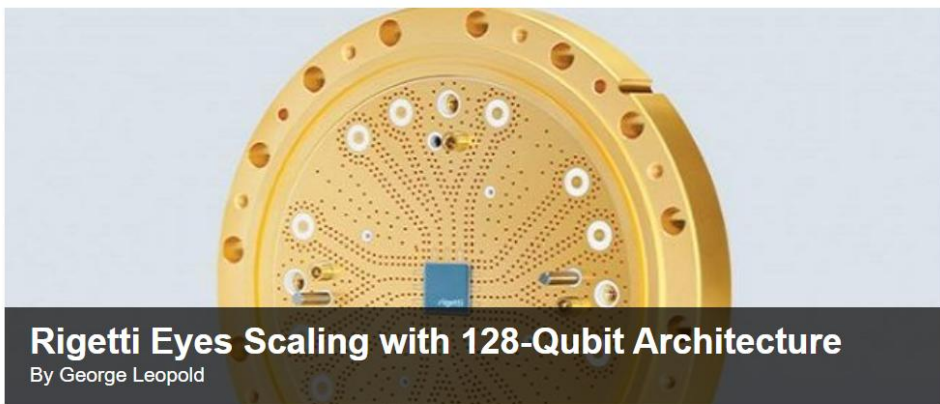
14



15



16



August 10, 2018

➔ **2025:**
84 qubits (Ankaa)
36 qubits (better fidelities)

2025:
36 qubits (Forte)



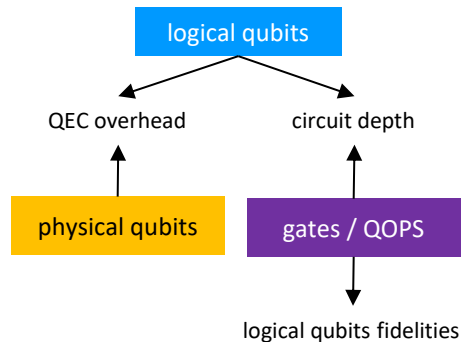
IonQ Has the Most Powerful Quantum Computers With 79 Trapped Ion Qubits and 160 Stored Qubits

December 11, 2018 by [Brian Wang](#)

what should we have in FTQC roadmaps?

bare minimum

- # logical qubits.
- supported circuit size / logical error rates.
- # physical qubits.

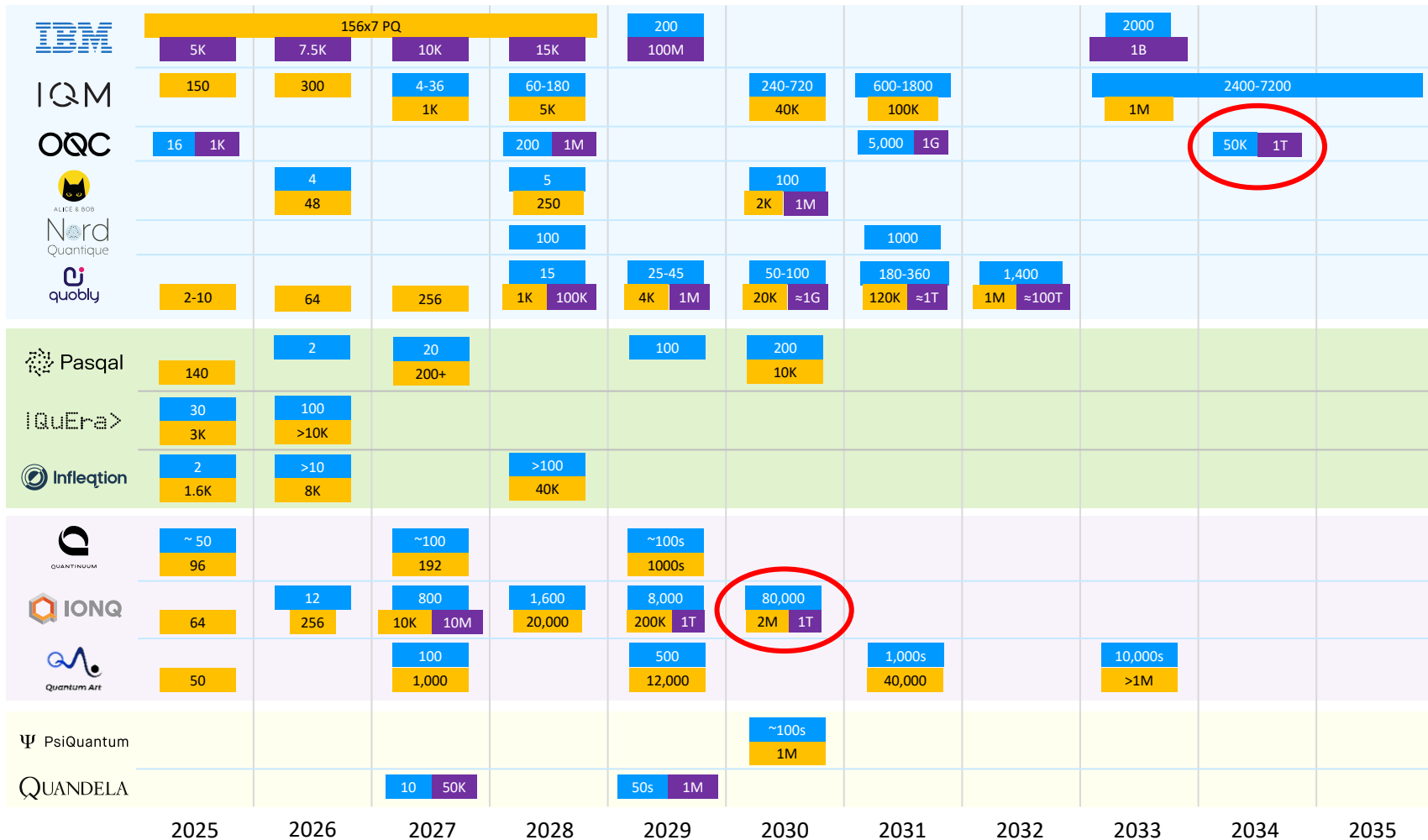


nicer to have

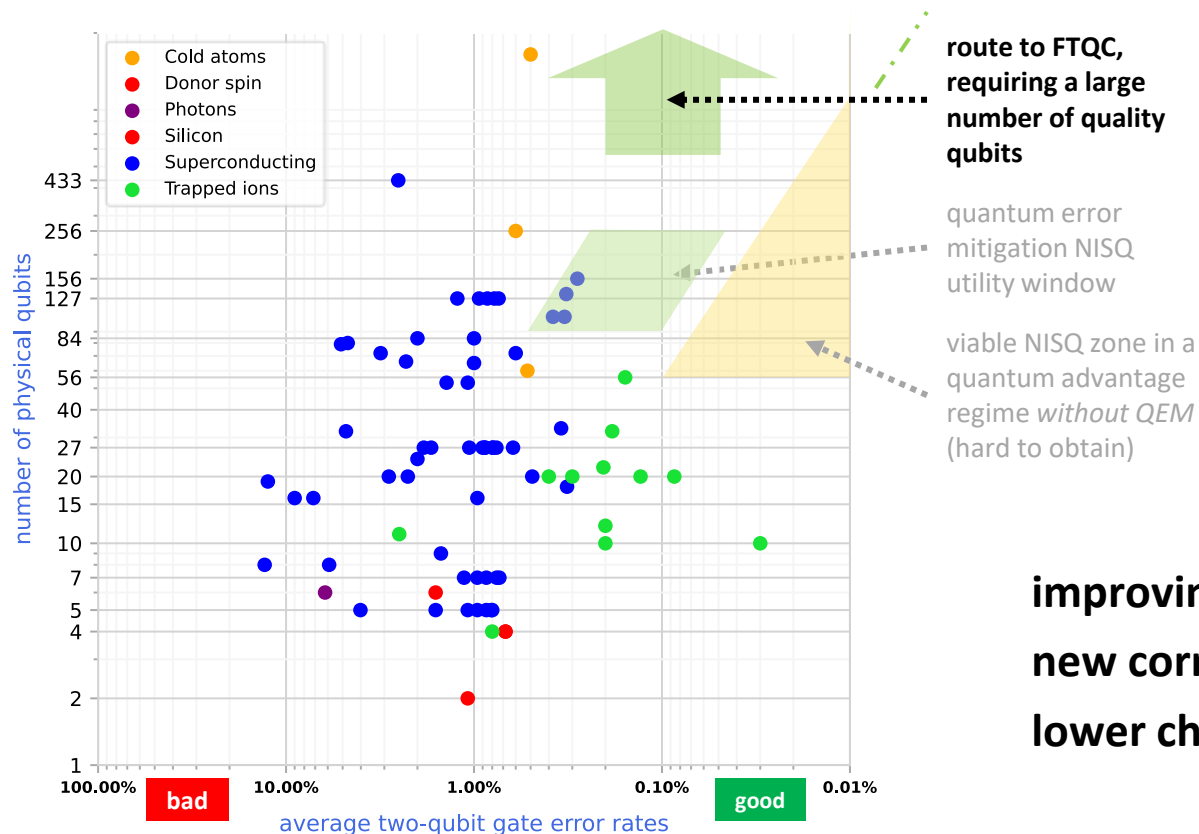
- clock speed and QLOPs/s.
- planned QEC codes and methods.
- processor size & reliance on QPU interconnect.

- peak power consumption in W.
- components operating temperature.
- QPU weight and size.
- operational constraints like temperature variability.
- components MTBF.
- capex/opex cost structure.

operational metrics

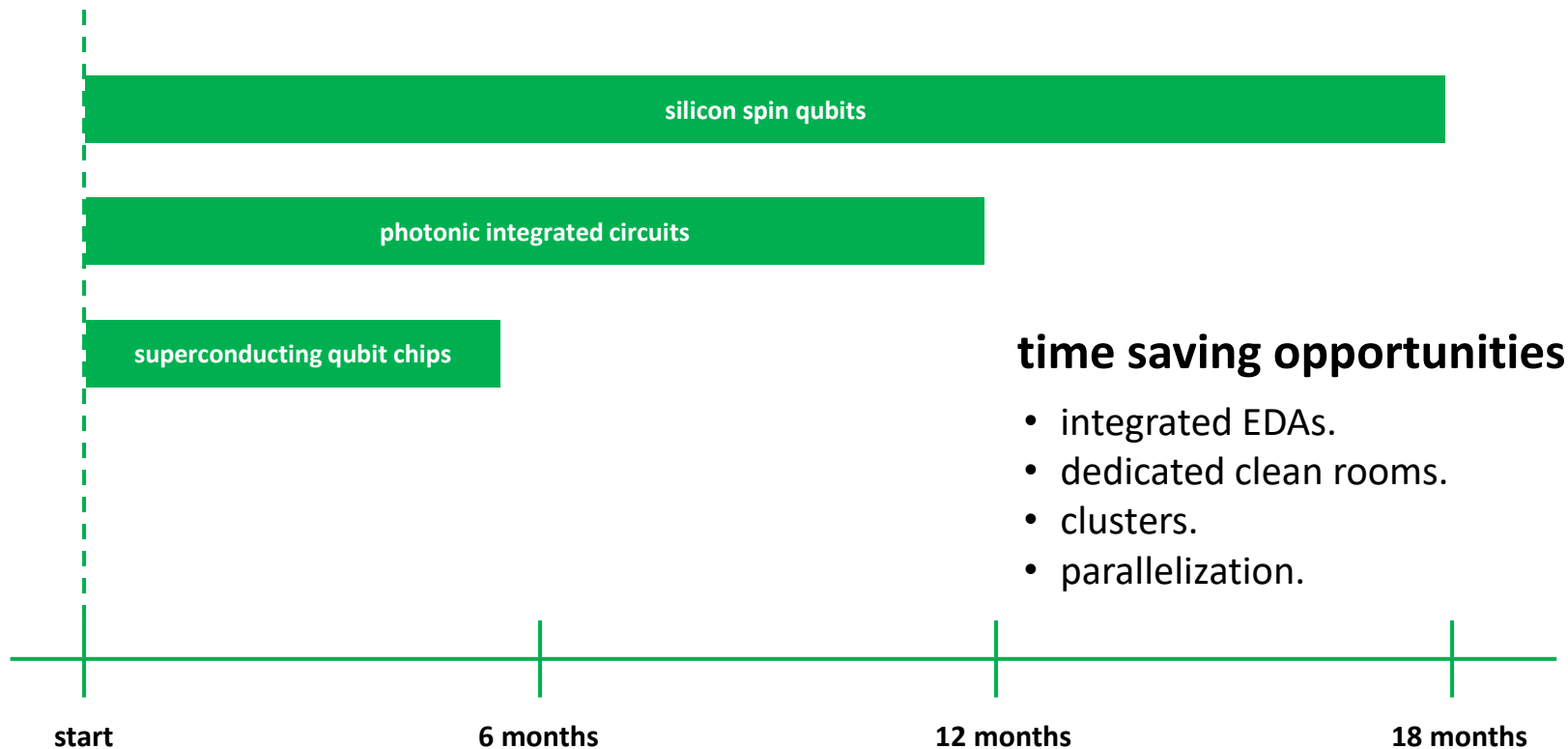


challenge 1: qubit *infidelities*

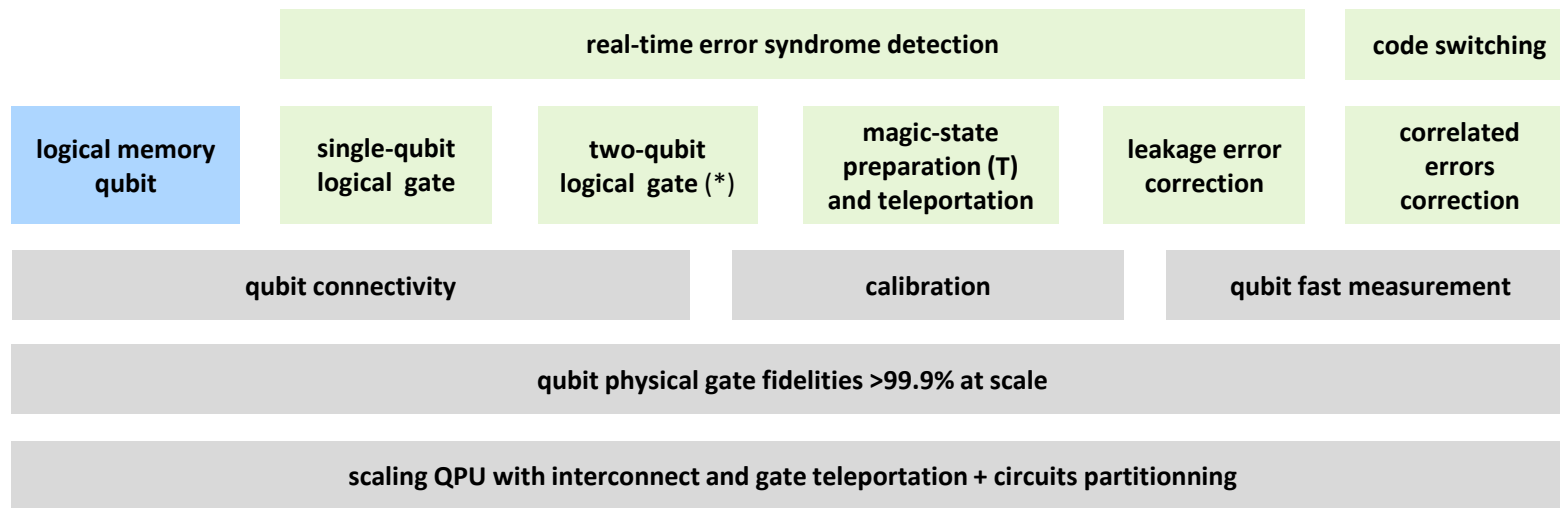


improving qubit fidelity at scale?
new correlated noise sources?
lower chips variability?

challenge 2: chips iteration cycles



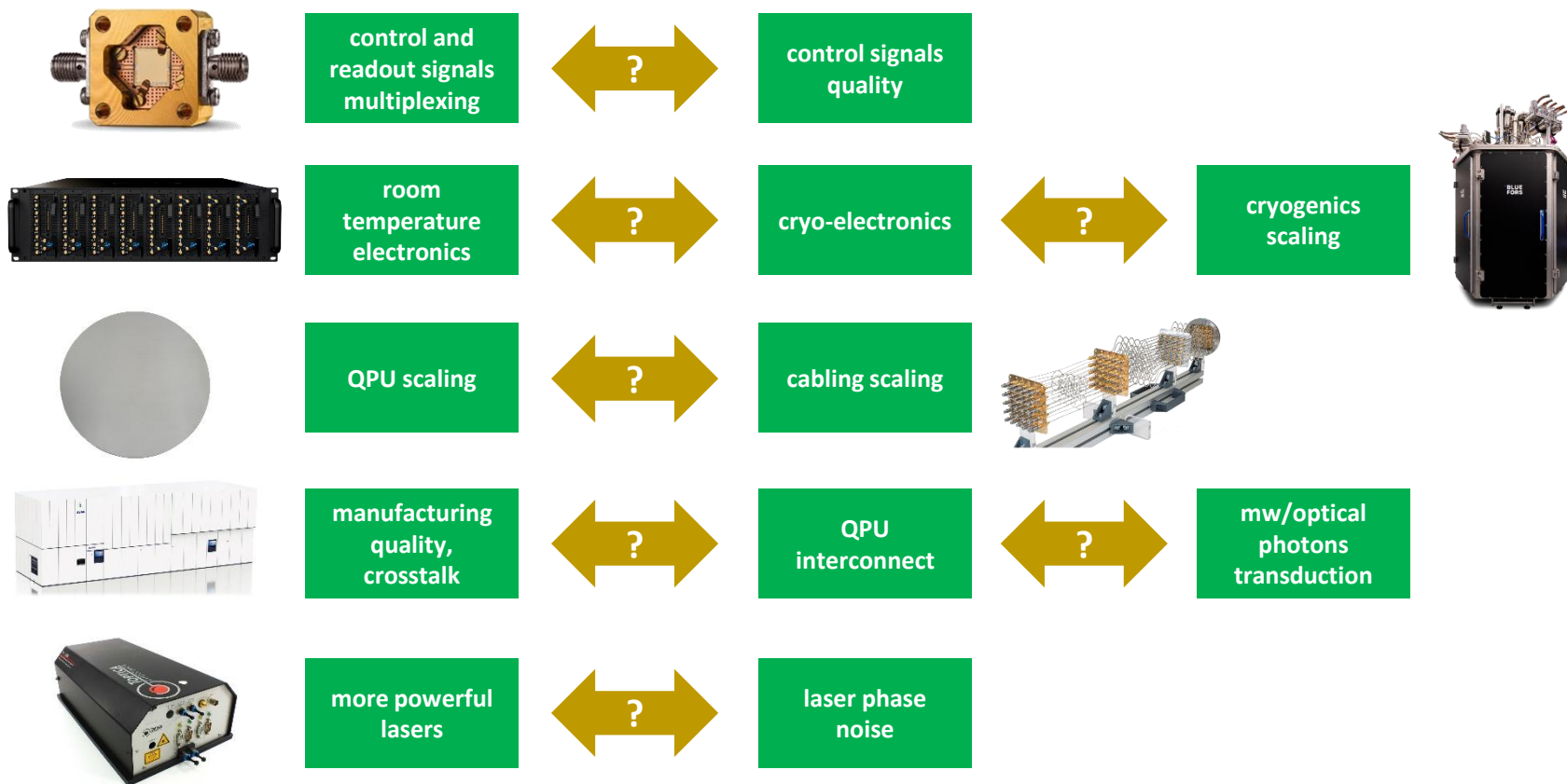
challenge 3: QEC/FTQC integration



(*): not using post-selection which doesn't scale to deep circuits.

blue QEC basic component.
green FTQC component.
grey QEC hardware enablers.

challenge 4: enabling technologies



challenge 5: software

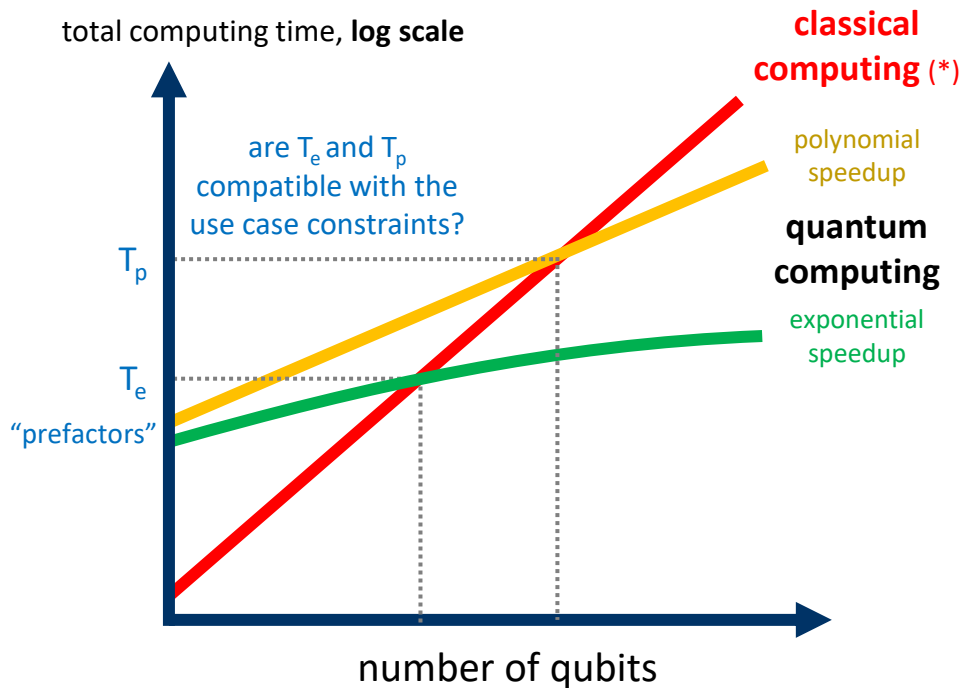
practical vs theoretical speedups

compiler & optimizers scalability

classical pre- and post-processing costs (chemistry)

verification, certification, benchmarking.

classical computing progress (MPS, DMRG).



inspired by [Opening the Black Box inside Grover's Algorithm](#)

by E. Miles Stoudenmire and Xavier Waintal, PRX, November 2024.

(*) for a fair comparison, the classical computer can be as expensive and/or energy hungry as the QPU.

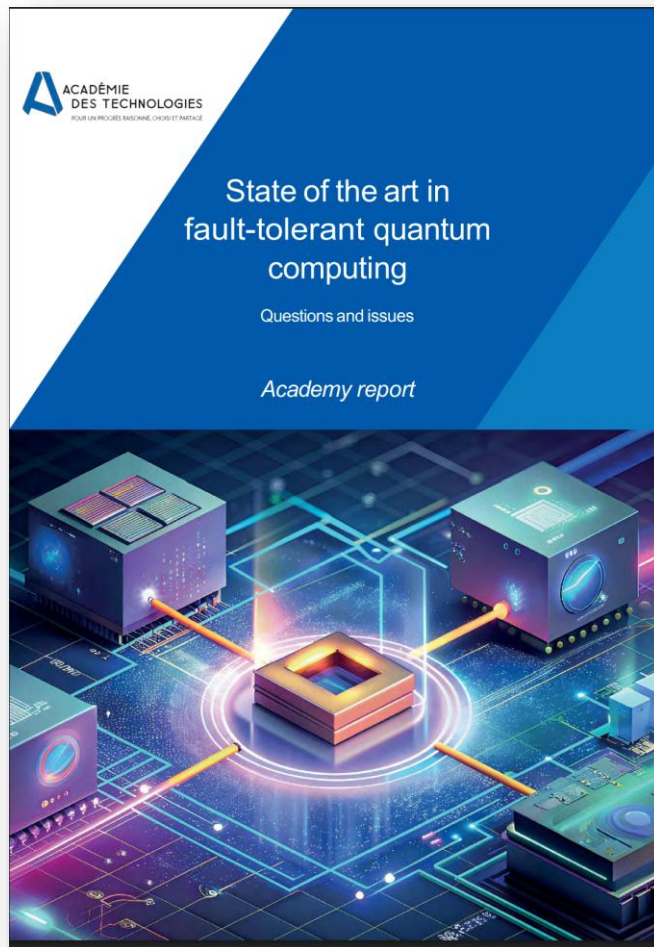
end-user dialog with vendors

vendors to end-users

- explain how challenges 1, 2, 3 and 4 are handled.
- information on R&D workload distribution (partners, academics).
- adopt benchmarking methods.
- update roadmap every year.

end-users to vendors

- provide key use cases needs and resource estimates.
- adopt benchmarking methods.
- learn classical best-in-class methods and hardware.
- track vendors roadmaps every year.
- look at QPU economics.



next: Thursday 25th, 4:00 PM



the energetics challenges of FTQC



Olivier Ezratty

⟨ ... | free electron | QEI cofounder | ... ⟩

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Q2B Paris, September 25th, 2025

discussion



get the slides
now